e2v technologies

CCD60 Back Illuminated Electron Multiplying CCD Sensor

INTRODUCTION

The CCD60 is part of the new L3Vision™ range of products from e2v technologies. This device uses a novel output amplifier circuit that is capable of operating at an equivalent output noise of less than one electron at frame rates of 1 kHz.

The sensor is a frame transfer device, designed for high frame rate applications such as wavefront sensing or adaptive optics. The device operates in inverted mode to suppress dark current. A variant exists to provide image section antiblooming.

The e2v technologies back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by a low noise output amplifier.

The multiplication gain may be varied by adjustment of the multiplication phase amplitude R∅2HV.

GENERAL DATA

Active image area	3.072 x 3.072 mm
Image section active pixels	128 (H) x 128 (V)
Image pixel size	24 x 24 μm
Number of output amplifiers	1
Fill factor	100%

PACKAGE DETAILS (Nominal, see Fig. 14)

Ceramic Package 24-pin DIL

Overall dimensions	32.9 x 20.1 mm
Number of pins	24
Inter-pin spacing	2.54 ± 0.15 mm
Opposite row spacing	15.24 ± 0.25 mm
Window material	quartz or removable glass
Mounting position	any

Pin 1 is identified as shown in Fig. 14.

STORAGE AND OPERATION TEMPERATURE EXTREMES

	MIN	MAX
Storage temperature (°C)	−200	+100
Operating temperature (°C)	−120	+75
Temperature ramping (°C/min)	-	5

Note: Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

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TYPICAL PERFORMANCE SPECIFICATIONS

The following are for operation of devices at 500 Hz frame rate and at typical operating voltages. Parameters are given at 293 K unless specified otherwise. Where parameters are different in the normal and high gain mode, both are given.

PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity (normal mode) (see note 1)	$\mu V/e^-$	-	1.2	-
Multiplication register gain (see notes 2, 3 and 4)		1	-	1000
Peak signal - non-inverted mode operation (see note 5): non-antibloomed antibloomed	 e^-/pixel e^-/pixel	 - -	 530k 260k	 - -
Peak signal - inverted mode operation: non-antibloomed antibloomed	 e^-/pixel e^-/pixel	 - -	 240k 130k	 - -
Charge handling capacity of multiplication register (see note 6)	e^-/pixel	-	800k	-
Readout noise at 11 MHz (normal mode) (see note 7)	e^- rms	-	100	-
Readout noise at 11 MHz (high gain mode)	e^- rms	-	<1	-
Integrated dark signal at 293 K (see note 8)	e^-/pixel/s	-	900	-
Integrated dark signal non-uniformity (DSNU) at 293 K (see notes 8 and 9)	e^-/pixel/s	-	3400	-
Excess noise factor (see note 10)		-	$\sqrt{2}$	-
Maximum readout frequency (settling to 1%) (see notes 5 and 11)	MHz	-	11	18
Maximum parallel transfer frequency	MHz	-	10	-

NOTES

1. Measured at a pixel rate of 1 MHz.
2. The typical variation of gain with R∅2HV is shown in Fig. 1.
3. The typical variation of gain with R∅2HV at different temperatures is shown in Fig. 1.
4. Some increase of R∅2HV may be required throughout life to maintain gain performance. Adjustment of R∅2HV should be limited to the maximum specified under Operating Conditions.
5. These values are predicted from design and not measured.
6. When multiplication gain is used, a linear response of output signal with input signal is achieved for output signals up to typically 400 ke^-.
7. These noise values are dominated by reset noise in the output amplifier and it is assumed that correlated double sampling (CDS) is not being implemented. If CDS is used to suppress the reset component, a noise of 10 e^- can typically be achieved at a pixel rate of 1 MHz with a noise floor of 4 e^- rms. At 11 MHz the noise with CDS is about 35 e^-. These values are inferred by design and not measured.
8. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, the dark signal will be dominated by an additional component generated during readout. Operating at a temperature of 293 K and 500 Hz frame rate, the readout component contributes typically 3.6 e^-/pixel/frame at a gain of 1000 and referred to the image area, and has a temperature dependence consistent with non-inverted mode operation. There exists a further weakly temperature dependent component, the clock induced charge, which is independent of the integration time and is a function of the operating biases and timings employed. For more information, refer to the e2v technologies technical note: "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".
9. DSNU is defined as the 1σ variation of the dark signal.
10. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.
11. A maximum readout frequency of 18 MHz is expected to be achievable with a 20 pF load, output settling to 1%, and single sampling.

ORDERING INFORMATION

PART NUMBER	OPERATING MODE	ANTIBLOOMING	COATING	WINDOW
CCD60-01-*-B89	2-phase IMO	None	Midband	Temporary
CCD60-00-*-108	2-phase IMO	Shielded	Midband	Temporary

DEVICE COSMETIC PERFORMANCE

Grade 1 devices are supplied to the blemish specification shown below.

Note that incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

Test Conditions

Operating mode	Device run in 2-phase inverted mode at a rate of 500 frames/second.
Sensor temperature	22 $\pm$ 3 °C.
Multiplication gain	Set to approximately 1000.
Illumination	Set to give a signal level of approximately 50 e^-/pixel/frame.

BLEMISH SPECIFICATION

Black Columns Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A black column contains at least 9 contiguous black defects.

White Columns White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum specified dark signal level. A white column contains at least 9 contiguous white defects.

Pin-Head Columns Pin-head columns are manifest as a partial dark column with a bright pixel showing photoresponse at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

SPECIFICATION FOR GRADE 1 DEVICES

PARAMETER	SPECIFICATION
White Columns	0
Black Columns	0
Pin-head Columns	0

Figure 1: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH R∅2HV AT DIFFERENT TEMPERATURES

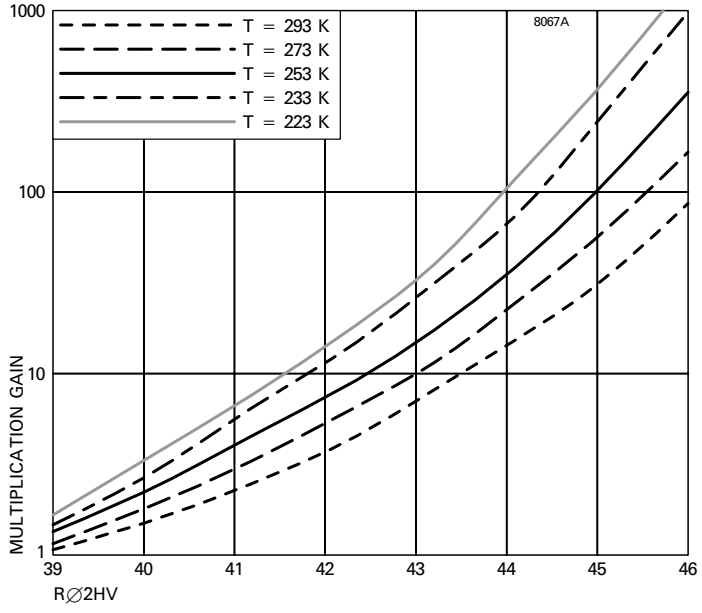


Figure 2: TYPICAL VARIATION OF INTEGRATED DARK SIGNAL WITH TEMPERATURE (No window, T = 20 °C)

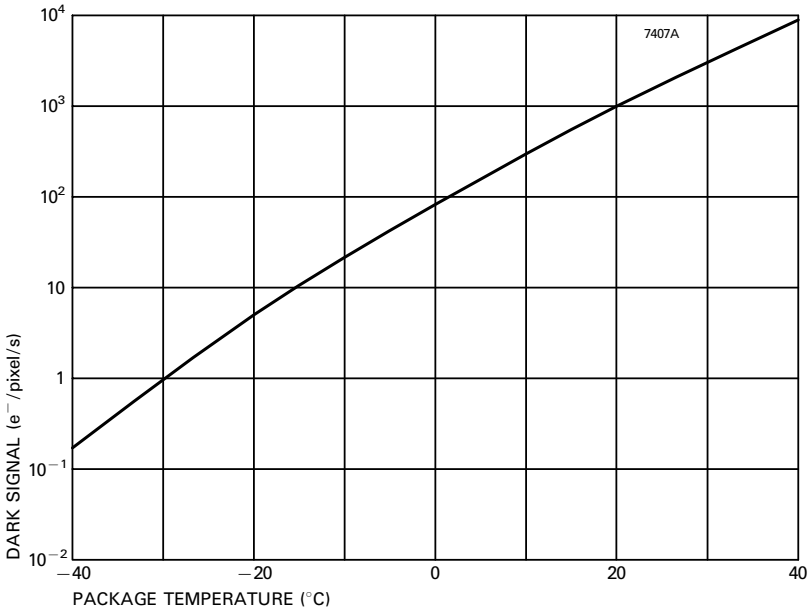
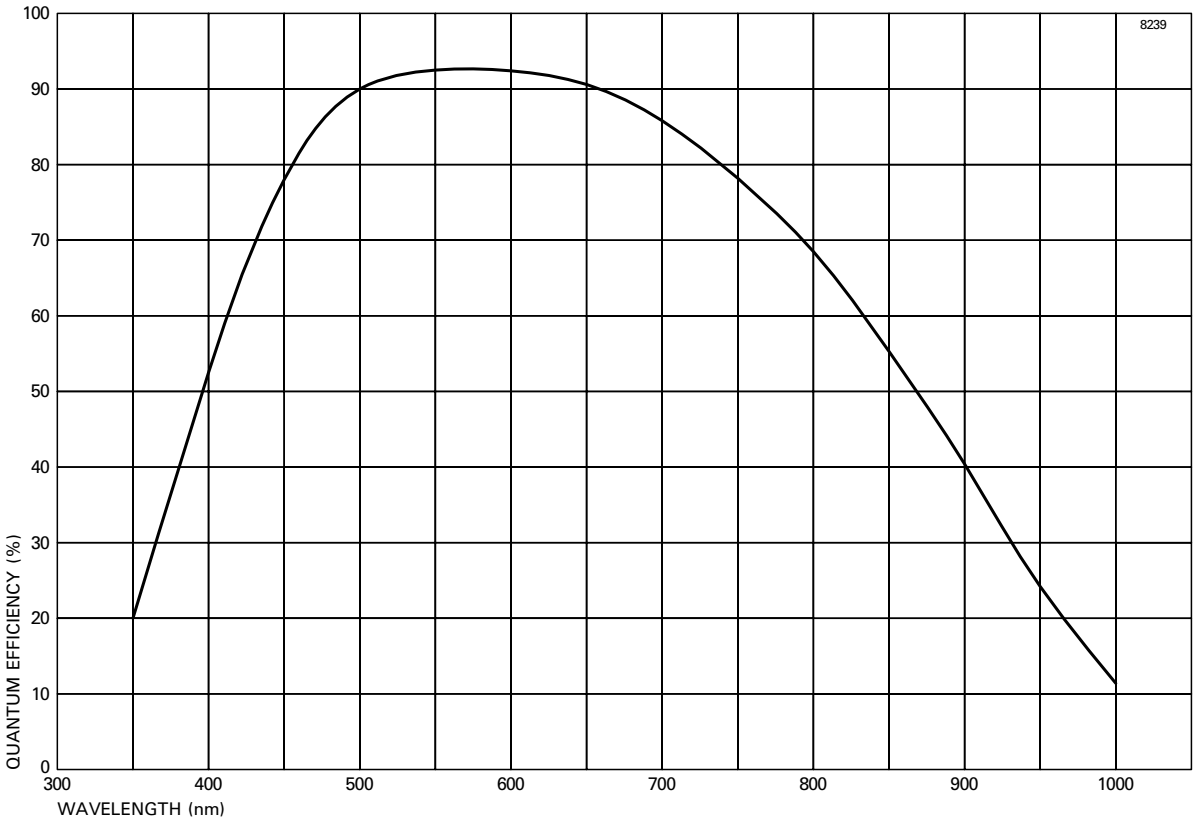


Figure 3: TYPICAL SPECTRAL RESPONSE, MIDBAND COATED (At +20 °C, no window)



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to SS.

PIN	CONNECTION	MIN (V)	MAX (V)
1	S∅2	−20	+20
2	S∅1	−20	+20
3	ABD	−0.3	+28
4	IG	−20	+20
5	I∅1	−20	+20
6	SS	0	
7	∅R	−20	+20
8	SS	0	
9*	OS	−0.3	+25
10	OD	−0.3	+32
11	R∅DC	−20	+20
12	R∅2HV	−20	+50
13	RD	−0.3	+25
14	OG	−20	+20
15	R∅2	−20	+20
16	R∅1	−20	+20
17	R∅3	−20	+20
18	R∅1	−20	+20
19	R∅2	−20	+20
20	DG	−20	+20
21	S∅2	−20	+20
22	S∅1	−20	+20
23	I∅2	−20	+20
24	S∅1	−20	+20

* Permanent damage may result if, in operation, OS experiences short-circuit conditions.

Maximum voltages between pairs of pins:

PIN	CONNECTION	PIN	CONNECTION	MIN (V)	MAX (V)
10	OD	9	OS	−15	+15
12	R∅2HV	11	R∅DC	−20	+50
12	R∅2HV	11	R∅DC	−20	+50
12	R∅2HV	17	R∅3	−20	+50
Output transistor current (mA)					20

ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

CONNECTION	PULSE AMPLITUDE OR DC LEVEL (V)		
	Min	**Typical**	**Max**
I∅1,2 high	+4 (see note 12)	+5	+7 (see note 12)
I∅1,2 low	-	−5	-
S∅1,2 high	+4 (see note 12)	+5	+7 (see note 12)
S∅1,2 low	-	−5	-
R∅1,2,3 high	+10	+12	+13
R∅1,2,3 low	-	0	-
R∅2HV high	+20	+40	+50 (see note 4)
R∅2HV low	0	+4	+5
∅R high	+10 (see note 13)	+12	+13 (see note 13)
∅R low	-	0	-
R∅DC	+2	+3	+5
OG	+1	+3	+5
SS	0	+4.5	+7
OD	+25	+28	+32
RD	+15	+18	+20
IG	-	−5	-
ABD: non-antibloomed devices antibloomed devices	 +20 +10	 +24 +15	 +27 +20
DG low: non-antibloomed devices antibloomed devices	 - -	 0 −5	 - -
DG high: non-antibloomed devices antibloomed devices	 +10 -	 +12 −5	 +15 -

NOTES

12. I∅ and S∅ adjustment may be common.
13. ∅R high level may be adjusted in common with R∅1,2,3.
14. For non-antibloomed devices, it is possible dump unwanted lines of signal by employing the timing diagram in Fig. 10. DG high should be 2 V greater than R∅1,2,3 high. Charge is dumped from the standard register (see Fig. 11) into ABD.

    Users of shielded antibloomed devices wishing to dump unwanted lines are advised to contact e2v technologies.

An external load is required. This can either be a resistor of about 2.2 kΩ (non-critical) or a constant current type of about 7.5 mA. The total on-chip power dissipation at 500 Hz frame rate is approximately 200 - 250 mW, depending on the details of the voltages and clock timings used.

DRIVE PULSE WAVEFORM SPECIFICATION

The following are suggested pulse rise and fall times for operation at 500 Hz frame rate, and with pixel readout at 11 MHz.

CLOCK PULSE	TYPICAL RISE TIME (ns)	TYPICAL FALL TIME (ns)	TYPICAL PULSE OVERLAP
I∅	20	20	@90% points
S∅	20	20	@90% points
R∅1	5	5	@70% points
R∅2	5	5	@70% points
R∅3	5	5	@70% points
R∅2HV	25	25	see note 16
R∅2HV	Sine	Sine	Sinusoid- high on falling edge of R∅1

NOTES

15. Register clock pulses are as shown in Figs. 4 and 5.
16. An example clocking scheme is shown in Fig. 5. R∅2HV can also be operated with a normal clock pulse, as shown in Fig. 4. The requirement for successful clocking is that R∅2HV reaches its maximum amplitude before R∅1 goes low.

ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS				
Connection	**Capacitance to SS**	**Inter-phase Capacitances**	**Total Capacitance**	**Units**
I∅1 (see note 17)	750	100	850	pF
I∅2 (see note 17)	750	100	850	pF
S∅1 (see note 17)	750	100	850	pF
S∅2 (see note 17)	750	100	850	pF
R∅1	36	41	77	pF
R∅2	56	41	97	pF
R∅3	62	60	122	pF
R∅2HV	45	49	94	pF
SERIES RESISTANCES				
Connection	**Approximate Total Series Resistance**			
I∅1	9			Ω
I∅2	9			Ω
S∅1	9			Ω
S∅2	9			Ω
R∅1	7			Ω
R∅2	7			Ω
R∅3	7			Ω
R∅2HV	8			Ω
AMPLIFIER				
Output Impedance	250			Ω

NOTE

17. For operation in the inverted mode. For operation in the non-inverted mode, the capacitance to substrate is 400 pF and the total capacitance is 500 pF.

Figure 4: CLOCKING SCHEME FOR MULTIPLICATION GAIN (Normal clock pulses)

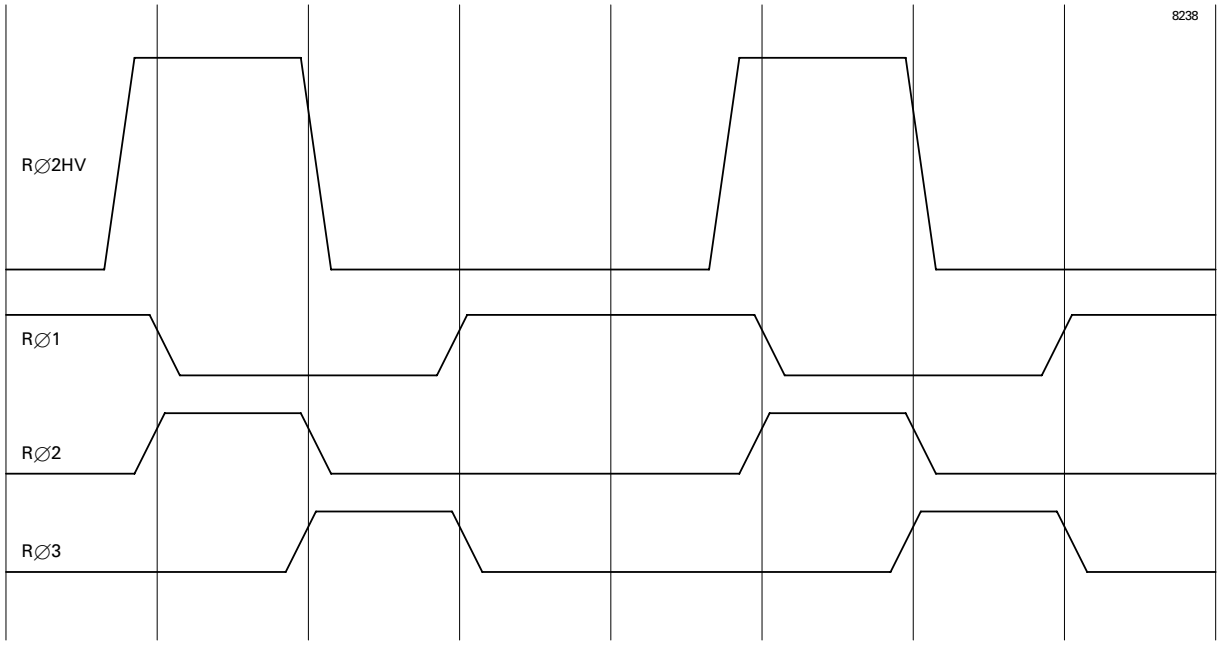
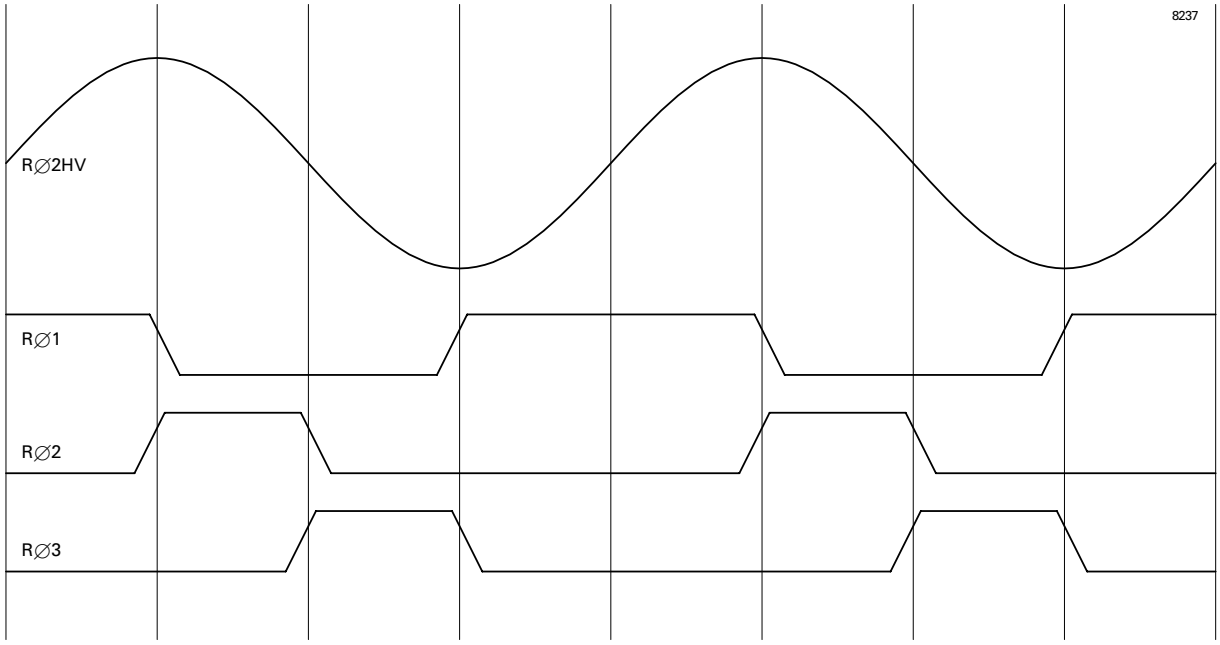
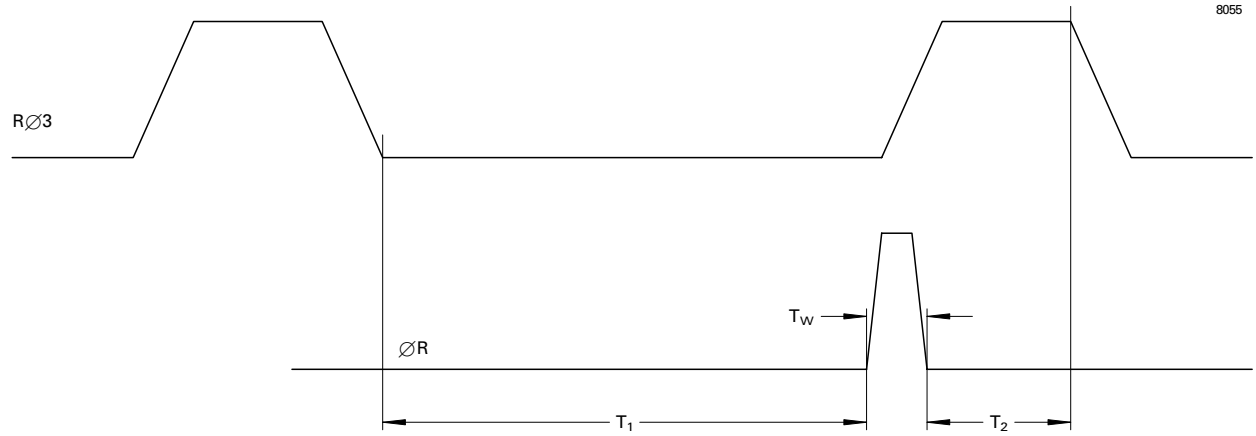


Figure 5: CLOCKING SCHEME FOR MULTIPLICATION GAIN (Sine wave clocks)



PULSE TIMINGS AND OVERLAPS

Figure 6: RESET PULSE



T_W = 10 ns typical
T_1 = output valid
T_2 > 0 ns

Figure 7: PULSE AND OUTPUT TIMING

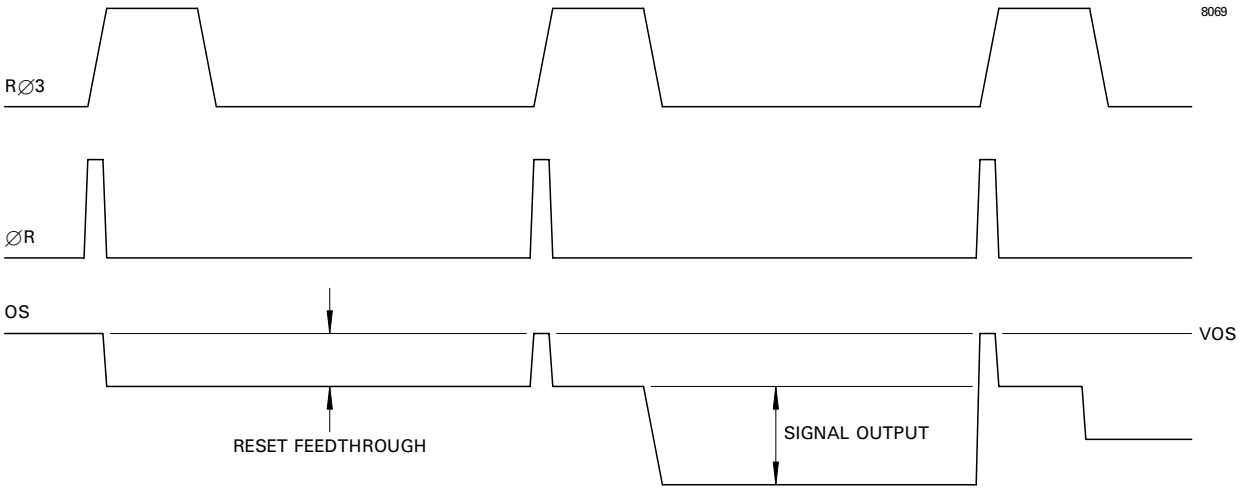


Figure 8: EXAMPLE LINE TIMING DIAGRAM

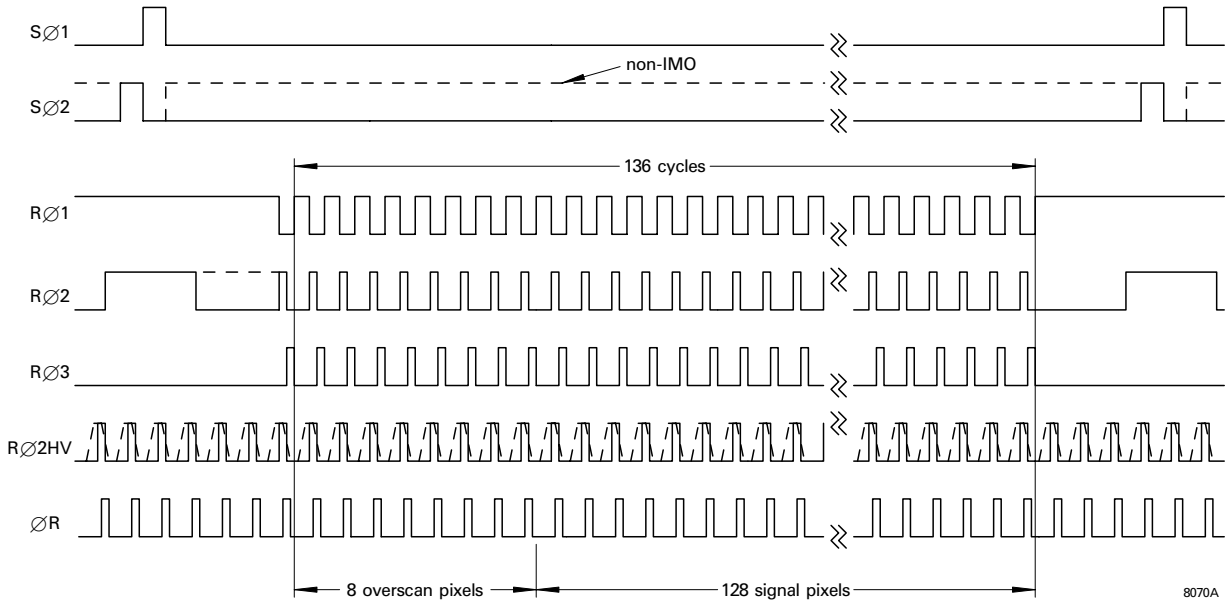


Figure 9: EXAMPLE FRAME TIMING DIAGRAM

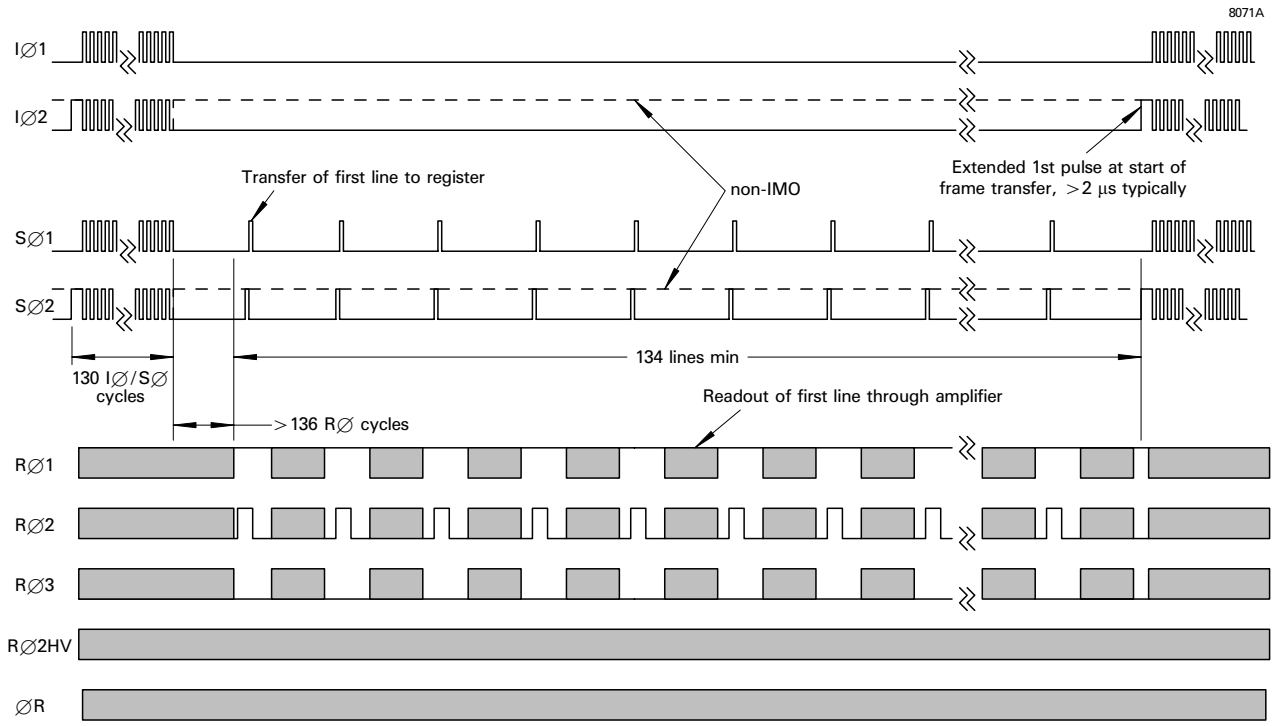


Figure 10: OPERATION OF THE DUMP GATE TO DUMP n LINES OF UNWANTED DATA FROM THE STANDARD REGISTER (Non-antibloomed devices only, see note 14)

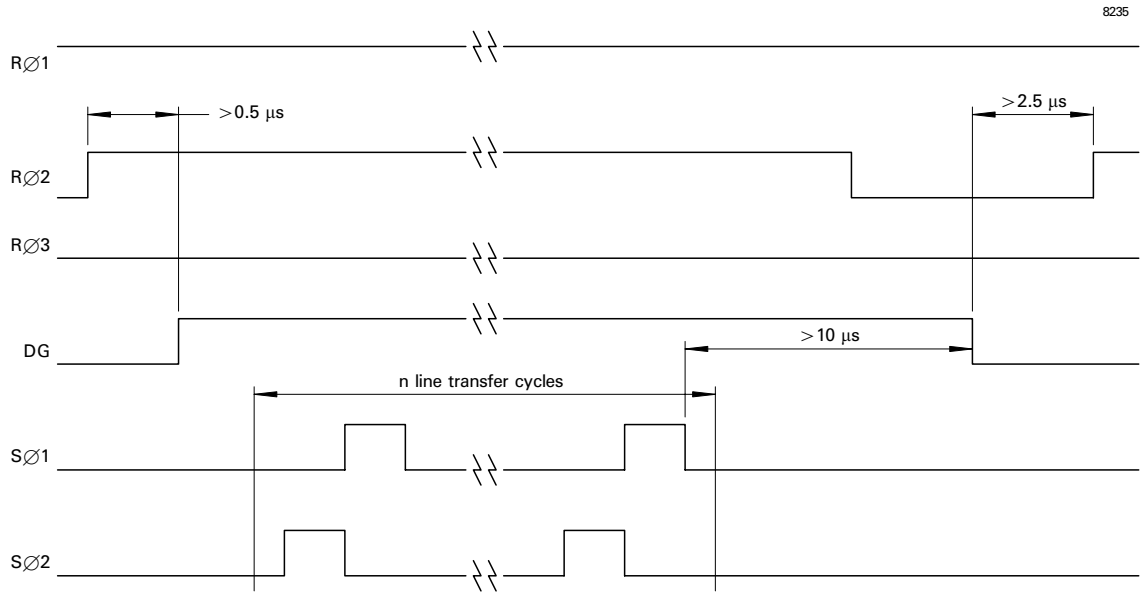


Figure 11: SCHEMATIC CHIP DIAGRAM

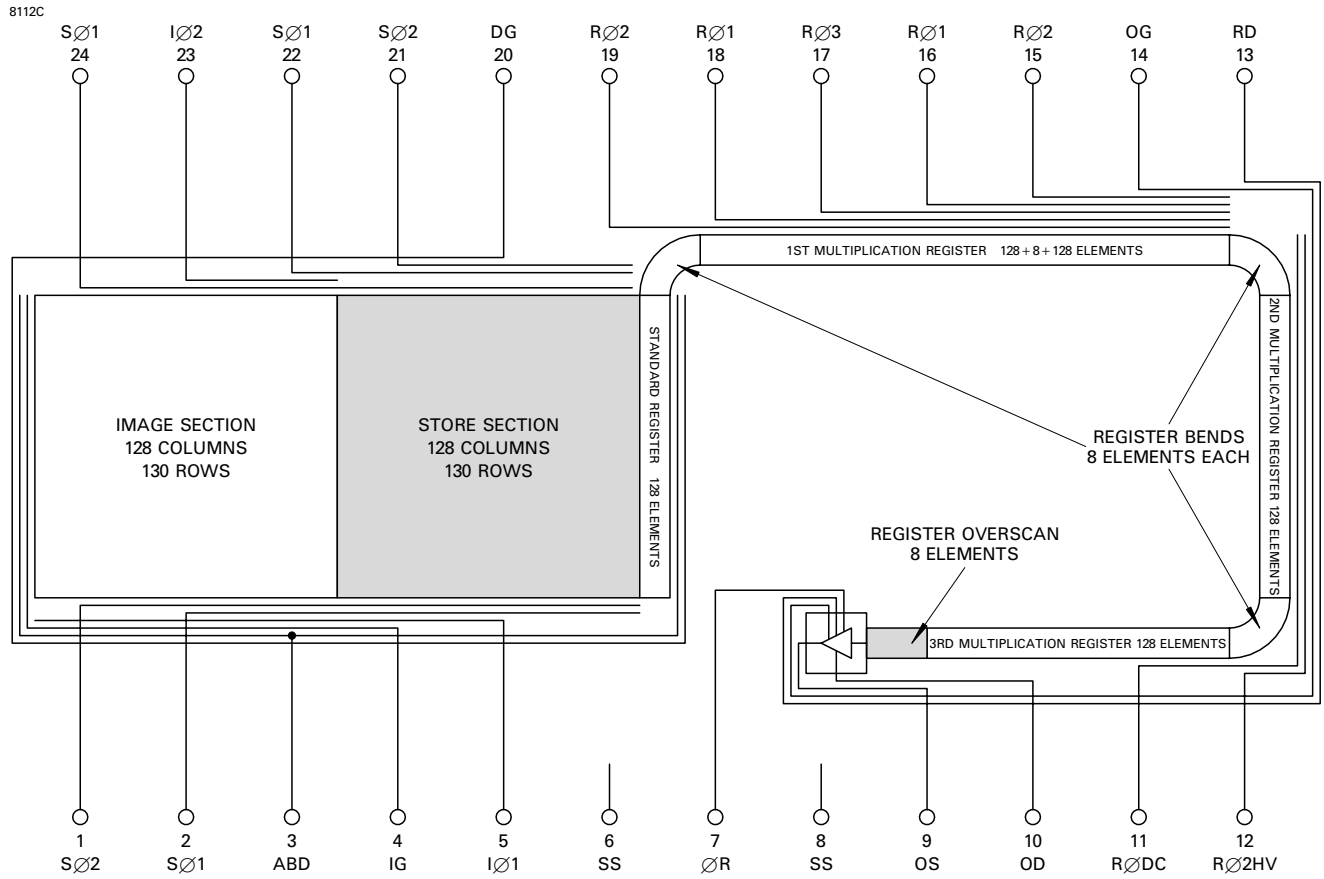
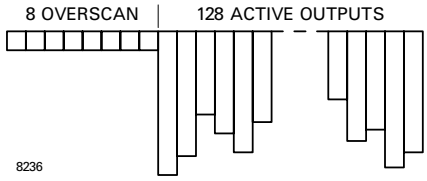


Figure 12: LINE OUTPUT FORMAT



NOTE

18. There is a 4-line propagation delay between transferring a line from the store section to the standard register and reading it out through the output amplifier.

Figure 13: OUTPUT CIRCUIT SCHEMATIC

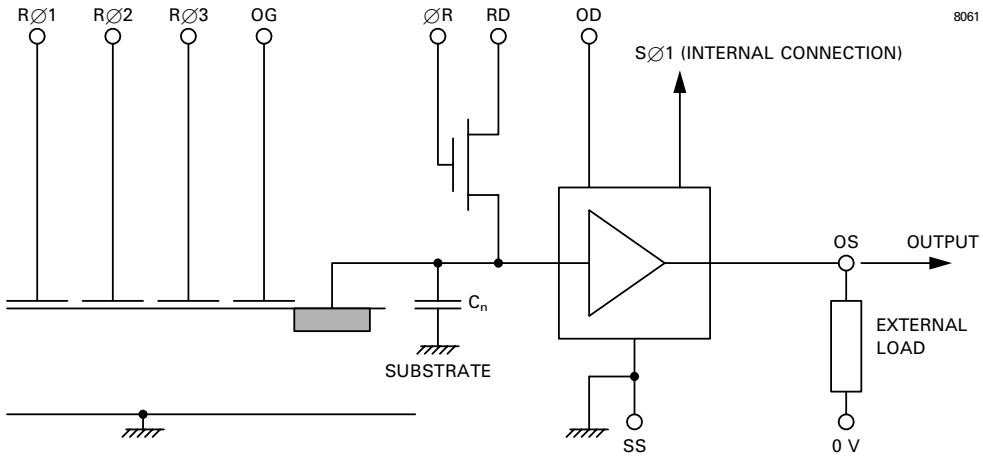
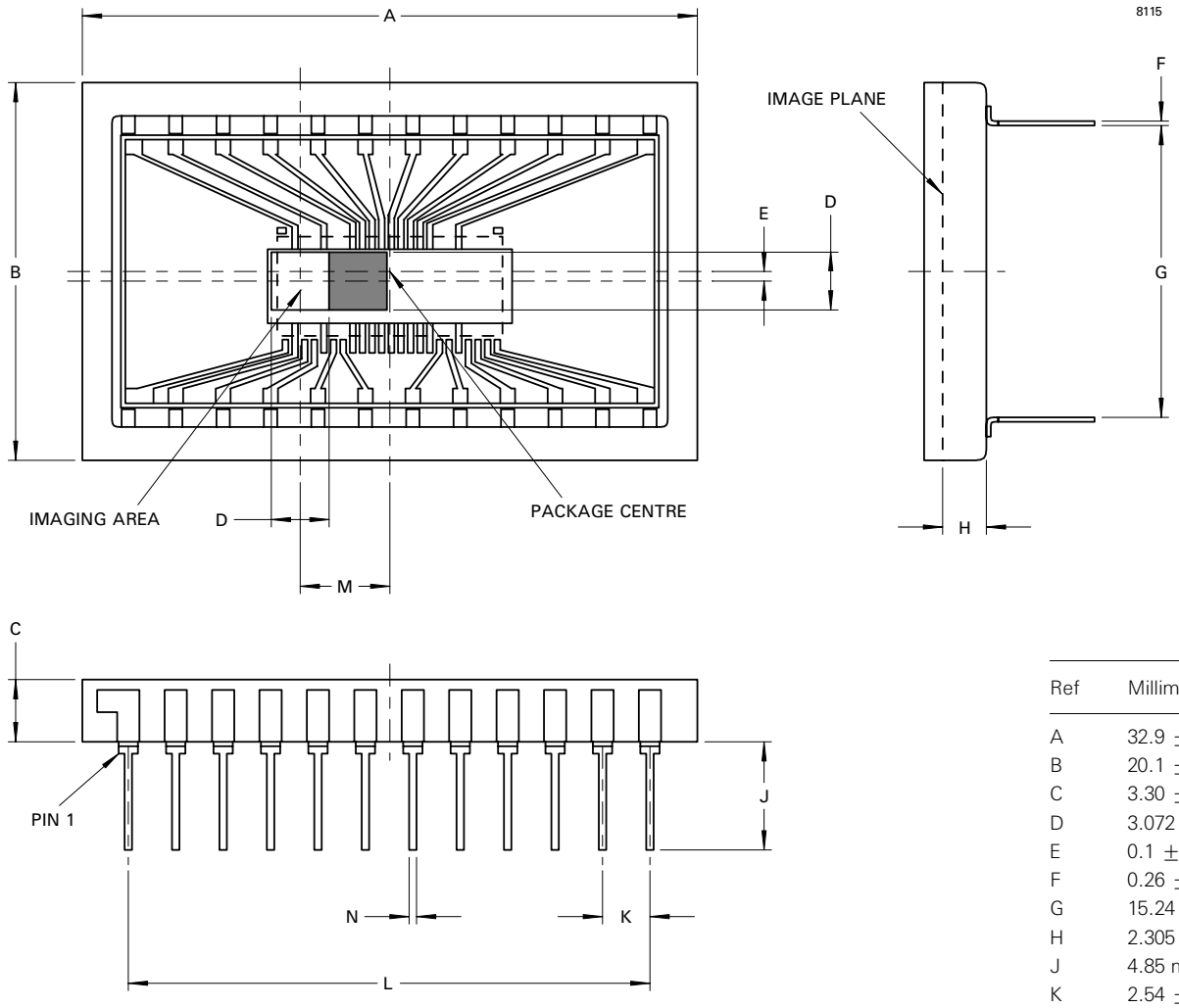


Figure 14: PACKAGE OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	32.9 ± 0.4
B	20.1 ± 0.3
C	3.30 ± 0.35
D	3.072
E	0.1 ± 0.5
F	0.26 ± 0.04
G	15.24 ± 0.25
H	2.305 ± 0.600
J	4.85 min
K	2.54 ± 0.15
L	27.94 ± 0.15
M	4.76 ± 0.50
N	0.46 ± 0.20