CCD262-50 Front-illuminated X-ray Sensor
512 x 1024 Pixels, Full-Frame, Eight Outputs

FEATURES

- 512 (H) x 1024 (V) pixels
- 50 µm square pixels
- Full-frame operation with 8 register sections
- Up to 60 Hz frame rate
- Fabricated using a radiation-hard process
- Front-illuminated
- Three-sides buttable
- Anti-static gate-protection devices

APPLICATIONS

- X-ray crystallography
- General purpose optical

INTRODUCTION

The CCD262 is a full-frame array with 512 x 1024 pixels each 50 µm square, plus 6 extra rows of non-imaging pixels before the read-out register. The read-out register is split into 8 sections each with 64 elements and 4 pre-scan elements leading to an output circuit comprising real and dummy amplifiers. Two-phase non-inverted mode clocking is used throughout.

A frame read-out time of 16.6 ms, corresponding to 60 Hz frame rate, can be possible with the clock timings at “minimum” values and the output circuit giving a sufficiently well-settled output waveform for reliable correlated double sampling to be possible. The “typical” values are more relaxed timings giving a frame read-out time of about 20 ms.

The device is primarily intended for X-ray crystallography and is fabricated with a process variant that minimises the effects of ionising radiation. The device may also find application as a large pixel sensor for general-purpose optical imaging applications.

The device package comprises a metal base with a flexi-lead connector. To facilitate close-butting in a tiled array the distances between the active pixels and the die edges are 300 µm at the sides and 150 µm at the top and the die overhangs the package body at the top and on one side. Note that devices are normally supplied attached to a handing jig in a transport box and guidelines for unpacking and handling should be followed.

VARIANTS

Only the baseline variant is currently available.

SUMMARY SPECIFICATION

Number of pixels	512(H) × 1024(V)
Pixel size	50 µm square
Silicon active thickness	50 µm
Image area	25.6 mm × 51.2 mm
Outputs	8
Package size	See details on p. 14
Focal plane height above base	12.1 mm
Package format	Invar base with flexi lead
Connector	37-pin micro-D
Amplifier responsivity	0.70 µV/e^-
Read-out noise at 5 MHz	100 e^- rms
Minimum frame read-out time	20 ms
Charge storage capacities	
Image area	4M e^-
Register	5M e^-
Output Node	4M e^-
Dark signal at -40°C	200 e^-/pixel/second

Quoted performance parameters given here are “typical” values. Specification limits are shown later.

Teledyne e2v (UK) Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne e2v (UK) Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact Teledyne e2v by e-mail: Enquiries@Teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

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PERFORMANCE (note 1)

	Min	Typical	Max	Units	Note
Full-well capacity	3M	4M	-	e^-/pixel	2
Output amplifier responsivity	0.40	0.70	0.85	µV/e^-	3
Read-out noise	-	100	200	e^- rms	4
Amplifier non-linearity		0.7	1.0	%	
Amplifier-amplifier cross-talk adjacent outputs non-adjacent outputs		 0.1 0.01	 0.2 0.1	 % %	5
Maximum read-out frequency	-	5.2	5.4	MHz	6
Maximum frame rate		50	60	Hz	
Spectral range - X-ray (> 5% QE)	700	-	15k	eV	7
Spectral range – optical (> 5% QE)	450		1050	nm	7
Charge transfer efficiency: parallel serial	 99.9990 99.9990	 99.9999 99.9993	 100 100	 % %	8
Dark signal (-40°C)	-	200	1000	e^-/pixel/s	9
Dark signal non-uniformity (-40°C)		50	100	e^-/pixel/s	9
Operating temperature range	-100	-40	30	°C	

NOTES

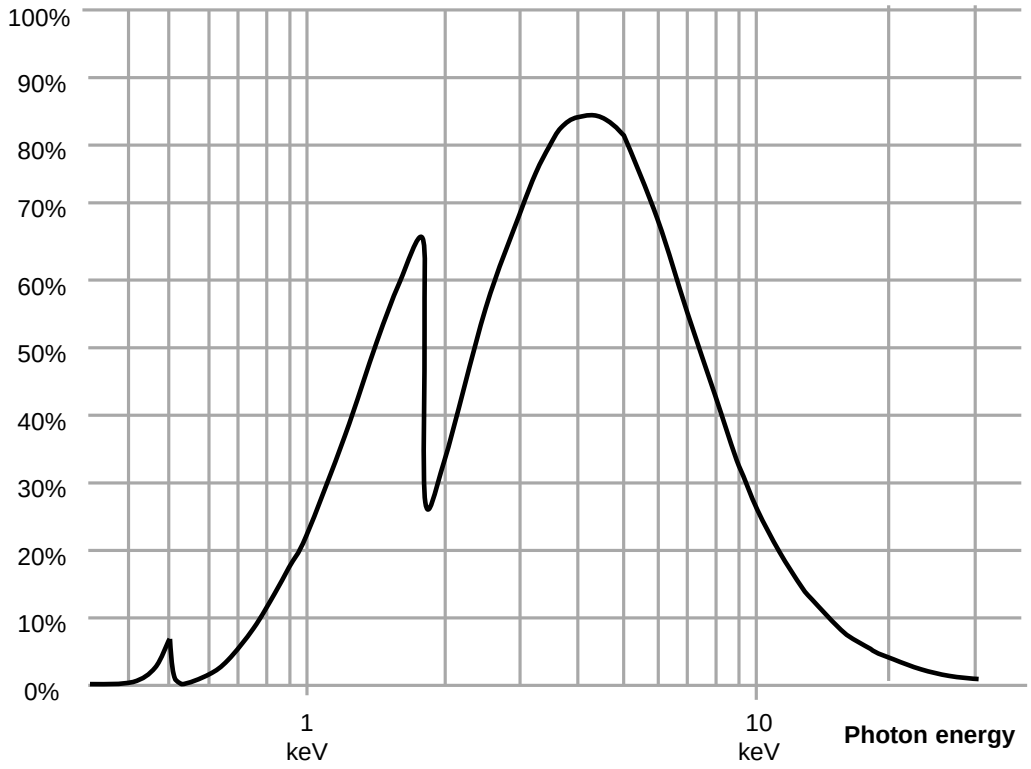
1. Device performance will be within the limits specified by “max” or “min”, as appropriate, when operated at the recommended voltages supplied with the test data. The test system uses a line transfer time of 3.2 µs, a read-out frequency of 5.2 MHz and with the device at -40°C.
2. Signal level at which the charge spilling indicates that the charge transfer efficiency has dropped to 99.999%.
3. The output node charge handling capacity is typically 4M e^-.
4. For measurements at 5.2 MHz read-out rate using correlated double sampling with the test system noise subtracted.
5. All outputs having parasitic capacitance C_L ~15 pF.
6. For 16.6 ms frame read-out time, but as largely set by the output settling time of the amplifier, see note 14. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.
7. Typical spectral response curves are shown on the next page. Note that in the case of X-ray imaging the mean number of electrons generated per interacting photon of energy E eV is E/3.65 and the standard deviation is given by $\sqrt{}$(FE/3.65), where F ~ 0.112 is the Fano factor.
8. The CTE value is quoted for the complete clock cycle (i.e. both phases).
9. The dark signal is a strong function of temperature and the typical average (background) dark signal N_D at any temperature T (Kelvin) between 173 K and 303 K is given by

   $N_D/N_{DO} = 122 \times T^3 e^{-6400/T}$

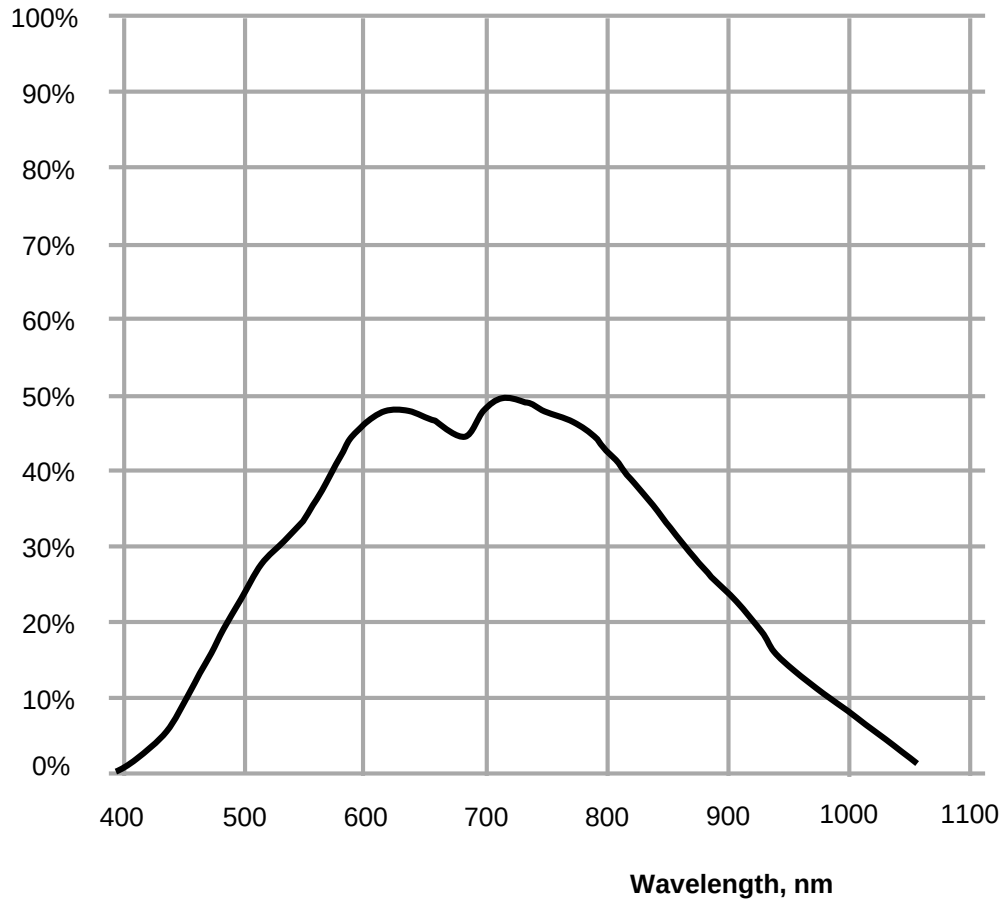
   where N_{DO} is the dark signal at 293 K (20°C). The typical value quoted above corresponds to about 1 nA/cm² at 20°C.

   Note that the dark signal and its non-uniformity will increase with exposure to ionising radiation, e.g. X-rays, as described in a later section.

Typical X-ray Quantum Efficiency



Typical Optical Quantum Efficiency



COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

Grade		0	1	2
Column defects	Black			24
	White			8
White spots				400
Black spots				800
Traps > 200e^-				48

Grade 2 is the highest currently available.

Lower grade devices may be available for set-up purposes and are designated **Grade 5**. These are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is 125 times the specified maximum dark signal generation rate at 293K. The typical temperature dependence of white spot defects is given by $N_D/N_{DO} = 122T^3e^{-6400/T}$
Black spots	A black spot defect is a pixel with less than 90% of the local mean at a signal level of approximately half full well.
Column defects	A column is counted as a defect if it contains at least 21 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^- at -40°C.

DEFINITIONS

Dummy Output

Each “real” output has an associated “dummy” circuit on-chip, which is of identical design but receives no signal charge. The dummy output should have the same levels of clock feed-through and crosstalk from adjacent outputs, and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier in the external electronics. The penalty is that the noise is increased by a factor of √2. If not required the dummy outputs may be powered down by connecting the DOS pin to its corresponding OD pin with no load resistor being present.

Read-out Noise

Read-out noise is the random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves determining the standard deviation of the output fluctuations using the pre-scan elements, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dark Signal

This is the output signal of the device with zero illumination, typically consisting of electrons thermally generated within the semiconductor material and accumulated during signal integration. The dark signal and its non-uniformity is a strong function of temperature, as described in note 9.

Correlated Double Sampling

This is a technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency (CTE)

The charge transfer efficiency (CTE) is the fraction of the charge stored in a CCD element that is correctly transferred to the adjacent element by a single clock cycle. The charge not transferred remains held in the original element, most probably in trapping states, and may possibly be released at a later time. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

Inverted Mode Operation (IMO)

An inverted mode CCD has an additional implant that allows charge integration to be carried out with all phases at clock low. With an appropriate positive voltage applied to the substrate, the whole of the device is flooded with holes (termed ‘inverted’ or ‘pinned’), which suppresses the surface component of dark signal. This leaves only the much lower bulk component, reducing the overall dark signal by a factor of approximately 100.

Inverted mode operation is also referred to as multi-phase pinning (MPP).

The CCD262 is operated in normal or non-inverted mode with the substrate at 0V and charge collection with an image clock at high level V_{PH}. This is necessary for fastest possible clocking and maximum full-well capacity, and where the higher surface component of dark current can be tolerated.

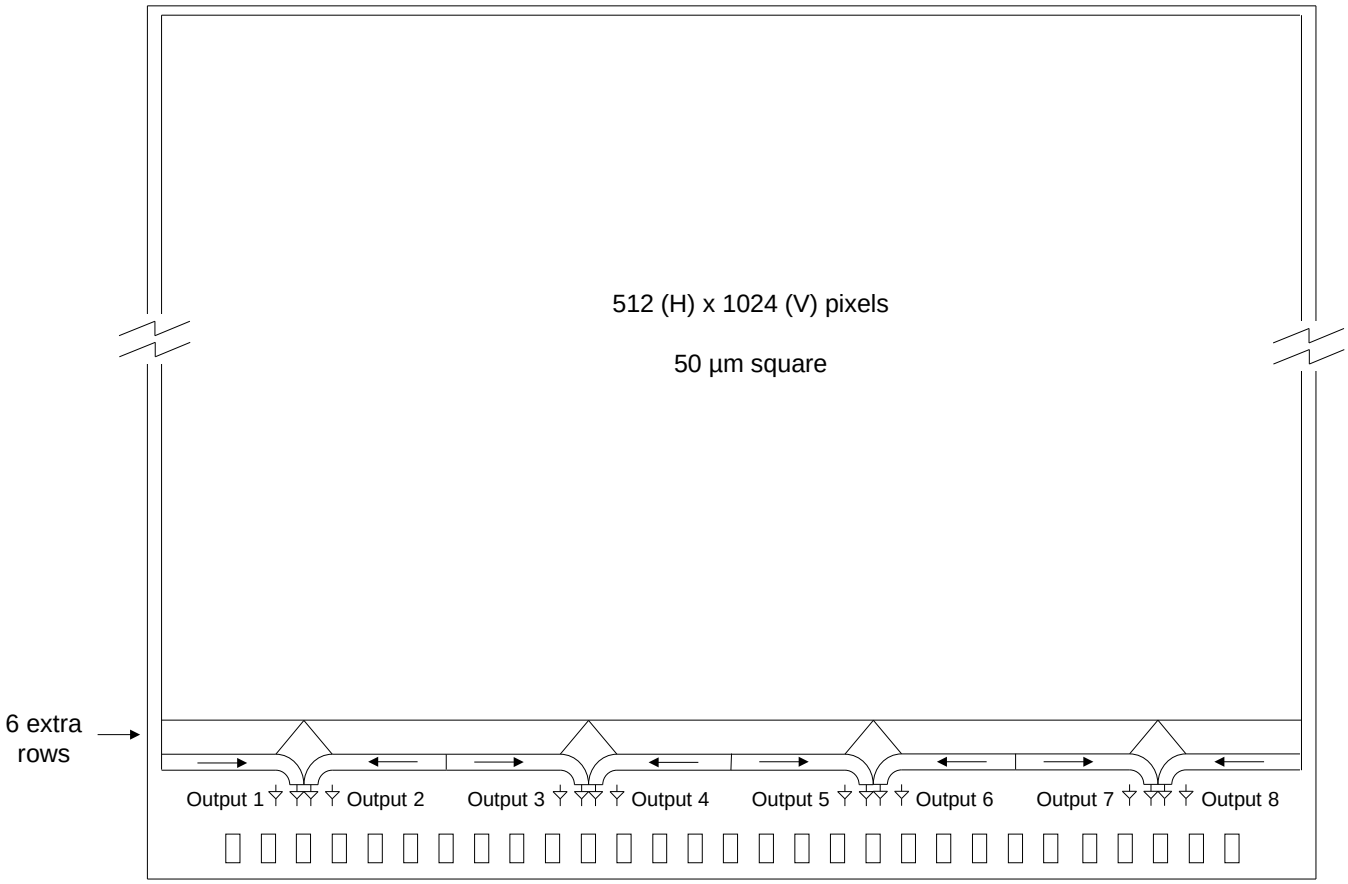
Illumination options

Some device types (such as the CCD262) have the illumination incident on the front-face and the radiation has to pass through the electrode structure – these devices are designated “front-illuminated”.

Some device types have the silicon reduced in thickness and the back surface treated to allow illumination incident on the back surface. The radiation now passes directly into the active silicon and a higher response is obtained – these devices are designated “back-illuminated”.

ARCHITECTURE

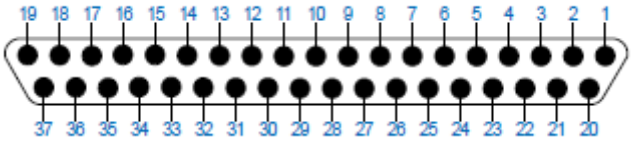
Chip Schematic



Not to scale

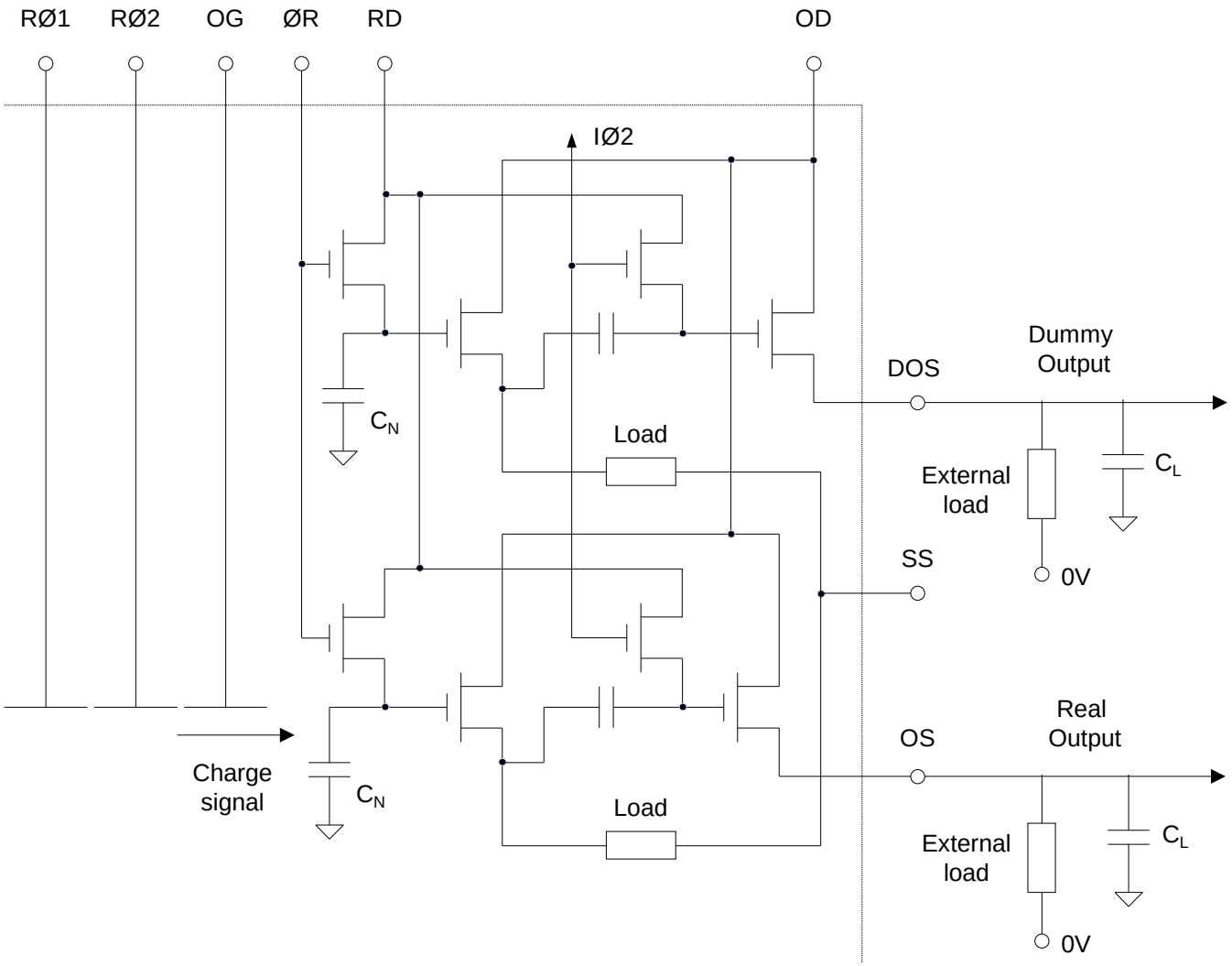
There are an additional 6 rows of non-shielded parallel transfer elements between the pixels and the read-out register. These are of slanted layout and not used for imaging purposes. Charge signals collected in these rows should therefore be dumped on frame read-out. Each register section has 64 elements with 4 pre-scan elements before the read-out circuitry.

PACKAGE CONNECTIONS



Micro-D, viewed facing connections

OUTPUT CIRCUIT



NOTES

10. The DC restoration circuitry requires a pulse at the start of line read-out, and this is automatically obtained by an internal connection to the IØ2 image clock.
11. The output load is not critical, but can be a 5 mA constant current supply or an equivalent resistor of 5k ohms connected to ground (0V). With the reset drain at 20V, the quiescent voltage on OS and DOS is typically within 22±1V.
12. The output impedance is typically 250 Ω.
13. The on-chip dissipation is typically 50 mW per amplifier, or 100 mW per real and dummy pair.
14. The maximum frequency of operation is largely set by the output settling performance, which is related to the parasitic capacitance C_L shunting the load. With $C_L \leq 15$ pF the output settles to 0.33% of the final value in a time of about 45 ns, which should leave sufficiently wide reset and signal sampling windows (as shown in the detail of output clocking) for operation at frequencies up to at least 5.4 MHz. This maximum speed will however reduce if the value for C_L increases above 15 pF.
15. Note that care should be taken in making the external connections for OD and 0V to the various amplifiers as common impedance will increase the cross-talk.

CONNECTIONS, OPERATING VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

The table below gives the pin connections, clock amplitudes, dc bias levels and maximum ratings. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications, which may differ from device to device.

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 16)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	TS1	Temperature sensor 1 (see note 17)				-
2	ID	Input drain (see note 19)	18	V_{OD}		-0.3 + 30 V
3	GD	Guard drain		V_{OD}		-0.3 + 30 V
4	OS1	Output source 1		See note 18		-0.3 + 30 V
5	OS2	Output source 2		See note 18		-0.3 + 30 V
6	DOS3	Dummy output source 3		See note 18		-0.3 + 30 V
7	OS4	Output source 4		See note 18		-0.3 + 30 V
8	DOS4	Dummy output source 4		See note 18		-0.3 + 30 V
9	IØ2	Image area drive pulse phase 2 ($V_{PH} – V_{PL}$)	9	11	12	± 20 V
10	RØ2	Register drive pulse phase 2 ($V_{RH} – V_{RL}$)	9	10	12	± 20 V
11	ØR	Output reset pulse ($V_{XH} – V_{XL}$)	9	10	12	± 20 V
12	OG	Output gates	1	2	3	± 20 V
13	DOS5	Dummy output source 5		See note 18		-0.3 + 30 V
14	RDR	Reset transistor drains	17	20	21	-0.3 + 30 V
15	DOS6	Dummy output source 6		See note 18		-0.3 + 30 V
16	OS7	Output source 7		See note 18		-0.3 + 30 V
17	OS8	Output source 8		See note 18		-0.3 + 30 V
18	GD	Guard drain		V_{OD}		-0.3 + 30 V
19	IG	Input gate (see note 19)	-10	0		± 20 V
20	TS2	Temperature sensor 2 (see note 17)				
21	SS	Substrate	0	0	0	-
22	DOS1	Dummy output source 1		See note 18		-0.3 + 30 V
23	OD12	Output drains, outputs 1 and 2		See note 18		-0.3 + 32 V
24	DOS2	Dummy output source 2		See note 18		-0.3 + 30 V
25	OS3	Output source 3		See note 18		-0.3 + 30 V
26	OD34	Output drains, outputs 3 and 4	28	29	30	-0.3 + 32 V
27	SS	Substrate	0	0	0	-
28	IØ1	Image area drive pulse phase 1 ($V_{PH} – V_{PL}$)	9	11	12	± 20 V
29	RØ1	Register drive pulse phase 1 ($V_{RH} – V_{RL}$)	9	10	12	± 20 V
30	SS	Substrate	0	0	0	
31	OD56	Output drains, outputs 5 and 6	28	29	30	-0.3 + 32 V
32	OS5	Output source 5		See note 18		-0.3 + 30 V
33	OS6	Output source 6		See note 18		-0.3 + 30 V
34	DOS7	Dummy output source 7		See note 18		-0.3 + 30 V
35	OD78	Output drains, outputs 7 and 8	28	29	30	-0.3 + 32 V
36	DOS8	Dummy output source 8		See note 18		-0.3 + 30 V
37	SS	Substrate	0	0	0	

NOTES

16. The low level of the drive pulses V_{PL}, V_{RL} and V_{XL} should be within 0 ± 0.5 V.

17. TS1000 Platinum resistance sensor. For details of operation please contact Teledyne e2v.

18. Connect load to ground (0V) as described in note 11. Maximum OS current is 20 mA.

19. The input drain and gate are used for certain test purposes but have no function in normal device operation and simply serve to isolate the top row of pixels from the peripheral structures.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. In particular, the voltage for the drain connections (OD, RD, GD and ID) must never be taken negative with respect to the substrate as damagingly high currents could then flow.

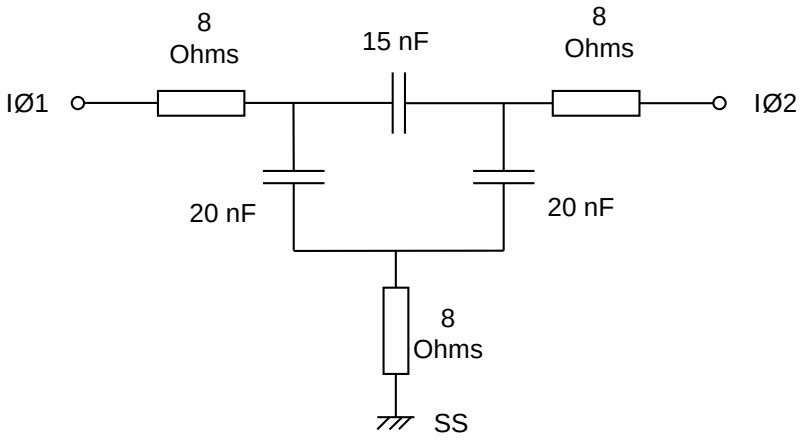
It is also important to ensure that excess currents do not flow in the OS pins (20 mA maximum). Such currents could arise from rapid charging of an external signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads). In the case of this device the amplifier dissipation dominates and is typically 800 mW.

ELECTRODE LOAD CAPACITANCES

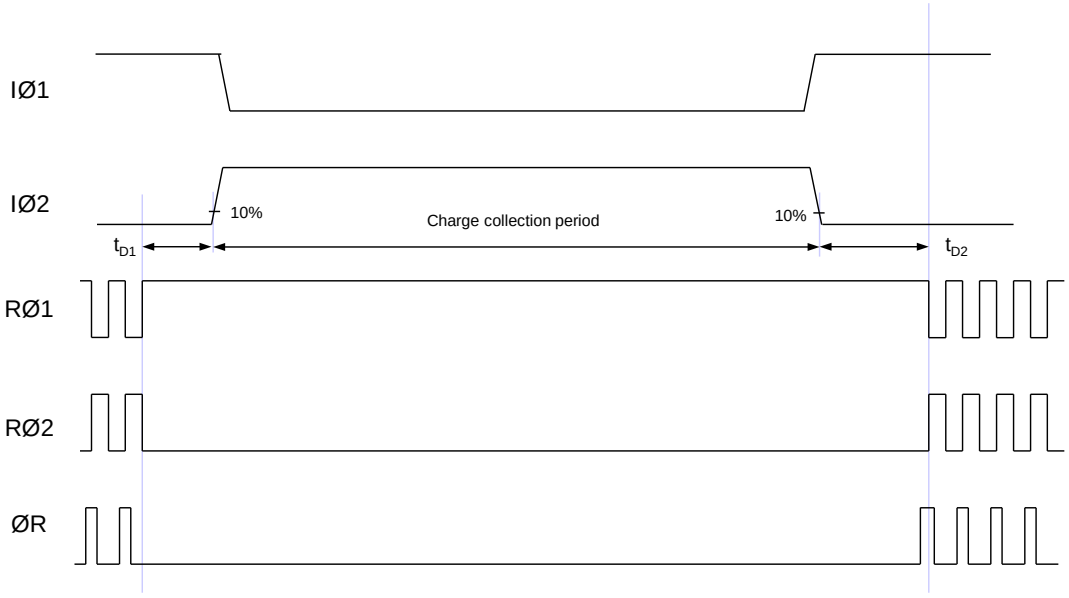
Image section, measured at mid-clock level



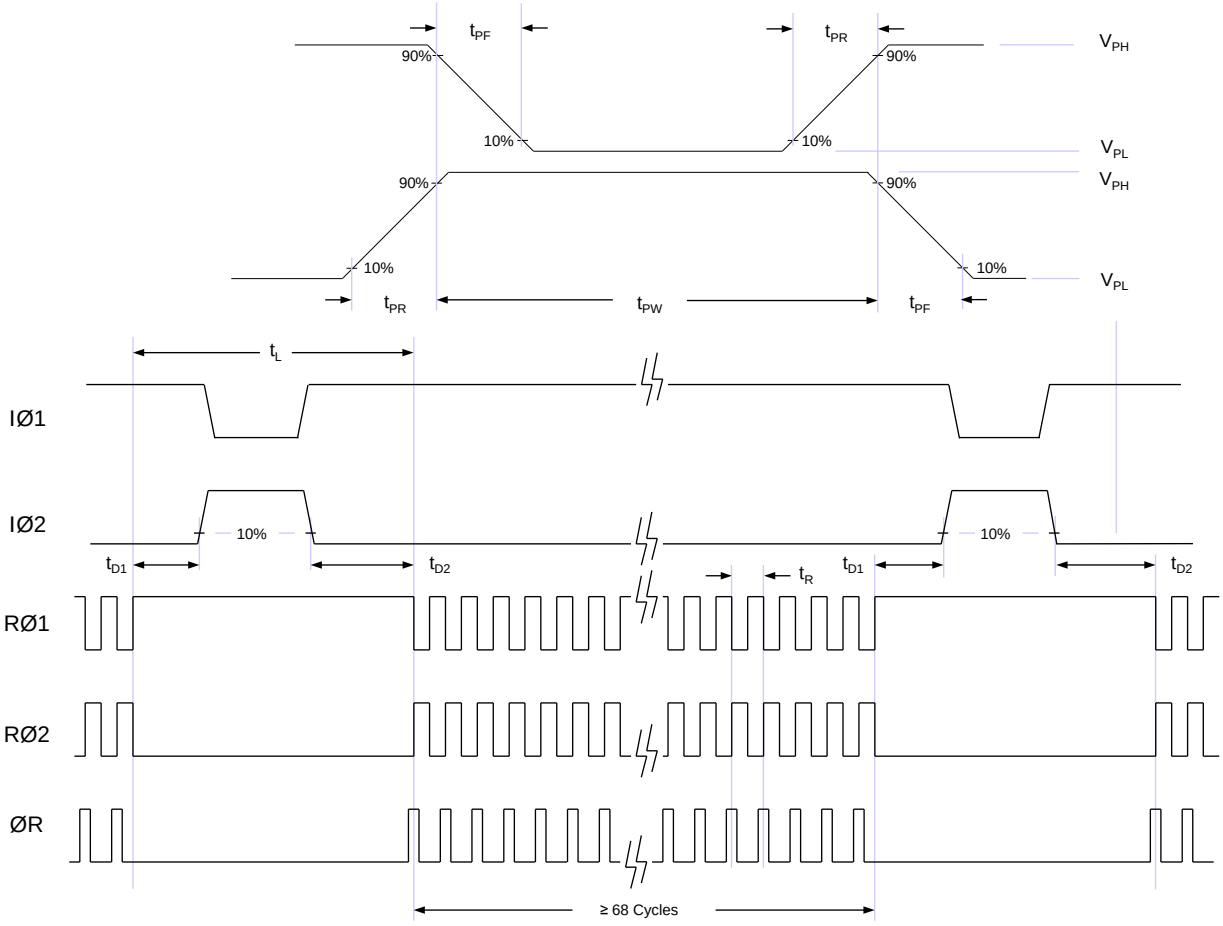
Register sections, measured at mid-clock level

Component	Typical
RØ1-SS	50 pF
RØ2-SS	80 pF
RØ1-RØ2	30 pF
ØR-SS	40 pF

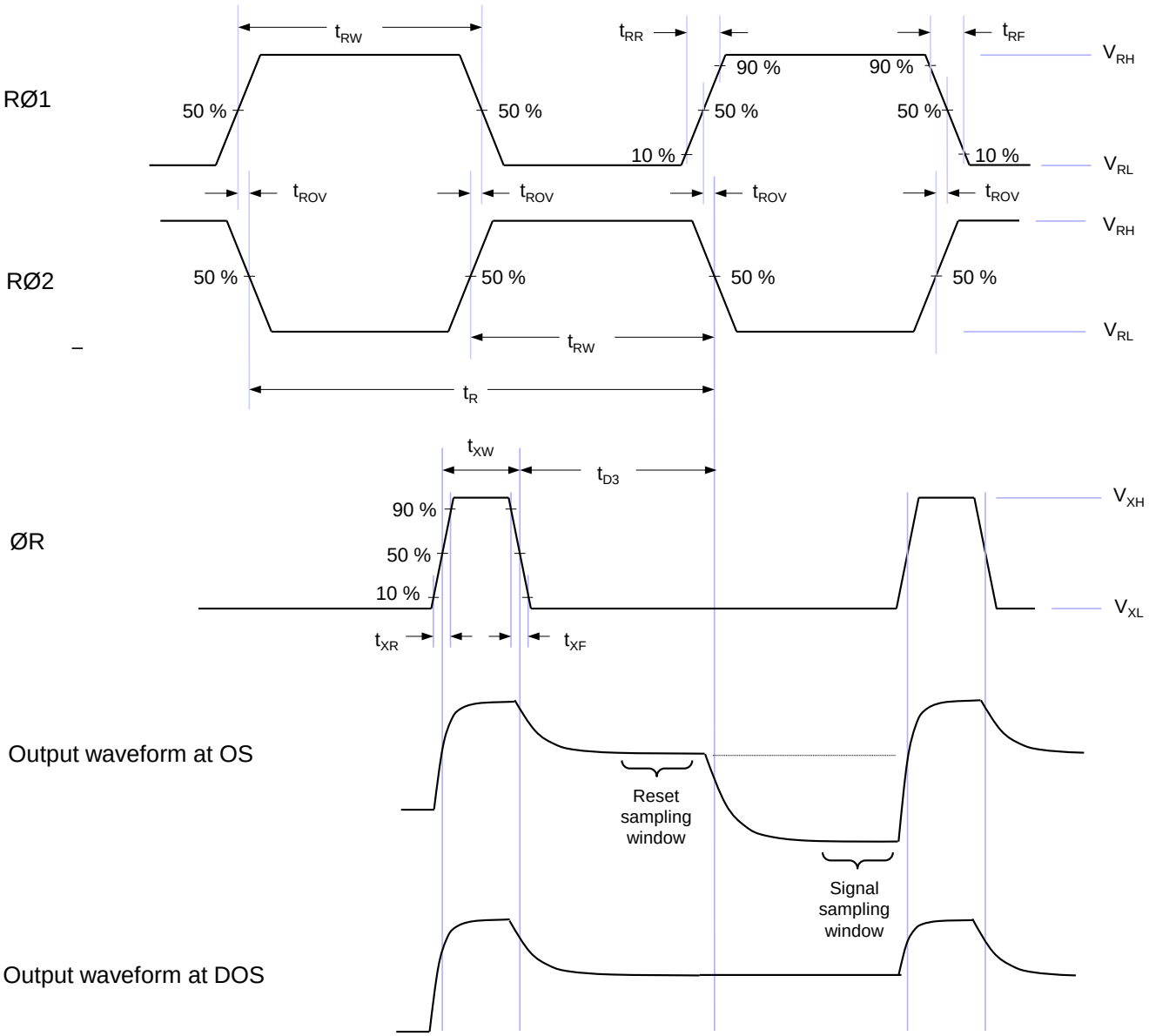
DETAIL OF CHARGE COLLECTION CLOCKING



DETAIL OF LINE TRANSFER CLOCKING



DETAIL OF OUTPUT CLOCKING



NOTES

20. Ideally the drive pulses should be of a trapezoidal shape with equal, well-defined rise and fall times.

21. The pulses are shown overlapping at nominally 50% amplitude as this results in minimal substrate disturbance as the charge/discharge currents are equal and opposite. Waveforms of a less-than-ideal shape may require increased amplitude and/or overlap.

CLOCK TIMING REQUIREMENTS

Timing information is given in the following table. The fact that many of the quantities are inter-related means that it is difficult to unambiguously specify individual minimum and maximum values. Thus, in determining a particular set of timing details for a given application, if there appear to be inconsistencies, then these should be resolvable with reference to the general principles outlined in the previous notes.

A maximum frame rate of 60 Hz can be possible using “minimum” values shown below. However, some critical adjustment of the image section clocking waveforms may be necessary to minimise t_L whilst still maintaining an acceptable full-well capacity. The register clocking and the performance of the output circuit (e.g. load capacitance) may also need critical adjustment to minimise t_R whilst giving a sufficiently well-sampled output for correlated sampling to be possible. The “typical” values shown below are for less -critical operation using a 5 MHz read-out rate to achieve a frame rate of about 50 Hz.

	Description	Minimum	Typical	Maximum
t_L	Line transfer time	3.2 µs	6.0 µs	
t_{PW}	Image section pulse width		$t_L/2$	
t_{PR}	Image section pulse rise time	200 ns	600 ns	0.3 t_{PW}
t_{PF}	Image section pulse fall time	200 ns	600 ns	0.3 t_{PW}
t_{D1}	Delay: register stop to image start	50 ns	100 ns	200 ns
t_{D2}	Delay: image stop to register start	800 ns	900 ns	$t_L/2 – t_{D1}$
t_R	Register clock period (see note 22)	185 ns	200 ns	
t_{RW}	Register pulse width		$t_R/2 + t_{ROV}$	
t_{RR}	Register pulse rise time	5 ns	10 ns	15 ns
t_{RF}	Register pulse fall time	5 ns	10 ns	15 ns
t_{ROV}	Register pulse overlap	-2 ns	0 ns	5 ns
t_{XW}	Reset pulse width	30 ns	40 ns	50 ns
t_{XR}	Reset pulse rise time	5 ns	10 ns	15 ns
t_{XF}	Reset pulse fall time	5 ns	10 ns	15 ns
t_{D3}	Delay: reset falling to RØ2 falling (see note 23)		$(t_R – t_{XW})/2$	
t_F	Frame read-out period (see note 24)	16.6	20.0	ms

Notes

22. The minimum register period is largely set by the degree of signal settling required from the output circuit.

23. t_{D3} can be adjusted to equalise the reset and signal sampling periods.

24. The total frame read-out period is nominally $1030[t_L + 68t_R]$.

EFFECTS OF RADIATION

Ionising radiation, essentially photons with energy E >10 eV, i.e. X-rays; also alpha, beta and gamma rays and high energy charged particles, e.g. protons, causes changes to certain device characteristics.

A first change is a build-up of positive charge in the gate dielectric. This is quantified in terms of a “flat-band voltage shift”, ΔV_{FB}, which is the change of threshold voltage that would be measured in an MOS transistor using the same dielectric. In the case of a CCD electrode, the maximum channel potential in the underlying silicon increases by this amount. With uniform irradiation the channel potentials under the CCD electrodes will shift by nominally the same amount, so the normal charge collection and transfer is unaffected. Correct operation of the output circuit does however require a defined potential difference between the channel potential under the output gate and the reset drain voltage, with the result that the reset drain voltage needs to be increased by ΔV_{FB} to maintain correct operation. Since the shift is also present in the output transistors, the output drain needs to be increased by $2\Delta V_{FB}$.

In practice the read-out sections can be shielded from the radiation, e.g. using a metal mask above the device (but take great care not to touch the surface as this can result in irreparable damage). The radiation dose experienced by the device then tends to tail off towards the output and the adjustment of drain voltage may not be required.

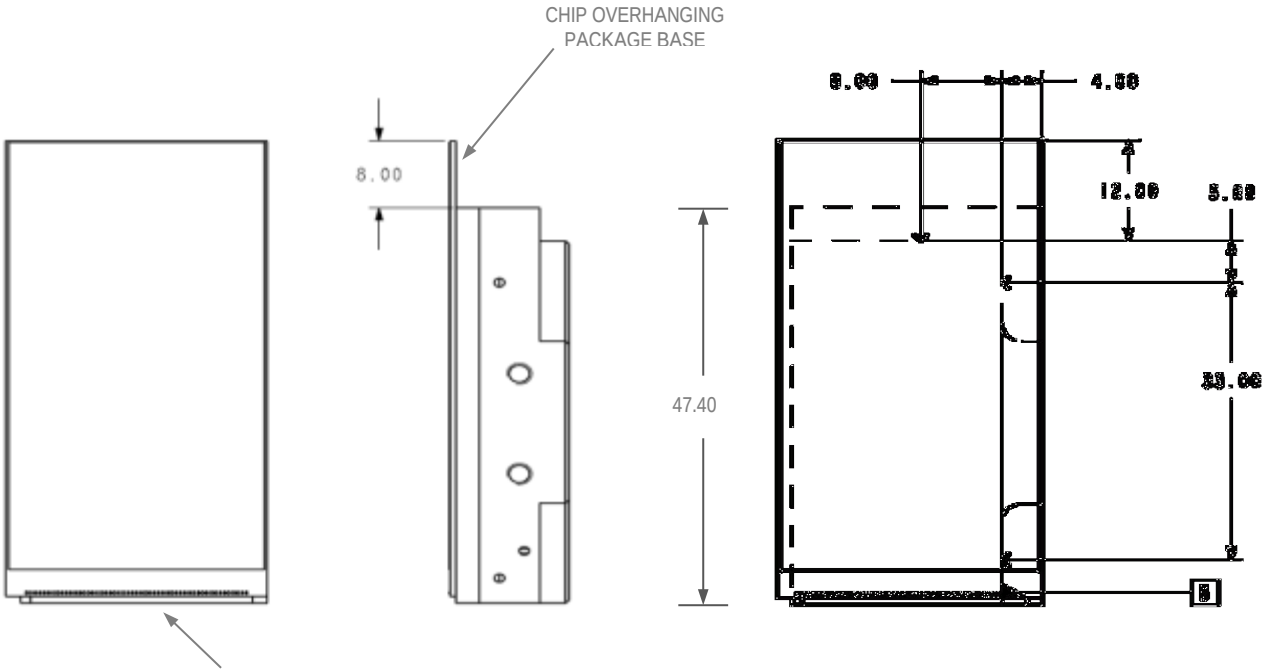
A second change is an increase in the dark current. The non-uniformity of dark current will therefore increase if regions of the image section experience a considerably higher dose than elsewhere in the section. The corresponding localised change of channel potential can also cause loss of full-well capacity and, if sufficiently large, there can be no charge transfer through the affected area.

Actual values of the changes are dependent on the fabrication process used for device manufacture. For these devices steps have been taken to minimise the changes, i.e. ‘radiation hardening’. Recent work has shown that the changes tend to saturate at higher total doses and typical values are as follows, where D is the dose in Mrad(Si):

	Lower doses < 100 kRad(Si)	Higher doses > 100 kRad(Si)
Flat-band voltage shift	~ 10 mV per kRad(Si)	Total shift ~ $\log_e[150D]$ volts
Dark current increase at 20°C	~ 30 pA/cm² per kRad(Si)	Total increase ~ $3[D/0.1]^{0.8}$ nA/cm²

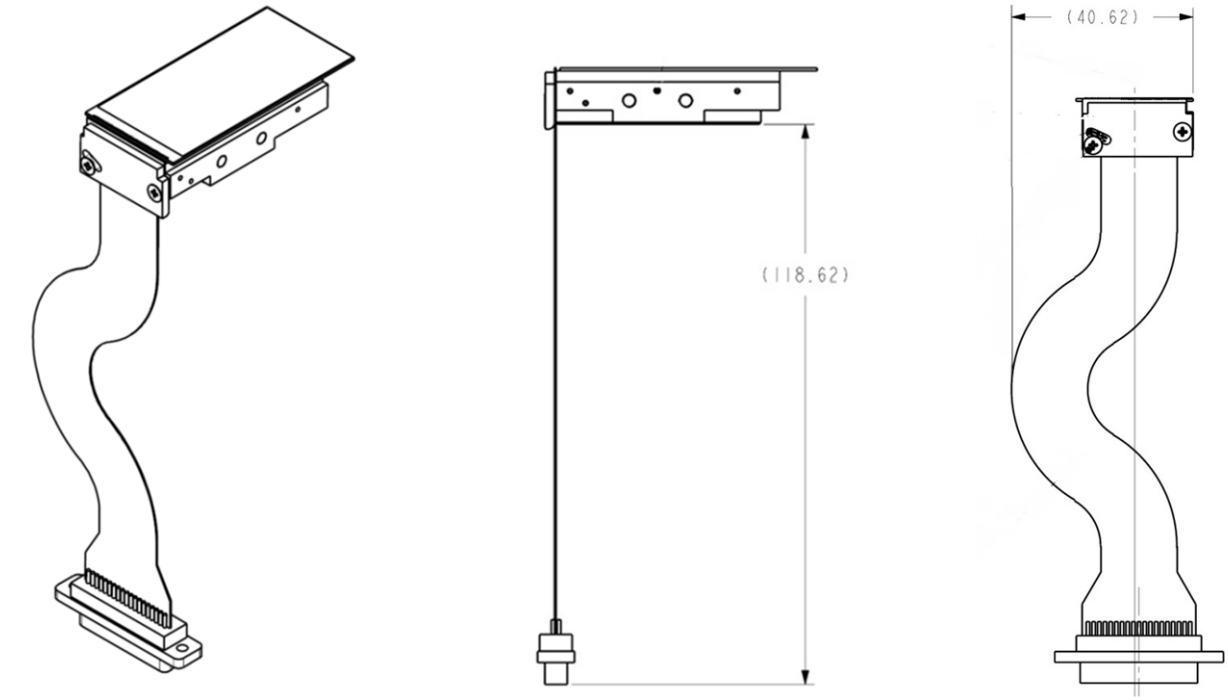
The maximum survivable dose will be set by either the output circuit voltages needing to be raised to unrealistically high values (if not shielded) or the dark signal non-uniformity becoming excessive.

PACKAGE DETAIL



VIEW FROM TOP OF CCD SHOWING POSITION OF POINTS OF CONTACT FOR THE ALIGNMENT PINS AGAINST THE PACKAGE.
e2v RECOMMENDS ALIGNMENT PINS ø3.00 x 2.94±0.05 TALL.

FLEXI-CONNECTOR DETAIL



HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully-grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment, and Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

TEMPERATURE RANGE

Operating temperature range 233 - 303 K

Storage temperature range 143 - 373 K

Full performance is only guaranteed at the nominal operating temperature of 233 K.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.