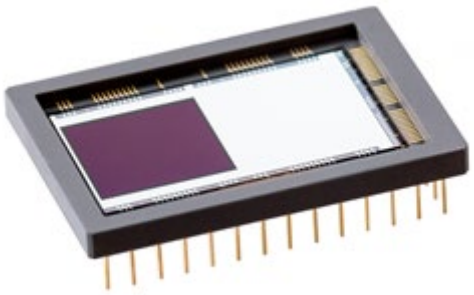
CCD201-20 Datasheet
Electron Multiplying CCD Sensor
Back Illuminated, 1024 x 1024 Pixels
2-Phase IMO

MAIN FEATURES

- 1024 x 1024 active pixels
- 13µm square pixels
- Variable multiplication gain
- Additional conventional output amplifier
- Inverted mode operation for low dark current.
- 36-pin ceramic package



OVERVIEW

The CCD201-20 is a frame transfer, electron multiplying CCD sensor designed for extreme performance in high frame rate ultra-low light applications. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by the Large Signal Output amplifier (OSL).

The device can also be read out without using the gain register via the High Responsivity Output amplifier (OSH).

The multiplication gain in the readout chain allows L3Vision devices to effectively eliminate readout noise. The gain may be varied from 1x to over 1000x by adjustment of the multiplication phase amplitude RØ2HV.

GENERAL DATA

Image section	1024 x 1024
Pixel size	13 µm × 13 µm
Active image area	13.3 mm × 13.3 mm
Package size	37.4 mm × 26.5 mm
Typical amplifier responsivity	5.3 µV/e^- (OSH) 1.4 µV/e^- (OSL)
Typical readout noise 1MHz at 1000x Gain 50kHz using OSH amp.	 <1e^- 3.1e^-
Max output data rate	20 MHz
Typical pixel charge capacity	80 ke^-/pixel
Typical dark signal (20°C)	260 e^-/pixel/s

ORDERING INFORMATION

CCD201-20-G-XYZ
G = cosmetic grade
XYZ= specific variant type (e.g. AR coating)
e.g. XYZ = 122 for basic process with midband coating
e.g. XYZ = S29 for no OSH amplifier variant.

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IMAGING PERFORMANCE

ELECTRO-OPTICAL PERFORMANCE

Except where otherwise specified, the following are measured at 18°C at a pixel rate of 15 MHz, with typical operating voltages. For the S29 variant, the parameters relating to the OSH amplifier do not apply; all other parameters are unchanged.

Parameters	Min	Typical	Max	Units	Notes
Output amplifier responsivity, OSH amplifier	-	5.3	-	µV/e⁻	Note 1
Output amplifier responsivity, OSL amplifier	-	1.4	-	µV/e⁻	Note 1, Note 2
Multiplication register gain, OSL amplifier	1	-	1000		Note 3
Peak signal - 2-phase IMO	65k	80k	-	e⁻/pixel	
Charge handling capacity of multiplication register	-	730k	-	e⁻/pixel	Note 4
Charge handling capacity of OSH amplifier	-	280k	-	e⁻	Note 5
Charge handling capacity of OSL amplifier	-	1M	-	e⁻	Note 5
Readout noise at 50 kHz with CDS, OSH amplifier	-	3.1	-	e⁻ rms	Note 5
Readout noise at 1 MHz with CDS, OSH amplifier	-	6.0	-	e⁻ rms	Note 5
Amplifier reset noise (without CDS), OSH amplifier	-	50	-	e⁻ rms	Note 5
Readout noise at 15 MHz with CDS, OSL amplifier	-	43	-	e⁻ rms	Note 2, Note 5
Amplifier reset noise (without CDS), OSL amplifier	-	100	-	e⁻ rms	Note 2, Note 5
Readout noise at 1 MHz (1000x gain)	-	<1	-	e⁻ rms	Note 5
Maximum frequency (settling to 1%), OSH amplifier	-	-	3	MHz	Note 5, Note 6
Maximum frequency (settling to 5%), OSH amplifier	-	-	4.5	MHz	Note 5, Note 6
Maximum frequency (settling to 1%), OSL amplifier	-	-	13	MHz	Note 5, Note 6
Maximum frequency (settling to 5%), OSL amplifier	-	-	20	MHz	Note 5, Note 6
Maximum parallel transfer frequency	-	0.9	-	MHz	Note 1
Dark signal equivalent at 20°C	-	260	530	e⁻/pixel/s	Note 7, Note 8
Dark signal non-uniformity (DSNU) equivalent at 20°C	-	90	-	e⁻/pixel/s	Note 9
Excess noise factor	-	√2	-		Note 10

Notes

Note 1. Measured at a pixel rate of 1 MHz.

Note 2. No EM gain applied.

Note 3. Some increase of RØ2HV may be required throughout life to maintain gain performance.

Note 4. When multiplication gain is used, a linear response is achieved for output signals up to 400 ke⁻.

Note 5. These values are inferred by design and not measured.

Note 6. The quoted maximum frequencies assume a 20 pF load and correlated double sampling (CDS) are being implemented. If instead a single sampling is used, the output will be settled to 1% at 20 MHz typically..

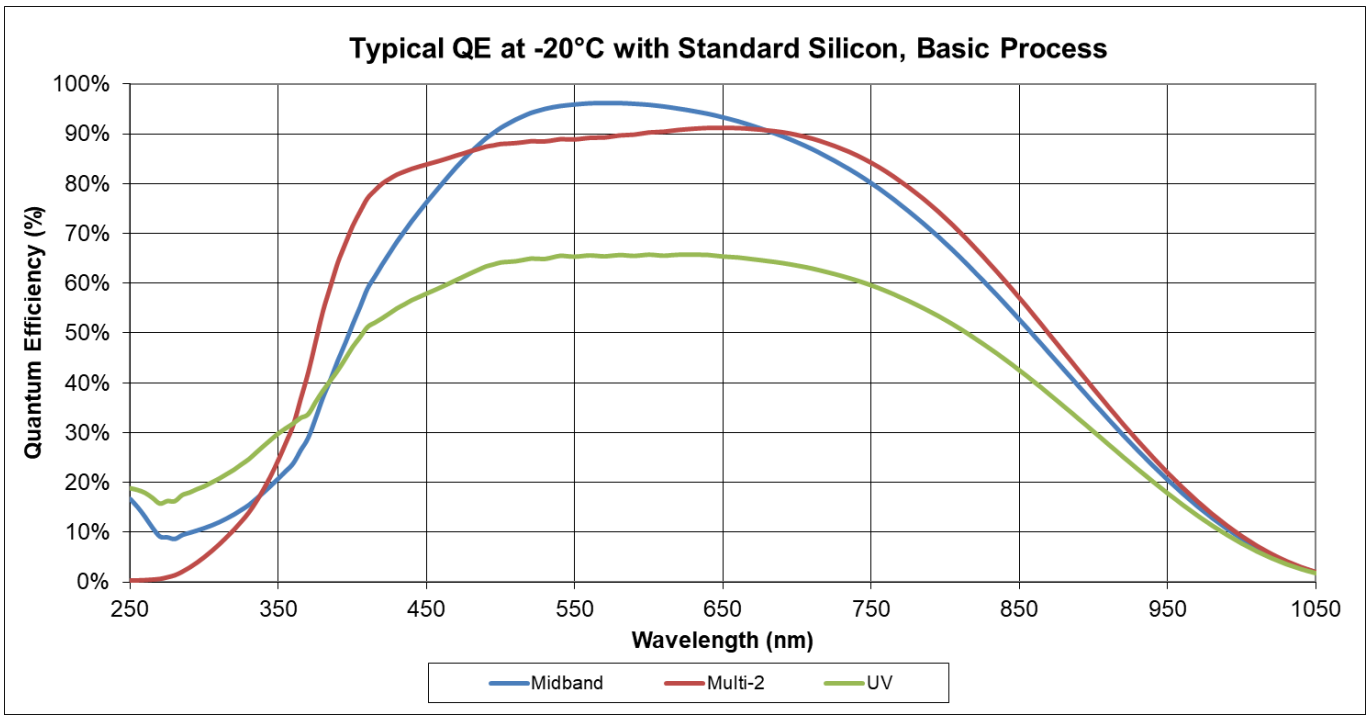
Note 7. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a component generated during readout through the register.
There exists a further weakly temperature dependent component, the clock induced charge (CIC), which is independent of the integration time. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".

Note 8. For fringe suppression variants, the dark signal will be higher (typical and maximum are 400 and 600 e⁻/pixel/s respectively).

Note 9. DSNU is defined as the 1σ variation of the dark signal.

Note 10. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

FIGURE 1: TYPICAL SPECTRAL RESPONSE (Not measured)



Devices can be supplied with alternative anti-reflection coatings optimised for different wavelengths – details from Teledyne e2v.

FIGURE 2: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH RØ2HV

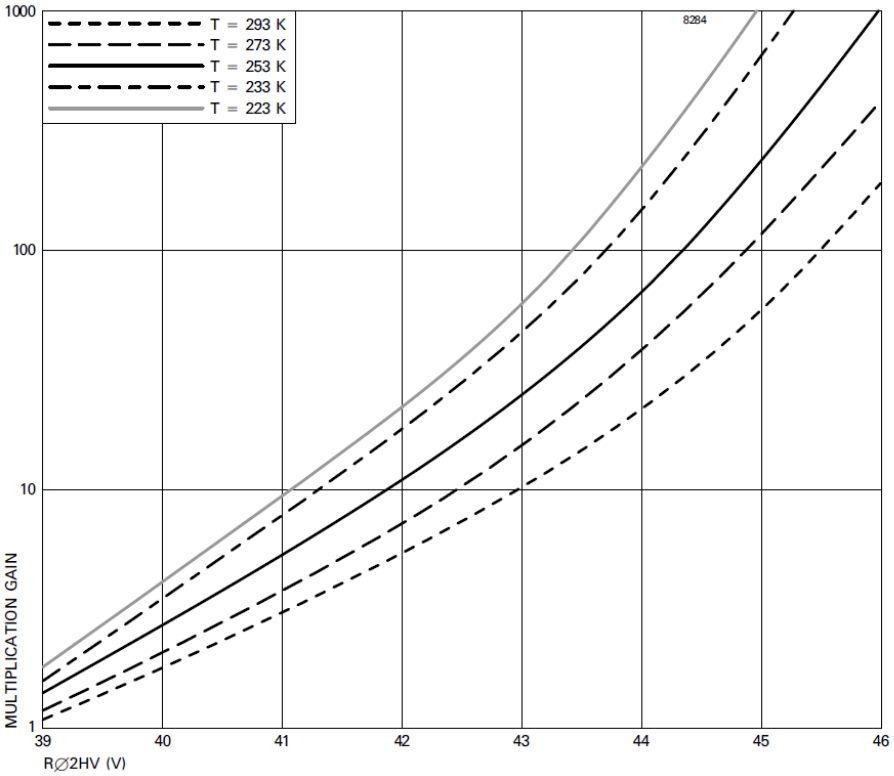
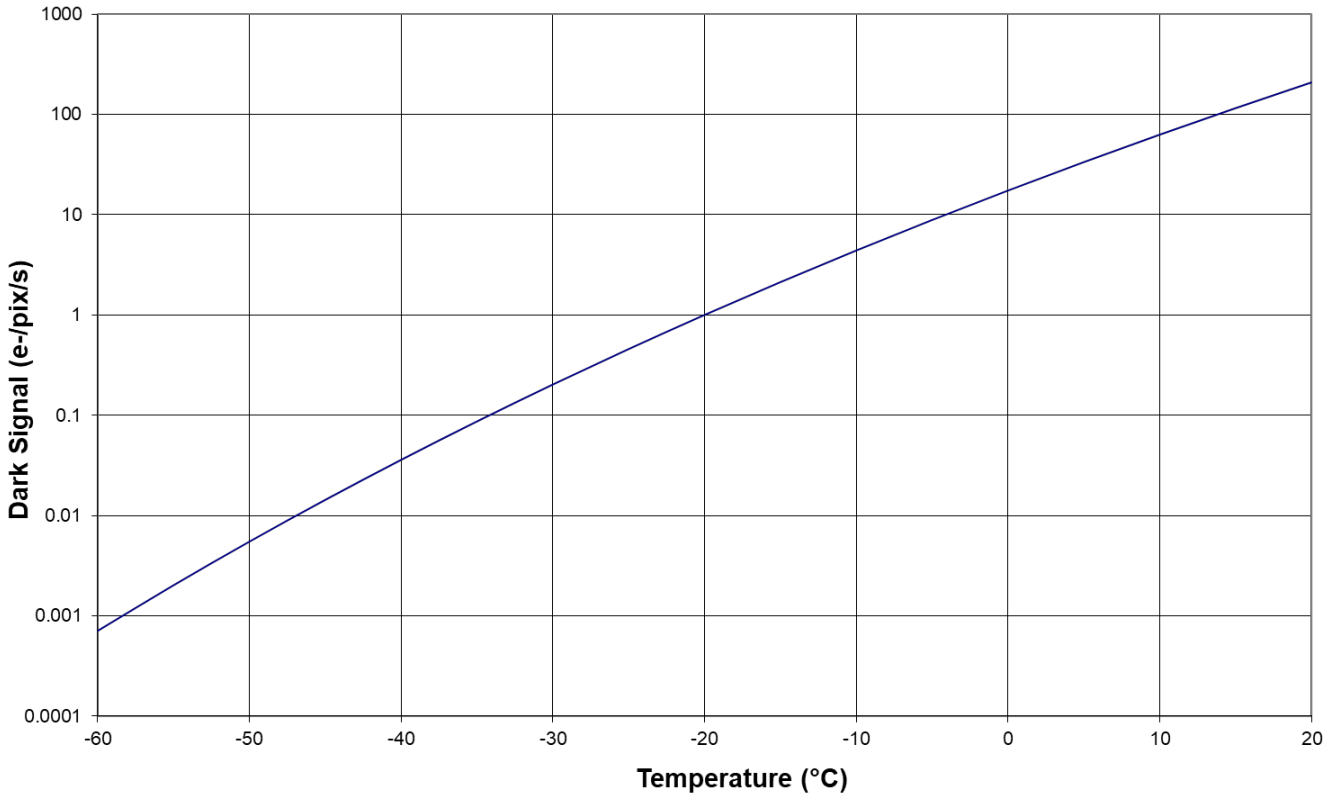


FIGURE 3: TYPICAL VARIATION OF IMO DARK SIGNAL WITH TEMPERATURE (Not measured)

Dark signal is a strong function of temperature and the typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by $Q_d/Q_{do} = 1.14 \times 10^6 T^3 e^{-9080/T}$ where Q_{do} is the dark current at 293K.



DEFECT DEFINITIONS

All cosmetic tests are performed at 18 ± 3ºC in 2-phase inverted mode with a readout rate of 15MHz.

SPECIFICATION

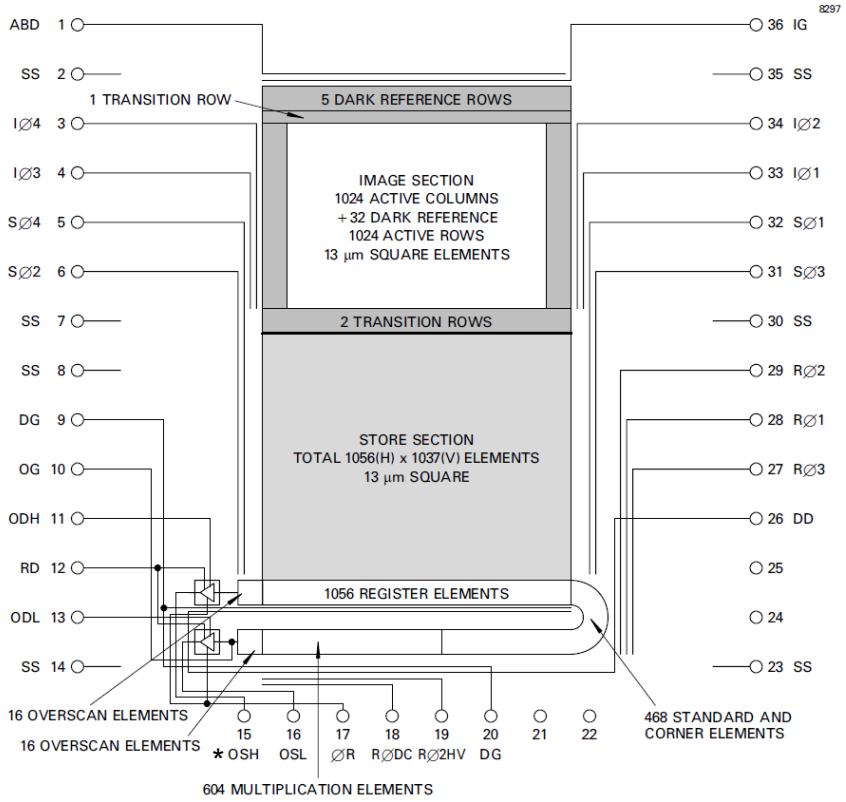
Parameter	Grade 1	Definition
White Defects	24	White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum dark signal level.
White Columns	0	A white column contains at least 9 white defects.
Black/Pin-head Columns	1	Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified gain and level of illumination. A black column contains at least 9 black defects. Pin-head columns are manifest as a partial dark column with a bright pixel showing photo-response at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

Grade 5 devices are fully functional but with an image quality below grade 1. Other specifications may also not be met or may not have been tested.

Incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

DEVICE DESCRIPTION

FIGURE 4: DEVICE ARCHITECTURE



* Pin 15 has no connection for S29 variant

The rows and colums immediately adjacent to the active image area may be only partially shielded, i.e. transition elements, and should not be used for reference purposes.

The electrodes of the image and store sections are configured for four-phase clocking, but adjacent phases need to be joined off chip to run in two phase operation.

The multiplication register requires two extra drive phases, RØDC and RØ2HV.

There is a dump drain DD below the 1056 register elements adjacent to the store section with the charge dumping operation controlled by the dump gate DG.

FIGURE 5: LINE OUTPUT FORMAT (OSH amplifier)

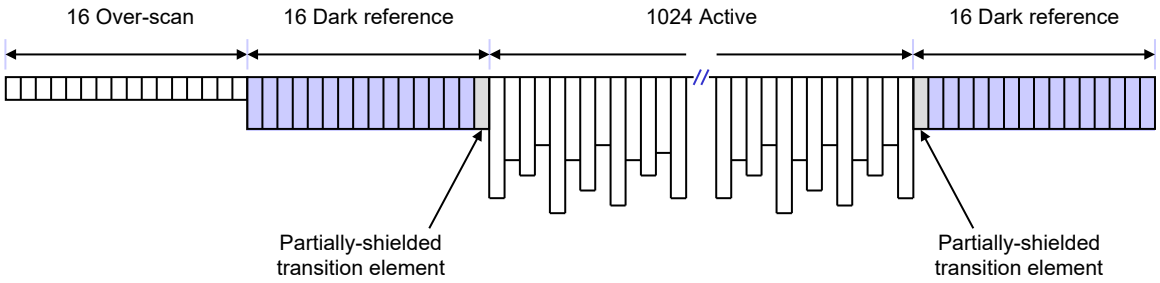
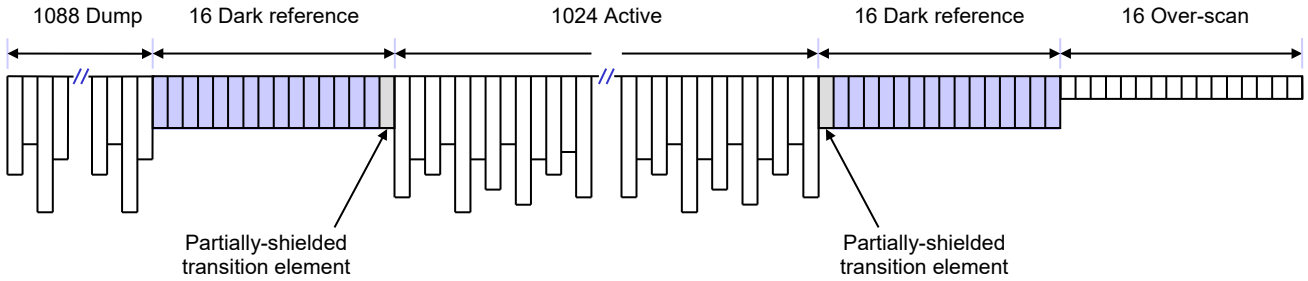


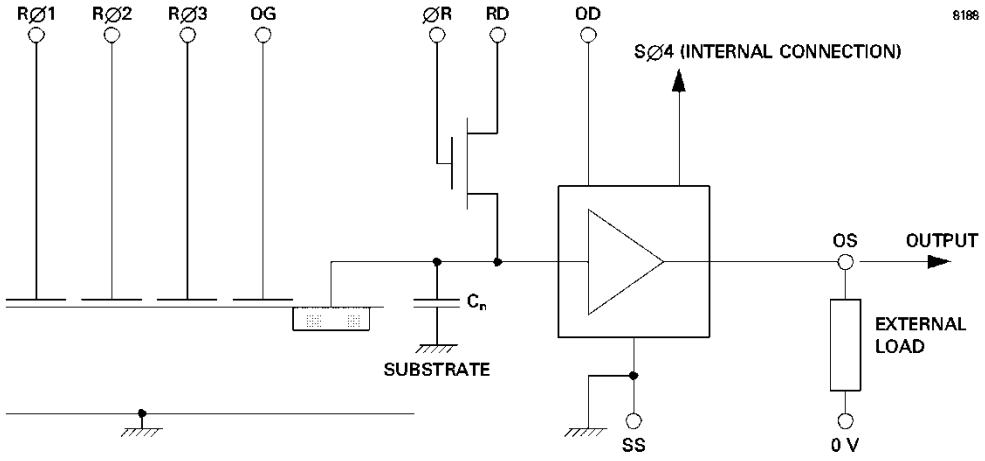
FIGURE 6: LINE OUTPUT FORMAT (OSL amplifier)



Notes

Note 11. There is a 1-line propagation delay between transferring a line from the store section to the standard register and reading it out through the OSL output amplifier.

FIGURE 7: OUTPUT CIRCUIT



The amplifiers have a DC restoration circuit that is internally activated whenever SØ4 is high.

Nominal Design Features (Not measured)

Feature	OSH	OSL
Output	OSH (pin 15)	OSL (pin 16)
External load	5 kΩ or 5 mA	3.3 kΩ or 7.5 mA
Output impedance	400 Ω	350 Ω
On-chip dissipation	30 mW	50 mW

ELECTRICAL PERFORMANCE

PIN DESCRIPTIONS

The table below gives the pin connections, functions and maximum ratings with respect to the substrate (SS).

Pin	Ref	Function	MIN (V)	MAX (V)
1	ABD	Anti-blooming drain [Note 13]	-0.3	+25
2	SS	Substrate	0	
3	IØ4	Image Clock 4	-20	+20
4	IØ3	Image Clock 3	-20	+20
5	SØ4	Store Clock 4	-20	+20
6	SØ2	Store Clock 2	-20	+20
7	SS	Substrate	0	
8	SS	Substrate	0	
9	DG	Dump Gate	-20	+20
10	OG	Output Gate	-20	+20
11	ODH	Output Drain (OSH Amplifier)	-0.3	+32
12	RD	Reset Drain	-0.3	+25
13	ODL	Output Drain (OSL Amplifier)	-0.3	+32
14	SS	Substrate	0	
15	OSH	Output Source (OSH Amplifier) [Note 12, Note 14]	-0.3	+25
16	OSL	Output Source (OSL Amplifier) [Note 14]	-0.3	+25
17	ØR	Reset Pulse	-20	+20
18	RØDC	Multiplication Register DC Bias	-20	+20
19	RØ2HV	Multiplication Register Clock	-20	+50
20	DG	Dump Gate	-20	+20
21	n.c.	Not Connected	-	-
22	n.c.	Not Connected	-	-
23	SS	Substrate	0	
24	n.c.	Not Connected	-	-
25	n.c.	Not Connected	-	-
26	DD	Dump Drain	-0.3	+25
27	RØ3	Register Clock 3	-20	+20
28	RØ1	Register Clock 1	-20	+20
29	RØ2	Register Clock 2	-20	+20
30	SS	Substrate	0	
31	SØ3	Store Clock 3	-20	+20
32	SØ1	Store Clock 1	-20	+20
33	IØ1	Image Clock 1	-20	+20
34	IØ2	Image Clock 2	-20	+20
35	SS	Substrate	0	
36	IG	Isolation Gate	-20	+20

Notes

Note 12. OSH (pin 15) is not connected for the S29 variant

Note 13. The ABD pin is used for connection purposes and must be biased as specified even for non-anti-blooming variants.

Note 14. Permanent damage may result if, in operation, OSL and OSH experience short-circuit conditions.

Maximum Voltage Between Pairs

Pin	Ref	Pin	Ref	Min (V)	Max (V)
15	OSH	**11**	ODH	-15	+15
16	OSL	**13**	ODL	-15	+15
19	RØ2HV	**18**	RØDC	-20	+50
19	RØ2HV	**27**	RØ3	-20	+50
Output Transistor Current (mA)					20

OPERATING VOLTAGES

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

Connection	Description	Phase Amplitude or DC Level (V)			Notes
		Min	Typical	Max	
IØ1, 2, 3, 4 high	Image section: clock high	+5	+7	+9	Note 15
IØ1, 2, 3, 4 low	Image section: clock low	-6	-5	-4	
SØ1, 2, 3, 4 high	Store section: clock high	+5	+7	+9	Note 15
SØ1, 2, 3, 4 low	Store section: clock low	-6	-5	-4	
RØ1, 2, 3 high	Register: clock high	+8	+12	+13	
RØ1, 2, 3 low	Register: clock low	-	0	-	
RØ2HV high	Register HV phase high	+20	+40	+50	Note 3
RØHV low	Register HV phase low	0	+4	+5	
ØR high	Reset clock high	-	+10	-	Note 16
ØR low	Reset clock low	-	0	-	
RØDC	Register DC phase	+2	+3	+5	
OG	Output gate voltage	+1	+3	+5	Note 17
IG	Isolation gate voltage	-	-5	-	
SS	Substrate	0	+4.5	+7	Note 18
ODL, ODH	Output drain	+25	+28	+32	
RD	Reset drain voltage	+15	+17	+20	Note 17
ABD	Anti-blooming Drain	+10	+18	+20	
DG high	Dump gate high	-	0	-	
DG low	Dump gate low	+10	+12	+13	
DD	Dump drain	+20	+24	+25	

Notes

Note 15. IØ and SØ adjustment may be common. The high level may need to be adjusted to achieve correct charge transfer and the low level may need to be separately adjusted to achieve correct inverted mode operation that is uniform across the array.

Note 16. ØRL and ØRH high level may be adjusted in common with RØ1, 2, 3.

Note 17. Between the two amplifiers, common connections are made to the reset gates (ØR), reset drains (RD) and output gates (OG).

Note 18. The SS voltage may also need to be adjusted to achieve correct inverted-mode operation.

ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS					SERIES RESISTANCE	
Connection	To SS	Inter-phase	Total	Units		Units
IØ1 + IØ2	7.8	4.8	12.6	nF	8	Ω
IØ3 + IØ4	7.8	4.8	12.6	nF	8	Ω
SØ1 + SØ2	7.8	4.8	12.6	nF	8	Ω
SØ3 + SØ4	7.8	4.8	12.6	nF	8	Ω
RØ1	68	98	166	pF	6	Ω
RØ2	56	68	124	pF	6	Ω
RØ3	89	74	163	pF	6	Ω
RØ2HV	15	18	33	pF	8	Ω

TIMING

CLOCK TIMING REQUIREMENTS

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases ∅1 and ∅2, and phases ∅3 and ∅4 of the image and store sections. Suggested timing diagrams are shown in Figs. 8 - 13.

The following are suggested pulse rise and fall times.

Symbol	Description	Min	Typical	Max	Units	Notes
T_i	Line transfer time during FT (see note 20)	$2[t_{wi} - t_{oi}]$	1.5		µs	Note 19, Note 20
t_{wi}	Image/store clock pulse width	$3t_{oi}$	1		µs	Note 20
t_{oi}	Image/store clock pulse edge overlap	200	250		ns	Note 20
t_{ri}	Image/store clock pulse rise time (10 - 90%)		50	0.3 t_{oi}	ns	
t_{fi}	Image/store clock pulse fall time (10 - 90%)		50	0.3 t_{oi}	ns	
t_{D1}	Image/store clock delay time at start of FT	20	40		µs	Note 20
t_{D2}	Delay time, RØ stop to SØ rising	0.1	1		µs	Note 20
t_{D3}	Delay time, SØ falling to RØ start	0.3	1		µs	Note 20
t_{D4}	Delay time, RØ falling to DG falling	5	20		µs	Note 20
t_{D5}	Delay time, DG falling to RØ rising	5	20		µs	Note 20
T_{rr}	Register clock period (see note 20)		67		ns	Note 19, Note 20
t_{w1}	Register pulse width, RØ1 (at 50% levels)		$T_{rr}/2$			Note 20
t_{w2}	Register pulse width, RØ2 (at 50% levels)		$T_{rr}/4$			Note 20
t_{w3}	Register pulse width, RØ3 (at 50% levels)		$T_{rr}/4$			Note 20
t_{rr}	Register clock pulse rise time (10 - 90%)	5	10	$T_{rr}/5$	ns	
T_{fr}	Register clock pulse fall time (10 - 90%)	5	10	$T_{rr}/5$	ns	
t_{or}	Register clock pulse edge overlap (50% levels)	5	10	$T_{rr}/5$	ns	
t_{wx}	Reset pulse width (at 50% levels)	10	15	$T_{rr}/4$	ns	
t_{rx}	Reset pulse rise time (10 - 90%)	2	5	$T_{rr}/10$	ns	
t_{fx}	Reset pulse fall time (10 - 90%)	2	5	$T_{rr}/10$	ns	
t_{Dx}	Delay time, ØR falling to RØ2 falling (at 50%)	0	5	$t_{w2} - t_{wx}$	ns	

Notes

Note 19. As used for device testing at 15 MHz readout rate

Note 20. No maximum other than set by system constraints

Note 21. Total line transfer time for line readout = $t_{D2} + 2t_{wi} - t_{oi} + t_{D3}$

FIGURE 8: FRAME READOUT TIMING DIAGRAM

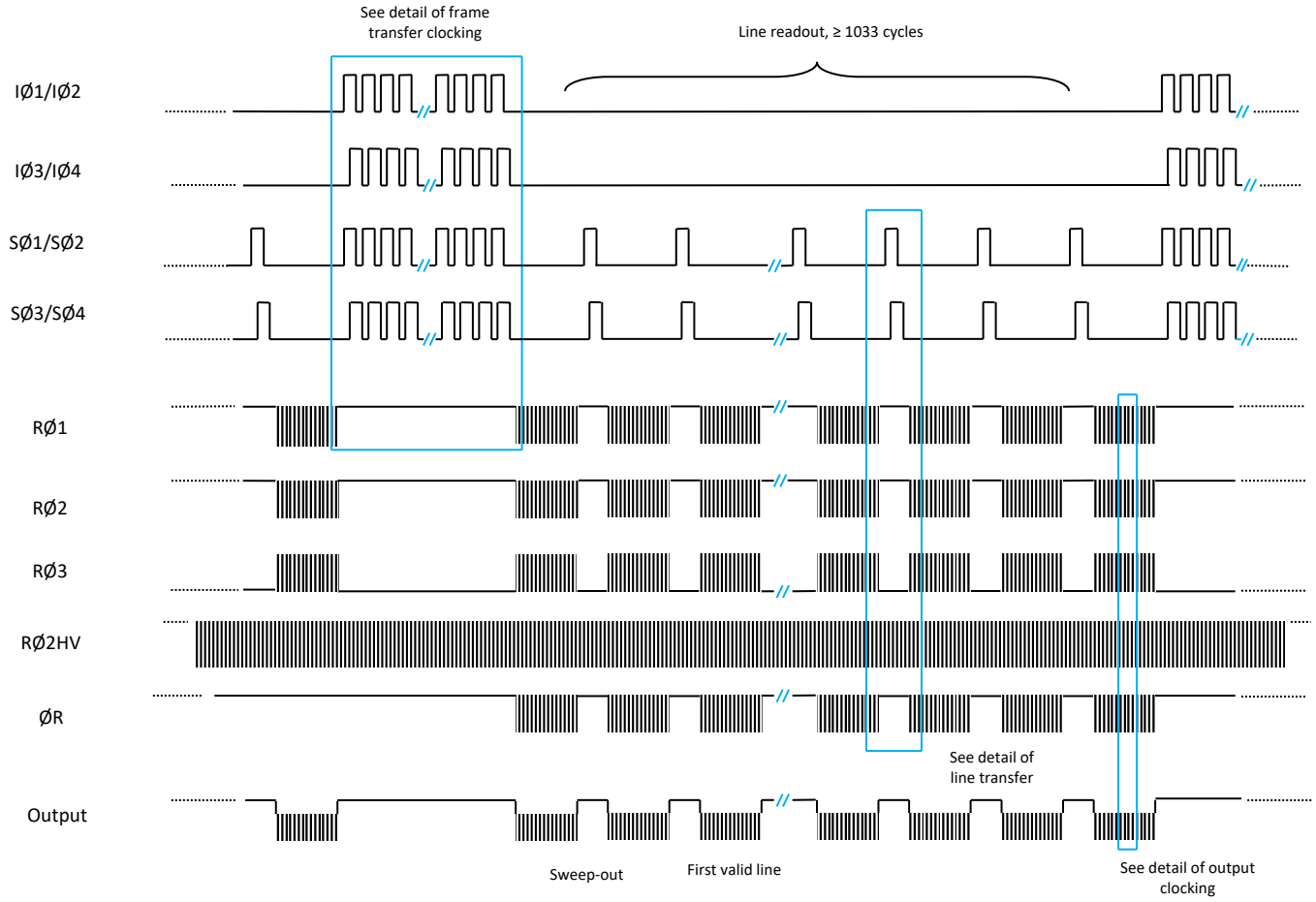


FIGURE 9: FRAME TRANSFER CLOCKING

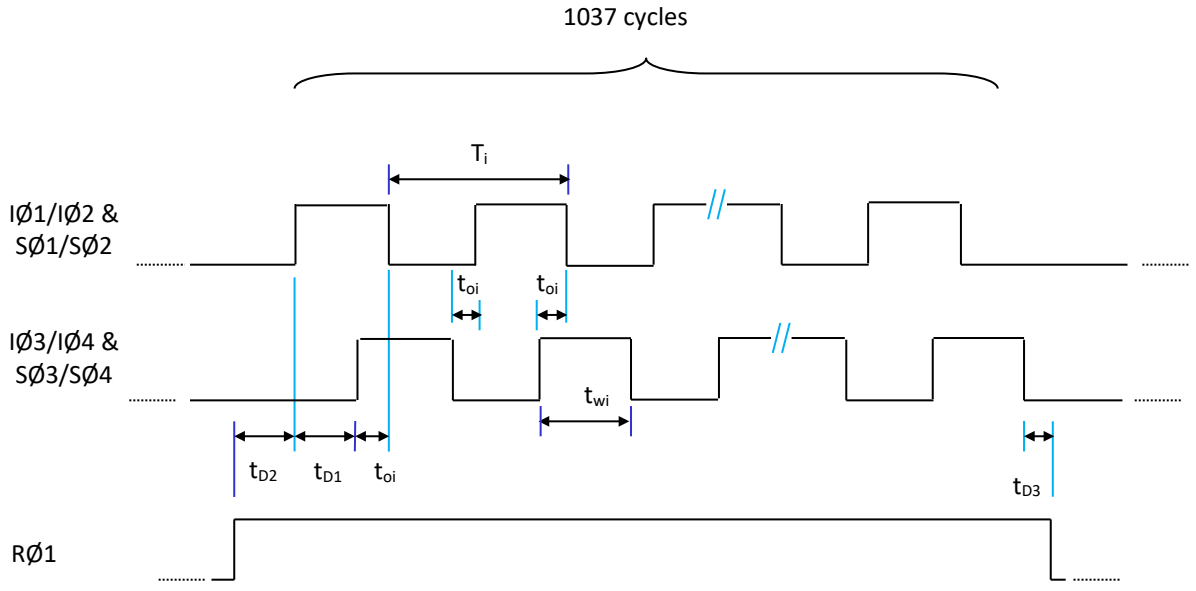


FIGURE 10: DETAIL OF LINE TRANSFER

(Operation through OSL, see Note 11 and Note 22)

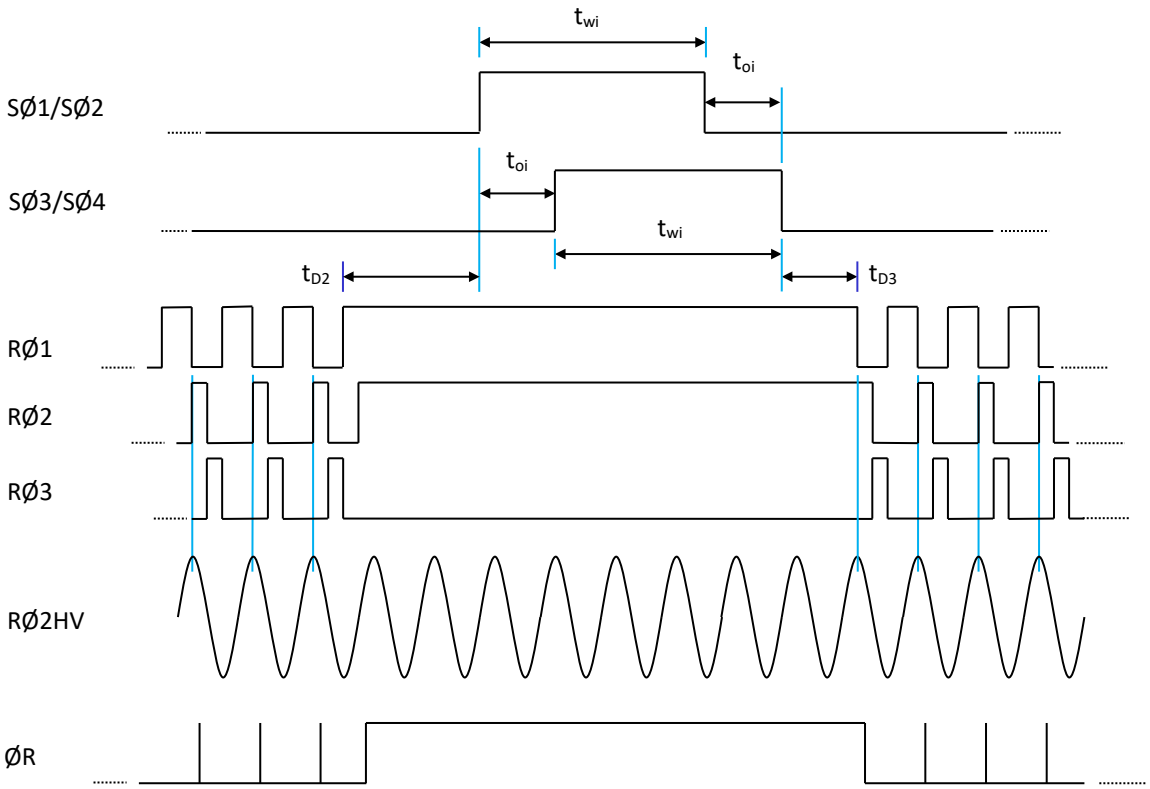
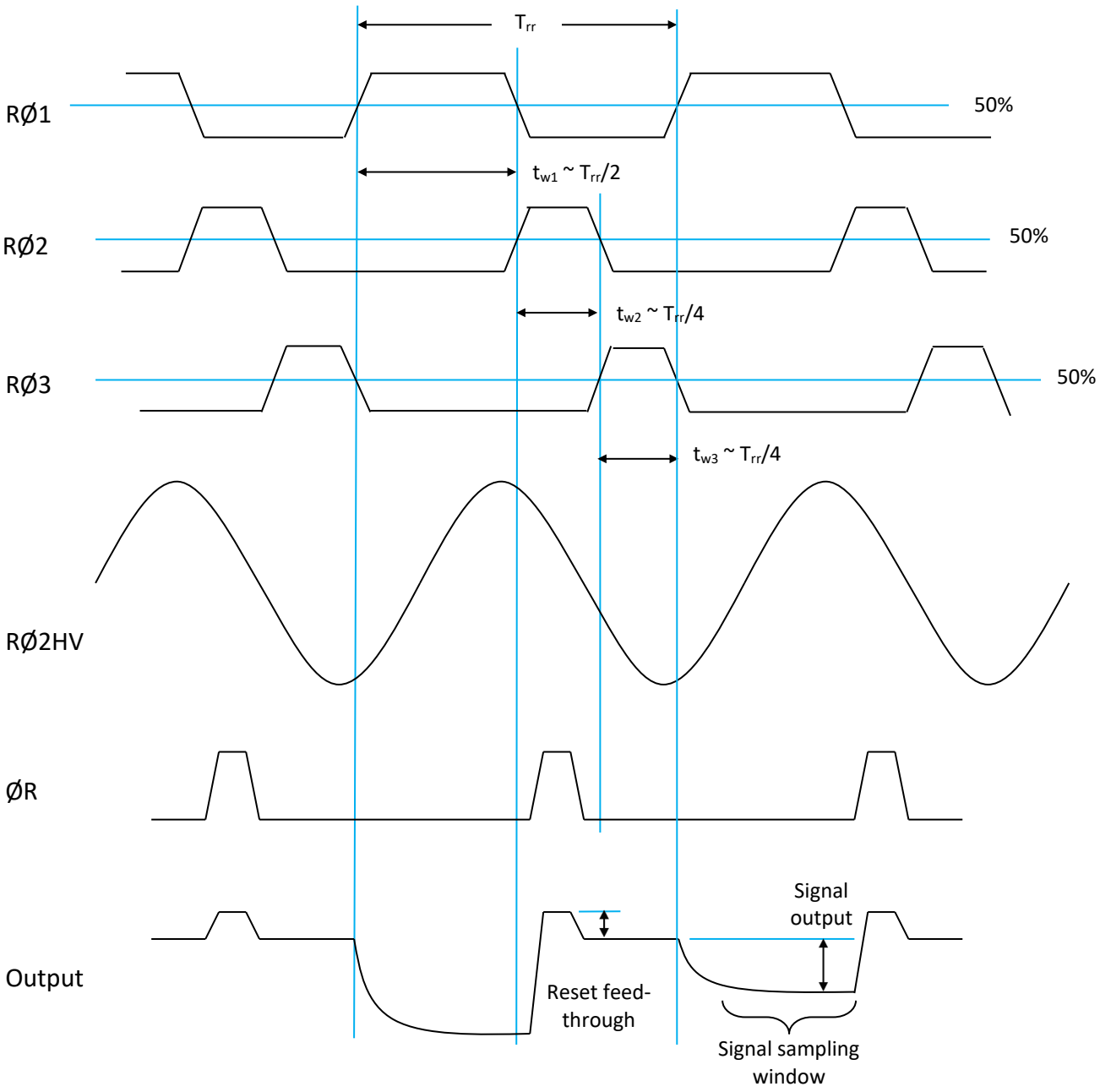


FIGURE 11: DETAIL OF OUTPUT CLOCKING

(Sinusoidal Clocking Scheme, see Note 22, used for factory testing)

RØ2HV can also be of a trapezoidal pulse shape, as shown in Figure 12 overleaf. The RØ2HV pulse should reach full amplitude before RØ1 starts to fall. The edge times are not critical and could be ~5% of the read-out period.



Notes

Note 22. To operate through the OSH output amplifier, the RØ1 and RØ2 waveforms should be interchanged.

FIGURE 12: DETAIL OF OUTPUT CLOCKING

(Trapezoidal Clocking Scheme, see Note 22, not used for factory testing)

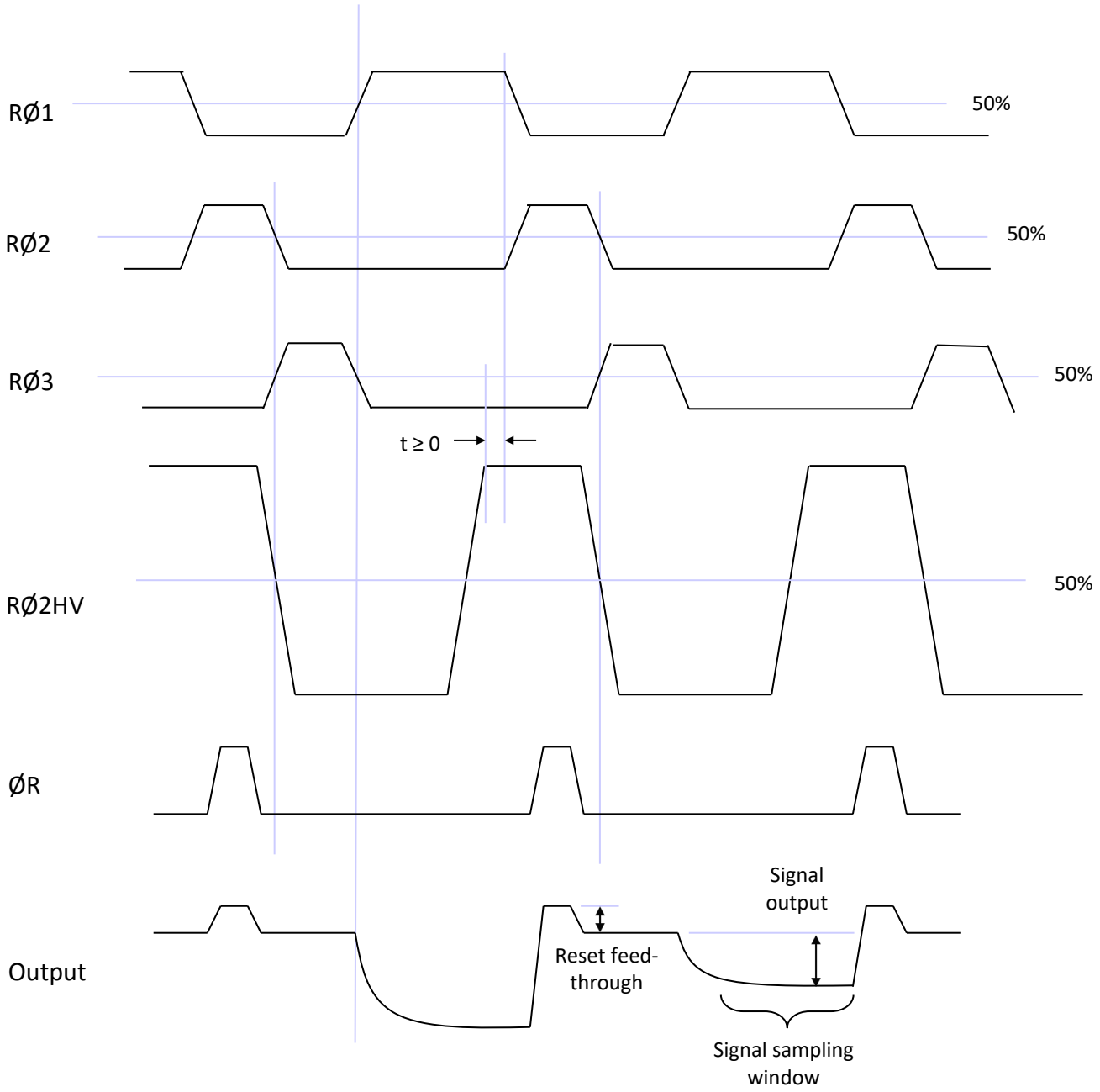
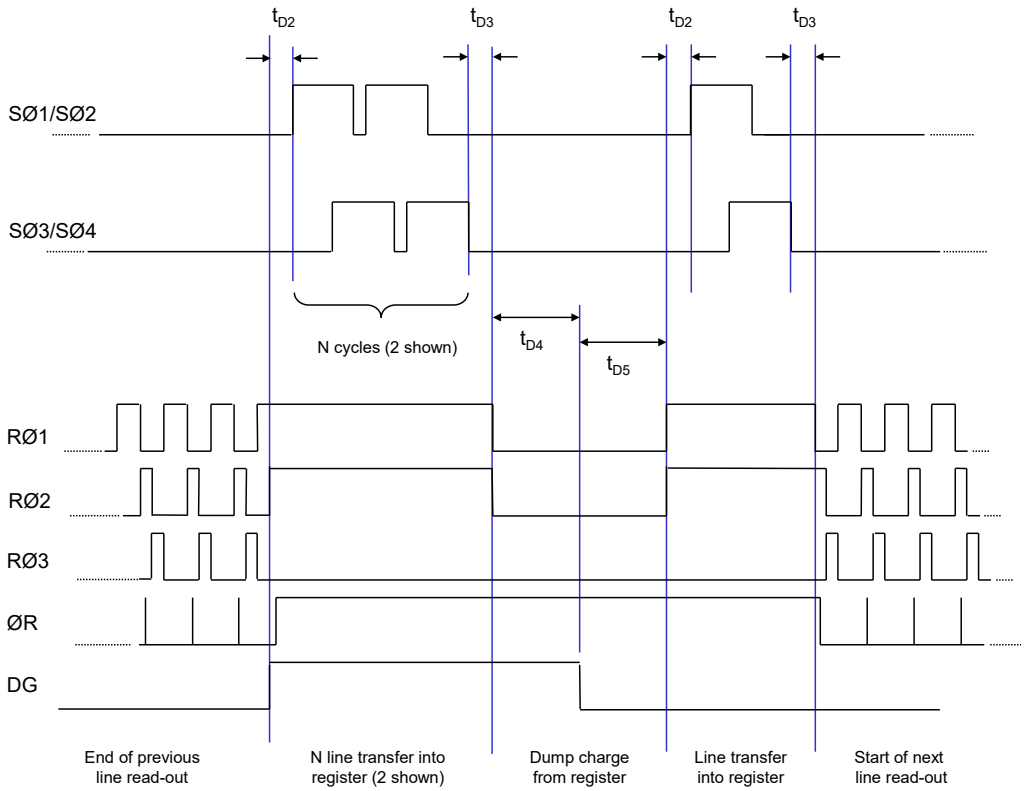


FIGURE 13: LINE DUMPING – IF REQUIRED



RØ2HV Not shown

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Furthermore, unlike most Teledyne e2v devices, the CCD201 is NOT provided with anti-static protection devices on all gate connections – during operation RØ2HV requires a high voltage peak amplitude for gain multiplication that is not compatible with standard gate protection structures. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be grounded

Evidence of incorrect handling will invalidate the warranty.

The devices are assembled in a clean room environment and Teledyne e2v technologies recommend that similar precautions are taken by the user to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at Teledyne e2v with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

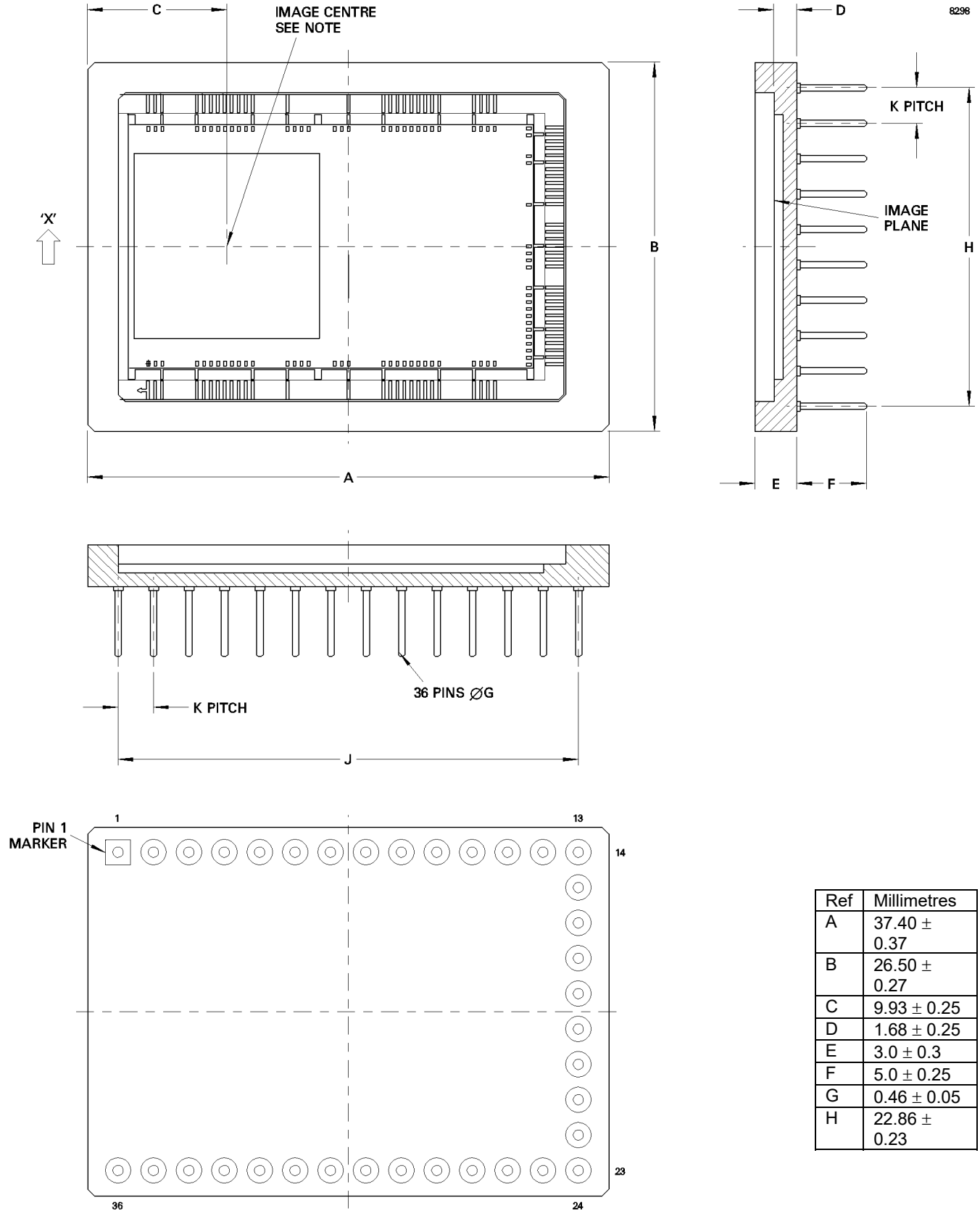
TEMPERATURE RANGES

Component	Min	Max
Operating Temperature	-120°C	+75°C
Non-Operating Temperature	-200°C	+100°C
Rate of change		5°C/min

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage. Full performance is only guaranteed at the nominal operating temperature of 18°C.

GEOMETRY

FIGURE 14: PACKAGE OUTLINE (Tolerances are by design and not verified on each part)



Ref	Millimetres
A	37.40 ± 0.37
B	26.50 ± 0.27
C	9.93 ± 0.25
D	1.68 ± 0.25
E	3.0 ± 0.3
F	5.0 ± 0.25
G	0.46 ± 0.05
H	22.86 ± 0.23

The image centre is aligned centrally in the package in direction 'X', to within a tolerance of ±0.20mm.