CCD55-20 Inverted Mode Sensor
770 x 1152 Pixel Full-Frame Back Illuminated CCD Sensor

FEATURES

- 770 x 1152 pixel Image Area
- 22.5 µm Square Pixels
- Low Noise and High Speed Output Amplifiers
- 100% Active Area
- Gated dump drain on Output Register
- Advanced Inverted Mode Operation (AIMO)
- Back Illuminated

INTRODUCTION

This version of the CCD55 family of CCD Sensors is normally used as a full-frame imaging device although the image area is split into two sections (A and B) that can be clocked separately if required for frame transfer operation. The CCD55 has a single serial output register that has separate charge detection circuits incorporated at each end. One output (A1) is intended for high-speed applications and has an associated dummy output. The maximum speed of this output is approximately 12 MHz when driven into a 10 pF load. At this frequency the output is sufficiently settled for reliable CDS. Operation up to 20 MHz should be achievable if incomplete settling can be tolerated. This output has a charge handling capacity of at least two binned pixels. The second output (A2) is designed for the lowest noise performance whilst still being able to handle the full well capacity of one pixel (approximately 450,000 electrons).

The CCD55 is intended as an upgrade to the CCD05 and is mostly pin compatible with the CCD05. The main features that have been upgraded are the output amplifiers which are now significantly lower noise and higher speed, the pixel full well capacity has been significantly enhanced, a register dump drain has been added and the new design is now compatible with the standard backthinning process.

GENERAL DATA

Format

Image area ..... 17.3 x 25.9 mm
Active pixels:
  horizontal..... 770
  vertical..... 1152
Pixel size ..... 22.5 x 22.5 µm

17 additional pixels are provided at each end of the output register for output settling purposes.

Number of output amplifiers..... 2

The device has a 100% fill factor for maximum sensitivity.

PACKAGE

Format ..... ceramic 44-pin
Size..... 45.7 x 33.0 mm
Inter pin spacing .....2.54 mm
Inter row spacing ..... 35.56/40.64 mm

TYPICAL PERFORMANCE

Output amplifier responsivity:
  A1 ..... 1.2 µV/e^-
  A2 ..... 3.0 µV/e^-
Maximum speed:
  A1 ..... 12 MHz
  A2 ..... 7 MHz
Readout noise (140 – 253 K)
  A2 .....3 e^- rms
Peak signal (no binning)..... 450,000 e^-/pixel/s
Dark signal (at 293 K) .....700 e^-/pixel/s
Charge transfer efficiency
  parallel..... 99.9999%
  serial 99.9993%
Dark signal non-uniformity, 1σ
  (at 293 K)..... 175 e^-/pixel/s
Readout register capacity..... 2 x pixel
Minimum spectral range ..... 200 – 1100 nm

Note: All values quoted using typical operating conditions at a readout frequency of 20 kHz and at a temperature of 253 K (approx).

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TYPICAL OPERATING CONDITIONS

Ref	Pin No	Description	Typ. Voltage
Vss	11,33	Substrate	9.5 V
AØ1	10,34		
AØ2	9,35	Parallel clocks (high level)	12 V
AØ3	8,36		
BØ1	12,32		
BØ2	13,31	Parallel clocks (high level)	12 V
BØ3	14,30		
RØ1	24		
RØ2	21	Register clocks (high level)	12 V
RØ3	22		
ØR1	25	A1 reset pulse (high level)	12 V
ØR2	20	A2 reset pulse (high level)	12 V
V_{OG}	23	Output gates	3 V
V_{OS} 1	28	Output source (A1)	
V_{DOS}	27	Dummy output source (A1)	
V_{OS}2	18	Output source (A2)	
V_{RD}1	26	Reset drain (A1)	17 V
V_{RD}2	19	Reset drain (A2)	17 V
V_{OD}1	29	Output drain (A1)	29 V
V_{OD}2	17	Output drain (A2)	29 V
V_{DG}	3,42	Dump gate (norm/dump)	0/12 V
V_{DD}	16	Dump drain	24 V
V_{ABD}	6,39	Antiblooming drain (see note 1)	24 V
V_{IG}	2,43	Isolation gate (see note 5)	0 V
nc	1,4,5,7,15,37,38,40,41,44		No connection

R_L	External load resistor	A1 5 kΩ
		A2 3.3 kΩ

Nomenclature

Vss	-	Substrate
AØ1, AØ2, AØ3	-	Image area clocks
RØ1/2/3	-	Serial register clocks
ØR	-	Reset clock
ØSW	-	Summing well
DG	-	Register dump gate
OG1, OG2	-	Output gates
DD	-	Dump drain
OD	-	Output drain
OS	-	Output source
RD	-	Reset drain
RL	-	Load resistor (for FET use)
OP	-	JFET source (output)
JD	-	JFET drain

NOTES

1. Although antiblooming is not provided on this sensor, these connections should be made to the appropriate voltages to ensure correct operation of the device.
2. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.
3. With the RØ connections shown this device will operate through A2. In order to operate from the A1 RØ1 and RØ2 should be reversed.
4. OS = 3 – 5 V below OD typically.
5. Charge can be reverse clocked into the drain at the top of the device. During this period of clocking V_{IG} should be raised to 12 V.

BLEMISH SPECIFICATIONS

(For CCD without any coatings or windows)

Grade	0	1	2
Column defects - black or slipped	0	2	6
- white	0	0	2
White spots	60	100	150
Black spots	20	100	200
Traps >200e^-	2	5	12

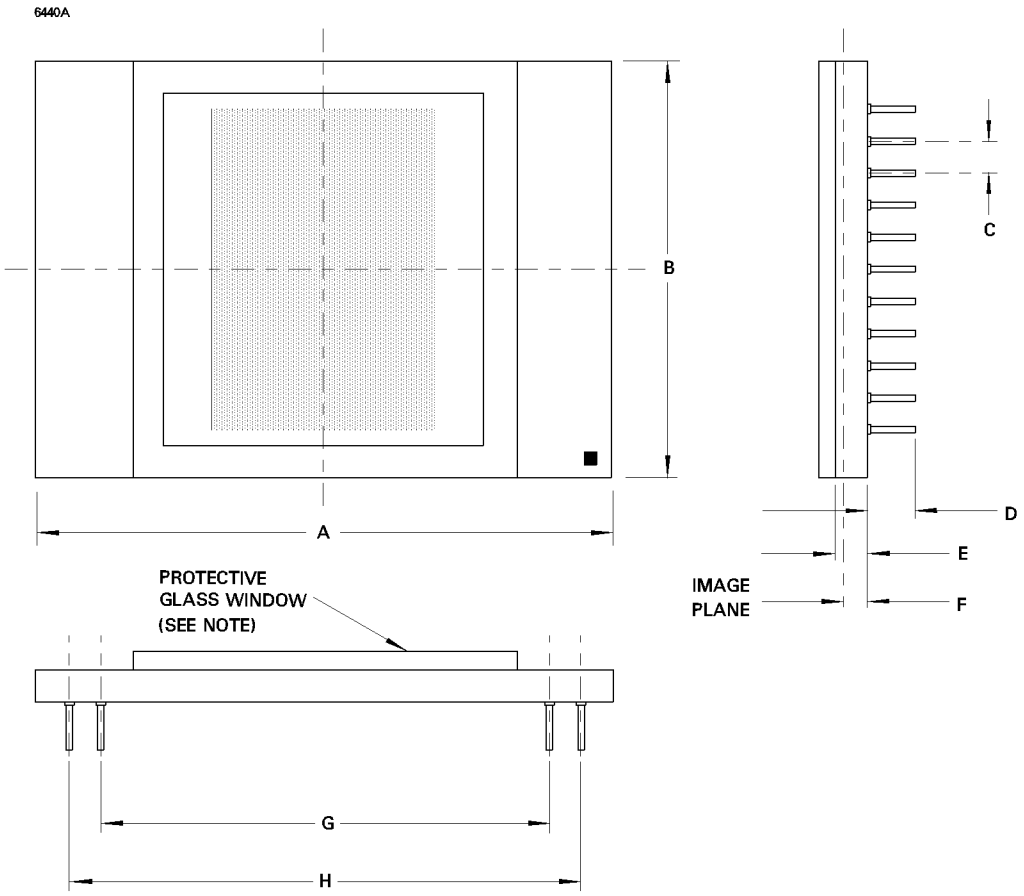
Minimum separation between adjacent column defects is 50 pixels.

Package

As CCD05-20

OUTLINE (All dimensions nominal)

Not for inspection purposes



Ref	Millimetres
A	45.72
B	33.02
C	2.54
D	3.81
E	2.29
F	1.68
G	35.56
H	40.64

Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

PIN CONNECTIONS (View on pins)