# CCD44-82 Scientific CCD Sensor
# Back Illuminated, 2048 x 4096 Pixels, Non Inverted Mode Operation

## INTRODUCTION

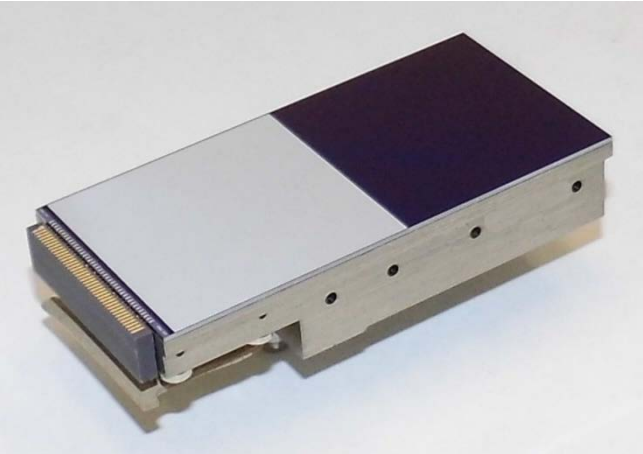
These devices offer an image area of 2048 x 4096 pixels in full frame (FF) architecture and 2048 x 2048 pixels in frame transfer (FT) architecture. Back illumination technology, in combination with an extremely low noise amplifier, makes the devices well suited to the most demanding applications, such as astronomy.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional scientific CCDs at pixel rates as high as 1 MHz. The low output impedance and optional FET buffer simplify the interface with external electronics.

The readout register has a gate-controlled dump-drain to allow fast dumping of unwanted data. The register is designed to accommodate three image pixels of charge and a summing well is provided capable of holding four image pixels. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

The device is supplied in a package designed to facilitate the construction of large close-butted mosaics and is designed to be used cryogenically. The design of the package will ensure that the device flatness is maintained at the working temperature.

The sensor is shipped in a protective container, but no permanent window is fitted.



This figure shows the storage area covered by a metal light shield for FT variants. FF and FT variants are available without this ‘store shield’.

## SUMMARY SPECIFICATION

| | |
|---|---|
| Number of pixels | 2048(H) x 4102(V) |
| Pixel size | 15 µm square |
| Image area FF | 30.7 mm x 61.4 mm |
| Image area FT | 30.7 mm x 30.7 mm |
| Outputs | 2 |
| Package size | 31.7 mm x 66.6 mm |
| Package format | Invar metal package with PGA connector |
| Focal plane height | 14.0 mm above base |
| Connectors | PGA |
| Flatness | 20µm p-v |
| Amplifier responsivity | 6.0 µV/$e^-$ |
| Readout noise | 2.5 $e^-$ at 20kHz |
| Maximum data rate | 1 MHz |
| Image pixel charge storage | 200,000 $e^-$ |
| Dark signal (at 153K) | 0.01 $e^-$/pixel/hour |

Quoted performance parameters given above are “typical” values. Specification limits are shown later in this datasheet.



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Template: DF764388A Ver 17

127244

## ELECTRO-OPTICAL PERFORMANCE (At 173K unless stated)

| Parameter | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|
| Peak charge storage (image) | 150,000 | 200,000 | - | e-/pixel | 1 |
| Peak charge storage (register) | - | 600,000 | - | e-/pixel | |
| Output node capacity: | | | | | |
| OG2 low (mode 1) | - | 300,000 | - | e- | 2 |
| OG2 high (mode 2) | - | 1,200,000 | - | e- | |
| Output amplifier responsivity: | | | | | |
| OG2 low (mode 1) | 4.5 | 6.0 | - | µV/e- | |
| OG2 high (mode 2) | - | 1.5 | - | µV/e- | |
| Readout noise | - | 2.2 | 4.0 | e- rms | 3 |
| Readout frequency | - | 20 | 1000 | kHz | 4 |
| Dark signal (at 153 K): | | | | | |
| Standard silicon | - | 0.01 | 1.00 | e-/pixel/hr | 5 |
| Deep depletion silicon | - | 0.02 | 2.00 | e-/pixel/hr | |
| Charge transfer efficiency: | | | | | |
| Parallel | 99.9990 | 99.9995 | - | % | 6 |
| Serial | 99.9990 | 99.9998 | - | % | |

**Notes:**

1. Signal level at which resolution begins to degrade.
2. Operation of the OG2 gate modified the output node. OG2 low (mode 1) is normally used for low noise high responsivity.
3. Measured with correlated double sampling at 20 kHz pixel rate with OG2 = OG1 + 1 V.
4. Depending on the external load capacitance to be driven. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.
5. Dark signal is typically measured at 173 K with the substrate voltage at +9.0 V for standard silicon (3.0 V for deep depletion silicon). It is a strong function of temperature and the typical average (background) dark signal is taken as:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Qdo is the dark current at 293 K.
6. Measured with a 55Fe X-ray source.

## COSMETIC SPECIFICATION

Maximum allowed defect levels are indicated below.

**Standard Silicon**

| Grade | 0 | 1 | 2 |
|---|---|---|---|
| Total column defects (black and white) | 2 | 6 | 12 |
| White spots | 250 | 500 | 1000 |
| Total spots (black and white) | 750 | 1250 | 2000 |
| Traps | 20 | 30 | 50 |

**Deep Depletion Silicon**

| Grade | 0 | 1 | 2 |
|---|---|---|---|
| Total column defects (black and white) | 2 | 6 | 12 |
| White spots | 500 | 1000 | 1500 |
| Total spots (black and white) | 1250 | 2000 | 3000 |
| Traps | 20 | 30 | 50 |

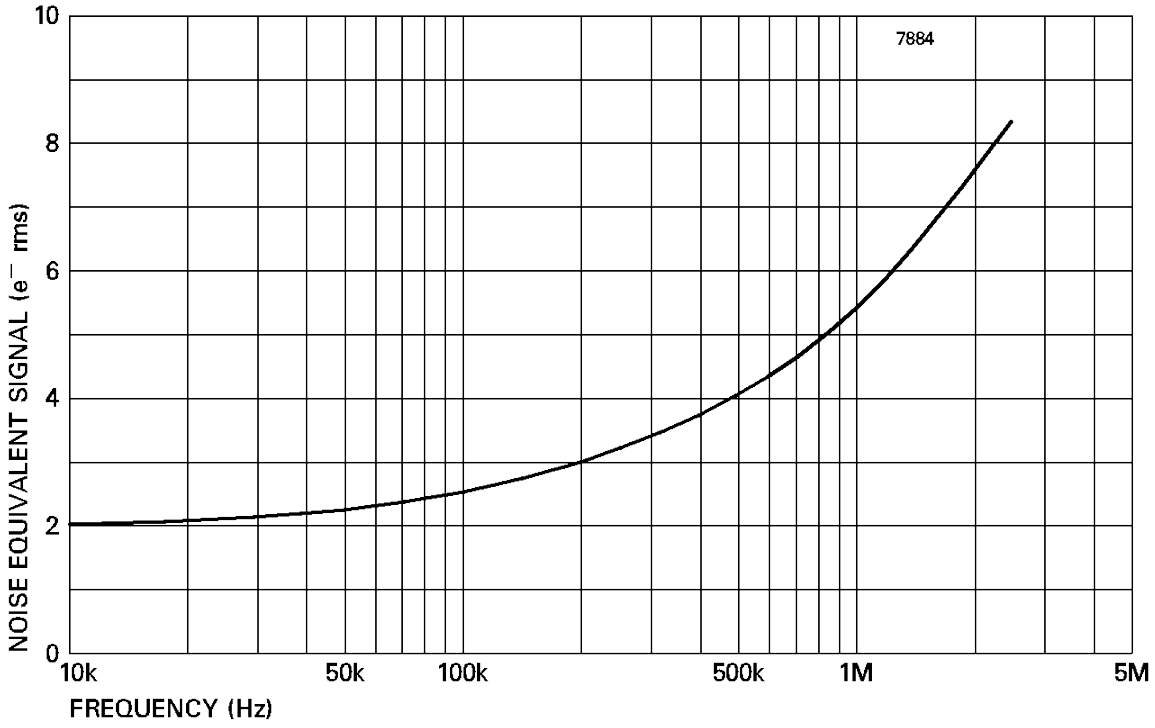
**Grade 5** devices are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

**Definitions**

| | |
|---|---|
| **White spots** | A defect is counted as a white spot if the dark generation rate is more than 100 e-/pixel/hr at 153 K (typically measured at 173 K). The typical temperature dependence is given by $Q_d/Q_{do} = 122 \times T^3 e^{-6400/T}$ |
| **Black spots** | A black spot defect is a pixel with a response less than 80% of the local mean signal. |
| **Column defects** | A column is counted as a defect if it contains at least 100 white or dark single pixel defects. |
| **Traps** | A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e- at 173 K |

## TYPICAL OUTPUT AMPLIFIER NOISE

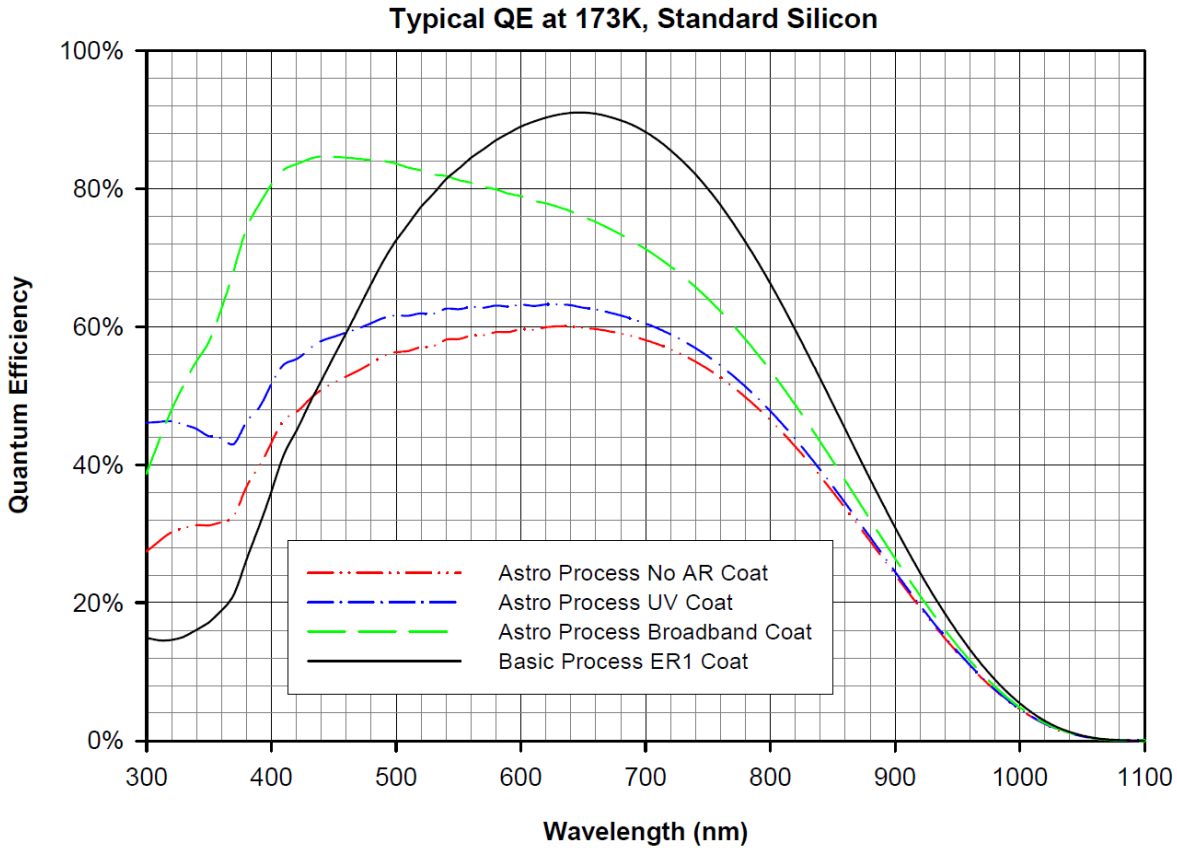
The variation of typical read noise with operating frequency is shown below (measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1 at approximately 173 K).



# SPECTRAL RESPONSE AT 173K

**Standard Silicon**

| Process/Coating: | Astro-BB | Astro-UV | Astro-No Coat | Basic-ER1 | Any |
|---|---|---|---|---|---|
| **Wavelength (nm)** | **Minimum QE (%)** | | | | **Maximum PRNU (1σ) (%)** |
| 350 | 40 | 37 | - | 10 | - |
| 400 | 70 | 48 | - | 25 | 3 |
| 500 | 80 | 60 | - | 60 | - |
| 650 | 75 | 60 | - | 85 | 3 |
| 900 | 25 | 20 | - | 25 | 5 |

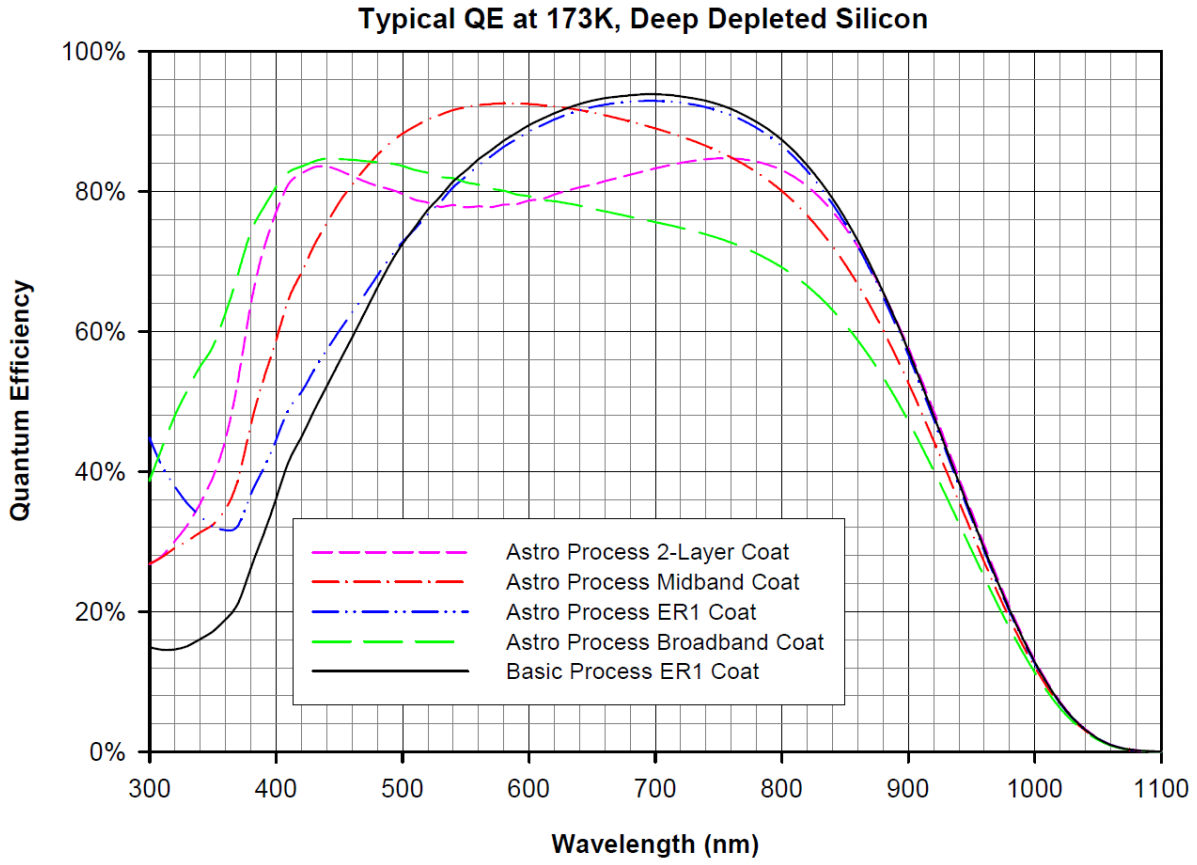



Abbreviations:

| | |
|---|---|
| Astro | Astronomy process (for improved UV QE) |
| BB | Broadband |
| ER | Extended Red |
| MB | Midband |
| Multi-2 | 2-layer AR coating |
| UV | Ultraviolet |

**Deep Depletion Silicon**

| Process/Coating: | Astro-MB | Astro-BB | Astro-ER1 | Astro-Multi-2 | Basic-ER1 | Any |
|---|---|---|---|---|---|---|
| **Wavelength (nm)** | **Minimum QE (%)** | | | | | **Maximum PRNU (1σ) (%)** |
| 350 | 20 | 40 | 20 | 30 | 10 | - |
| 400 | 50 | 70 | 35 | 70 | 25 | 3 |
| 500 | 80 | 75 | 65 | 75 | 60 | - |
| 650 | 80 | 70 | 80 | 75 | 85 | 3 |
| 900 | 40 | 40 | 45 | 50 | 45 | 5 |




Abbreviations:

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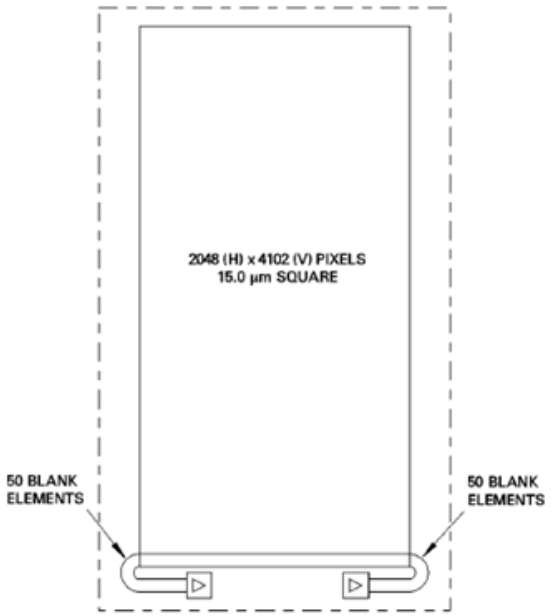
| UV | Ultraviolet |

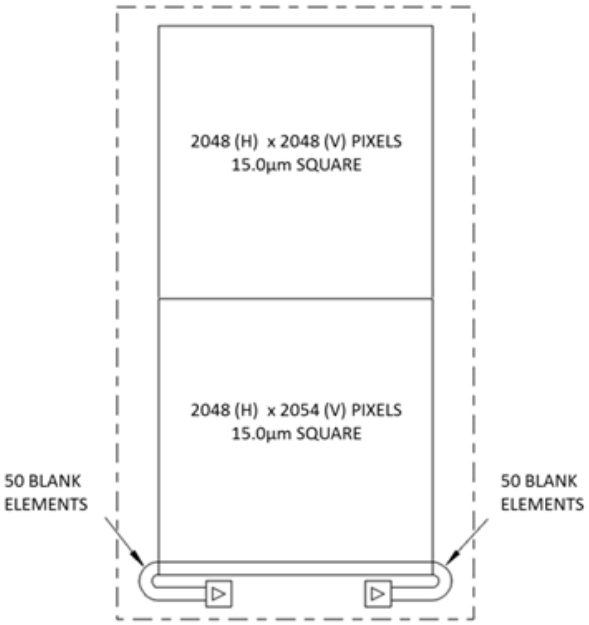
# ARCHITECTURE

## Device Schematic

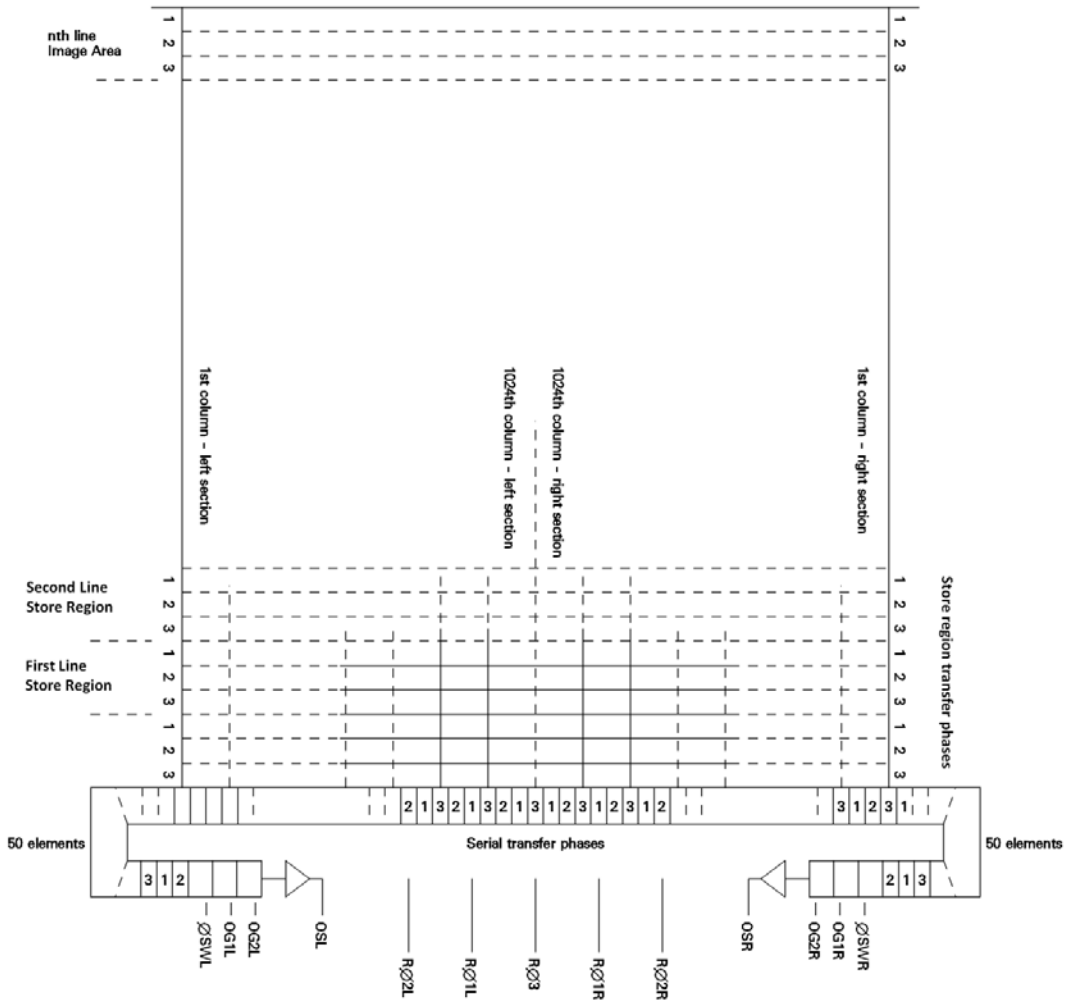
Full Frame (FT)




Frame Transfer (FT)

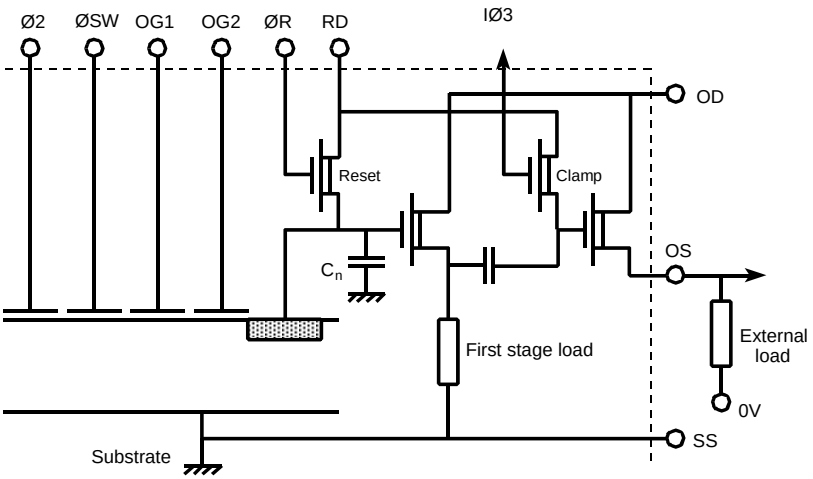



## Arrangement of Electrodes



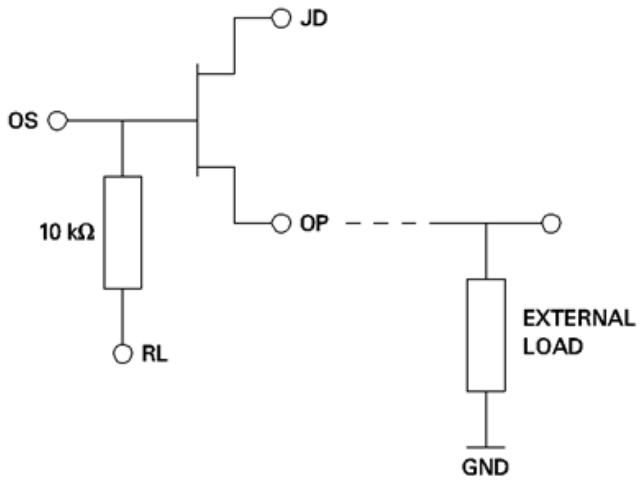
# ELECTRICAL INTERFACE

### Details of Output Circuit



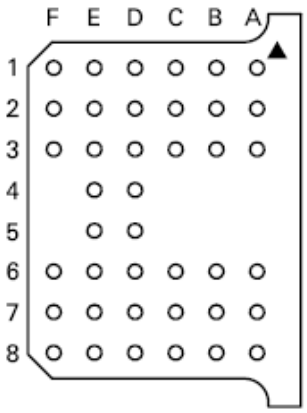

The output impedance is typically 300 Ω.

### Details of FET Buffer




### Pin Connections

View facing underside of package. Pin A1 is clearly marked.



**Connections, Typical Voltages and Absolute Maximum Ratings**

The tables below give the pin-outs and clock amplitudes. If all voltages are set to the typical values, operation at, or close to, specification should be obtained. Some adjustment within the minimum-maximum range specified may be required to optimize performance. Refer to the specific device test data if possible.

| PGA PIN | REF | DESCRIPTION | CLOCK AMPLITUDE OR DC LEVEL (V) (see note 7) | | | MAX RATINGS (V) with respect to $V_{SS}$ |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| A1 | SS | Substrate | See Note 8 | | | - |
| A8 | SS | Substrate | | | | |
| C1 | SS | Substrate | | | | |
| C8 | SS | Substrate | | | | |
| F2 | SS | Substrate | | | | |
| F7 | SS | Substrate | | | | |
| D8 | IØ1 | Image clock | 8 | 10 | 15 | ±20 |
| E8 | IØ2 | Image clock | 8 | 10 | 15 | ±20 |
| F8 | IØ3 | Image clock | 8 | 10 | 15 | ±20 |
| D1 | SØ1 | Store clock (Frame Transfer Variant) | 8 | 10 | 15 | ±20 |
| D1 | TS | Temperature Sensor (Full Frame Variant) | See note 13 | | | |
| E1 | SØ2 | Store clock (Frame Transfer Variant) | 8 | 10 | 15 | ±20 |
| E1 | - | Not Connected (Full Frame Variant) | See note 13 | | | |
| F1 | SØ3 | Store clock (Frame Transfer Variant) | 8 | 10 | 15 | ±20 |
| F1 | TS | Temperature Sensor (Full Frame Variant) | See note 13 | | | |
| D4 | RØ1 (L) | Register clock | 8 | 11 | 15 | ±20 |
| E4 | RØ2(L) | Register clock | 8 | 11 | 15 | ±20 |
| D5 | RØ1 (R) | Register clock | 8 | 11 | 15 | ±20 |
| E5 | RØ2(R) | Register clock | 8 | 11 | 15 | ±20 |
| F6 | RØ3 | Register clock | 8 | 11 | 15 | ±20 |
| E3 | ØR (L) | Reset gate | 9 | 12 | 15 | ±20 |
| E6 | ØR (R) | Reset gate | 9 | 12 | 15 | ±20 |
| E2 | ØSW (L) | Summing well gate | 9 | 11 | 15 | ±20 |
| E7 | ØSW (R) | Summing well gate | 9 | 11 | 15 | ±20 |
| F3 | DG (see Note 9) | Dump gate | -0.5 | 0 | 15 | ±20 |
| D3 | OG1 (L) | Output gate | 1 | 3 | 4 | ±20 |
| D6 | OG1 (R) | Output gate | 1 | 2 | 4 | ±20 |
| B2 | DD (L) | Dump drain | 22 | 24 | 26 | -0.3 to +30 |
| B7 | DD (R) | Dump drain | 22 | 24 | 26 | -0.3 to +30 |
| D2 | OG2 (L) | Output gate | See Note 10 | | | ±20 |
| D7 | OG2 (R) | Output gate | See Note 10 | | | ±20 |
| B1 | OD (L) | Output drain | 27 | 29 | 32 | -0.3 to +35 |
| B8 | OD (R) | Output drain | 27 | 29 | 32 | -0.3 to +35 |
| A2 | OS (L) | Output source | See Note 11 | | | -0.3 to +25 |
| A7 | OS (R) | Output source | See Note 11 | | | -0.3 to +25 |
| C2 | RD (L) | Reset drain | 15 | 17 | 19 | -0.3 to +25 |
| C7 | RD (R) | Reset drain | 15 | 17 | 19 | -0.3 to +25 |

| Optional connections for using the 309 JFET (see note 12) | | | | |
|---|---|---|---|---|
| **PGA PIN** | **REF** | **DESCRIPTION** | **CLOCK AMPLITUDE OR DC LEVEL (V)** | **MAX RATINGS (V)** with respect to $V_{SS}$ |
| A3 | RL (L) | Load resistor | $A_{GND}$ (0V) | - |
| A6 | RL (R) | Load resistor | $A_{GND}$ (0V) | - |
| B3 | OP (L) | JFET source | - | - |
| B6 | OP (R) | JFET source | - | - |
| C3 | JD (L) | JFET drain | OD(L) + 2V | - |
| C6 | JD (R) | JFET drain | OD(R) + 2V | - |

**Notes:**

7. For clock pins, the clock high levels are shown except for DG (see note 9). All clock low levels should be 0 ± 0.5V except readout register clocks which should be +1V.

8. Devices can be operated with low substrate (0V) or higher substrate (9V). Low substrate is particularly recommended for deep depleted and bulk variants, since it optimizes depletion depth for best Point Spread Function. For e2v factory testing substrate voltage is set at at +9.0 V for standard silicon and +3.0 V for deep depletion silicon.

9. Non-charge dumping level is shown. For charge dumping DG should be pulse to 12 ± 2V.

10. For operation in high responsivity, low noise mode, OG2=OG1+1V; therefore OG2 should be set to +4V typical. For operation in low responsivity, increased charge handling mode, OG2 should be set to +20V.

11. OS will be 3-5 V below OD. Do not connect to voltage supply but use a 3-5 mA current source or a 5-10 kΩ external load.

12. If not connected the JFETs are floating, with gates connected to OS. A floating 10 kΩ load resistor is also connected to each OS. In this configuration the CCD output is directly accessed via pins A2 and A7. The FET may be used to buffer the chip output (OS) if desired; in this case, connect the FET output on pins A3 and A6 to $A_{GND}$ via an external load supplying ~ 5 mA and also connect RL pins A3 and A6 directly to $A_{GND}$.

13. Pins D1,E1 and F1 change function depending on if the variant is a full frame sensor or a frame transfer sensor. If full frame, an optional PT100 temperature sensor can be fitted which connects to pins D1 and F1.

## Electrical Characteristics

Electrode capacitances (defined at mid-clock level)

| | Typical | Units |
|---|---|---|
| IØ or SØ inter-phase | 20 | nF |
| IØ or SØ /SS | 50 | nF |
| RØ /RØ | 90 | pF |
| RØ /SS | 175 | pF |
| ØR /SS | 20 | pF |

Electrode series resistances

| | Typical | Units |
|---|---|---|
| IØ (FF) | 40 | Ω |
| IØ (FT) | 70 | Ω |
| SØ | 32 | Ω |
| RØ | 10 | Ω |

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate.

## Power up/Power down

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltage for the amplifier drains (pins B1 and B8) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see Note 11) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

## Power Consumption

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

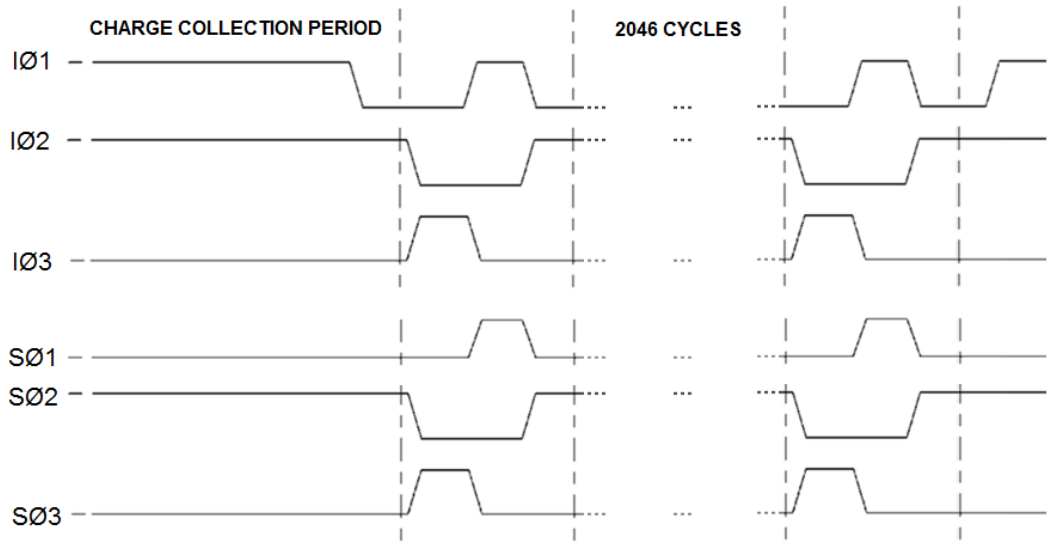
The table below gives representative values for the components of the on-chip power dissipation for the case of a full-frame device with continuous line-by-line read-out using one amplifier. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilized in each case.

| Readout frequency | Line time | Power dissipation | | | |
|---|---|---|---|---|---|
| | | Amplifiers | Serial clocks | Parallel clocks | Total |
| 100 kHz | 40 ms | 20 mW | 10 mW | 1 mW | 31 mW |
| 1 MHz | 4 ms | 20 mW | 100 mW | 10 mW | 130 mW |

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

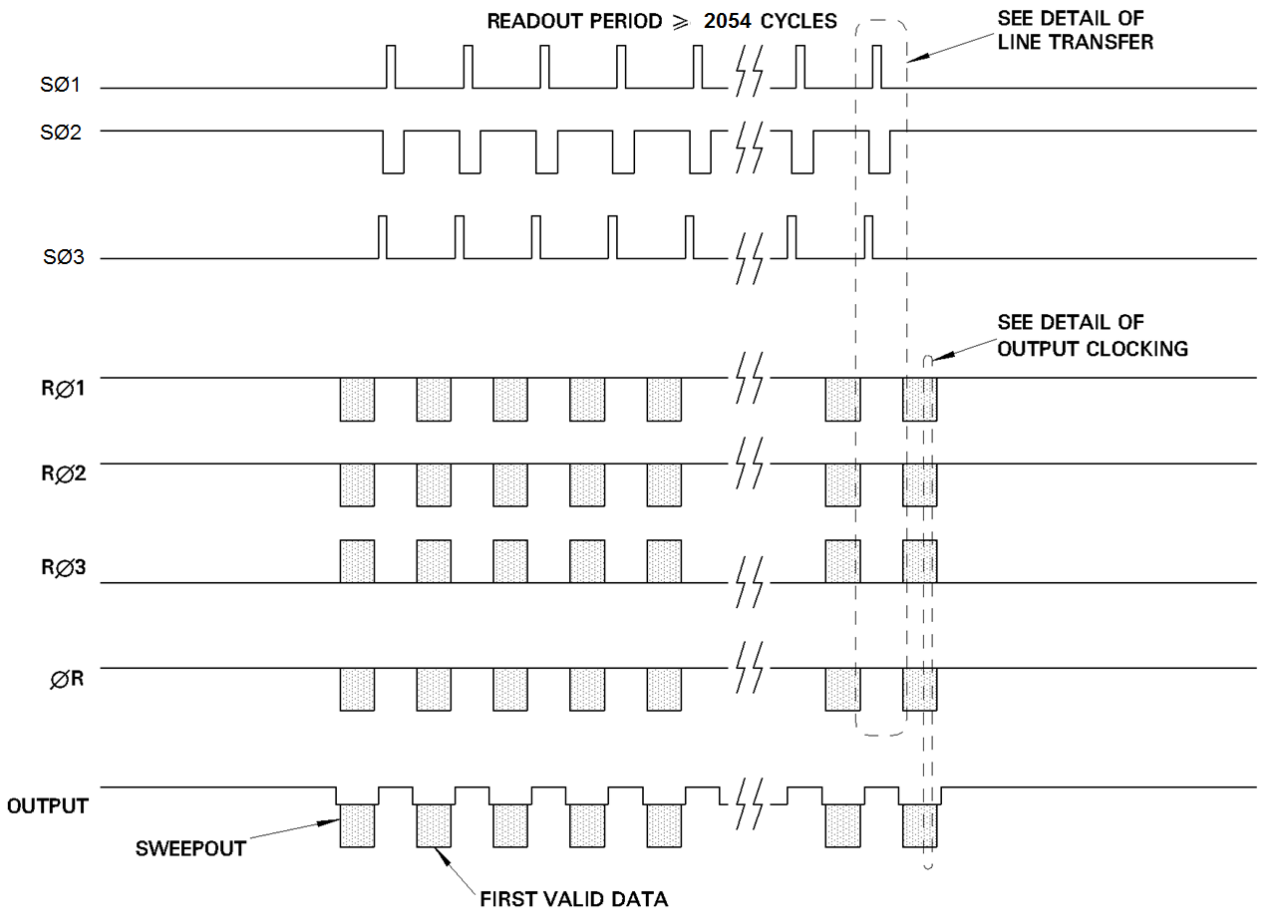
# TIMING INFORMATION

### Frame Transfer Operation (FT variants only)



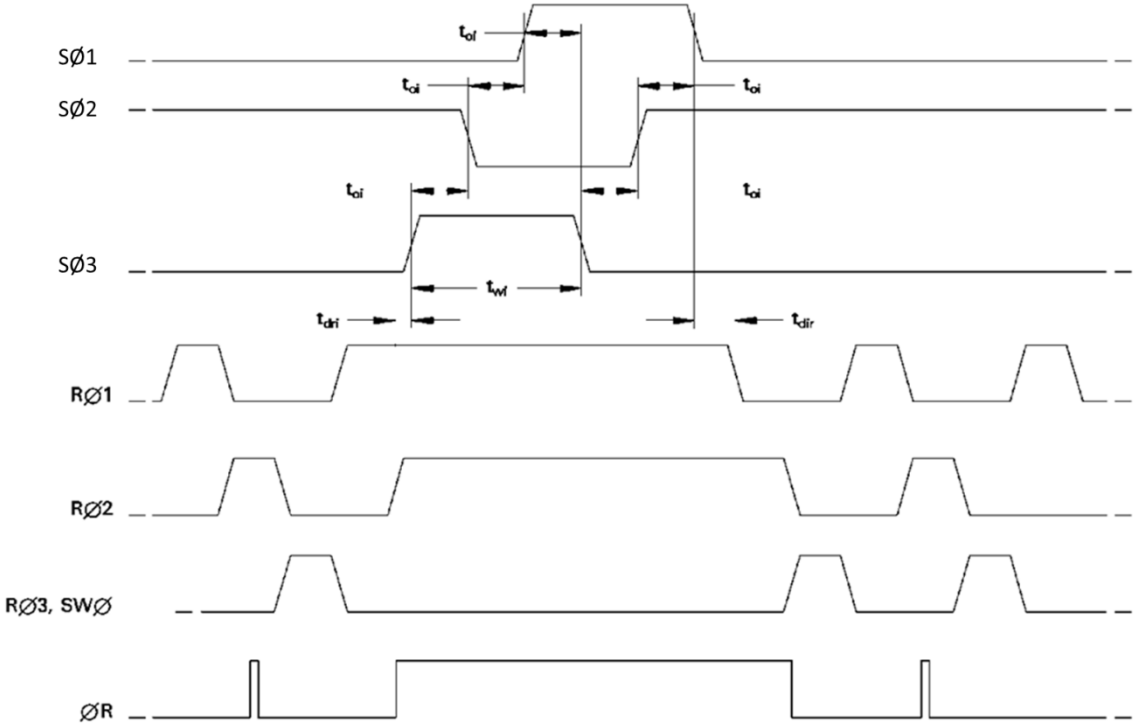

### Frame Readout

For FT variants frame readout can be performed during integration of the next image, i.e. when IØ phases are not clocked.
For FF variants replace SØ label with IØ label below and clock all rows out in darkness following integration.



**Detail of Line Transfer**

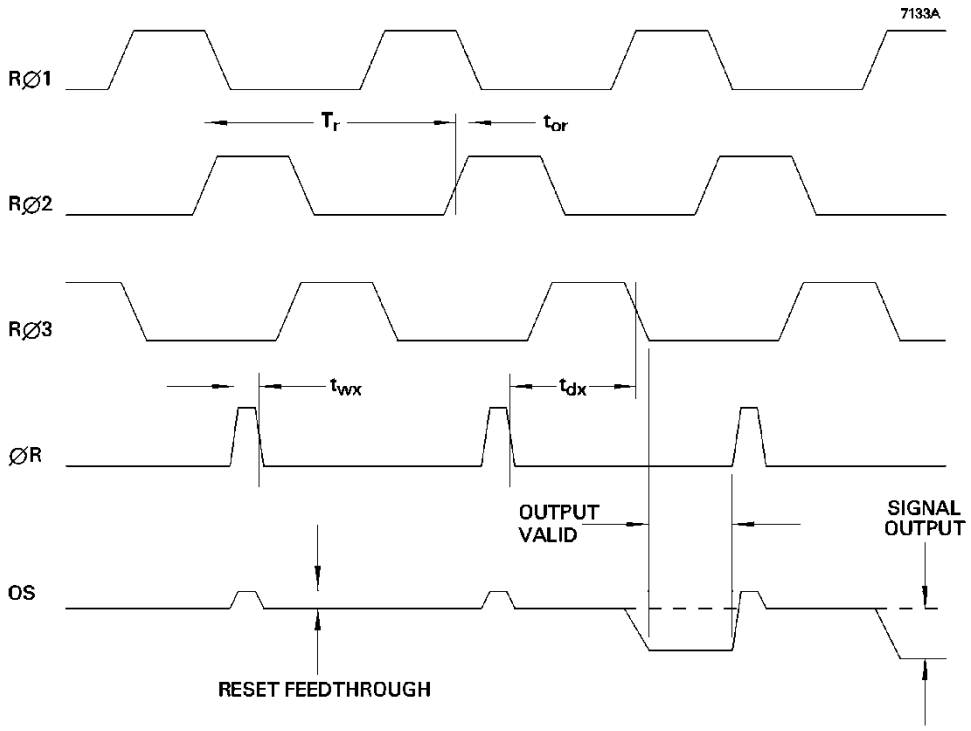
For FF variants replace SØ label with IØ label below.



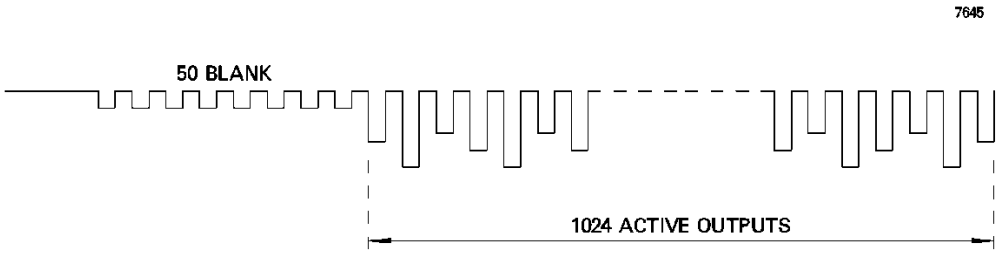

**Notes:**

14. The same clocking pattern as IØ clocks should be applied to SØ clocks. It is particularly important during frame transfer that the IØ phases are synchronised with the corresponding SØ phases.

**Detail of Output Clocking**

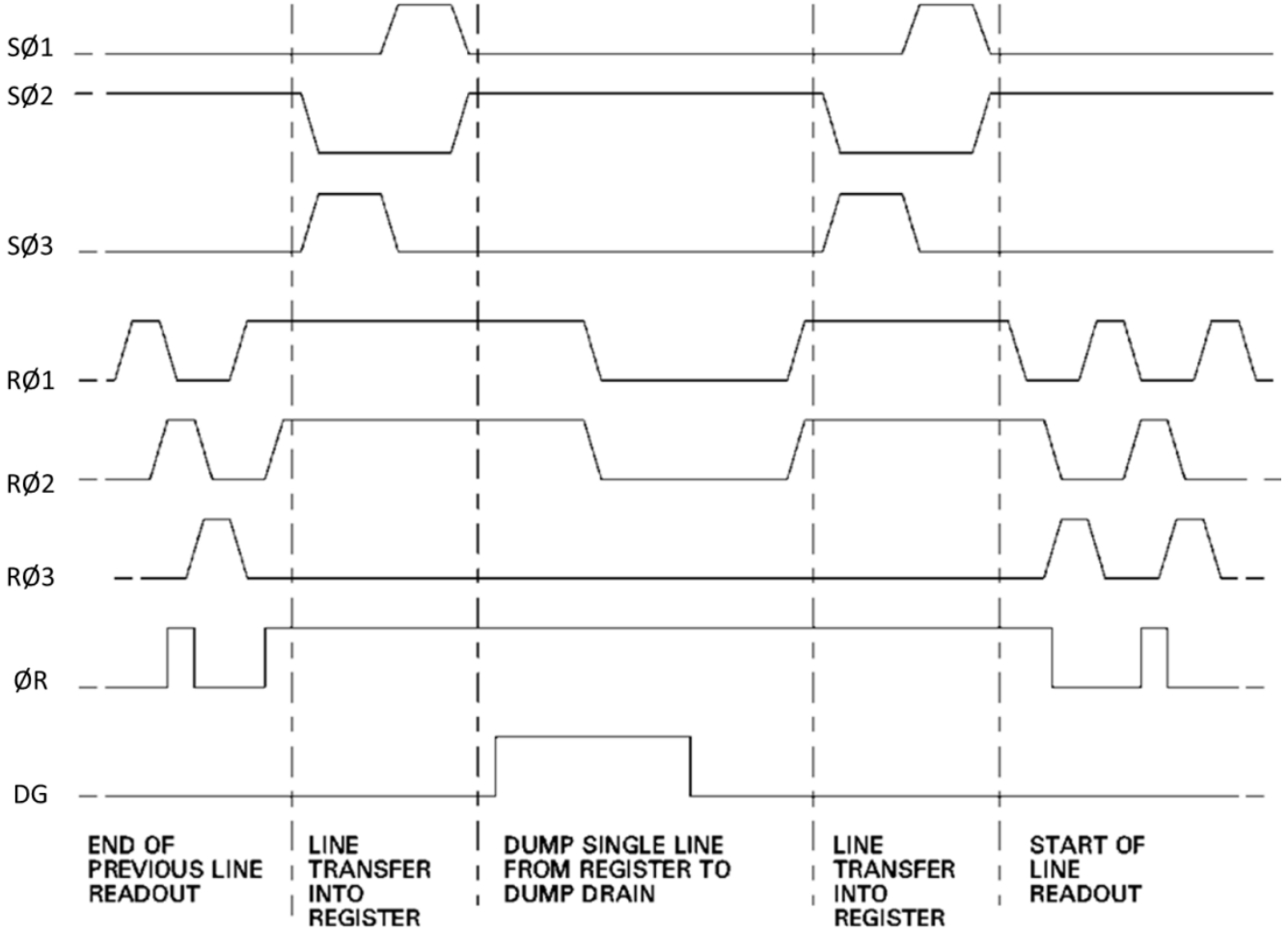


## Line Output Format




**Detail of Vertical Line Transfer (Single Line Dump)**

For FF variants replace SØ label with IØ label below.




**Notes:**

15. During frame transfer, both IØ and SØ phases will be clocked, and so with RØ1 and RØ2 held at high level, any charge in the store region will accumulate in the register. Therefore it is recommended that the dump gate (DG) is held at high level during frame transfer to avoid charge from spilling back in to the store region.

**Clock Timing Requirements**

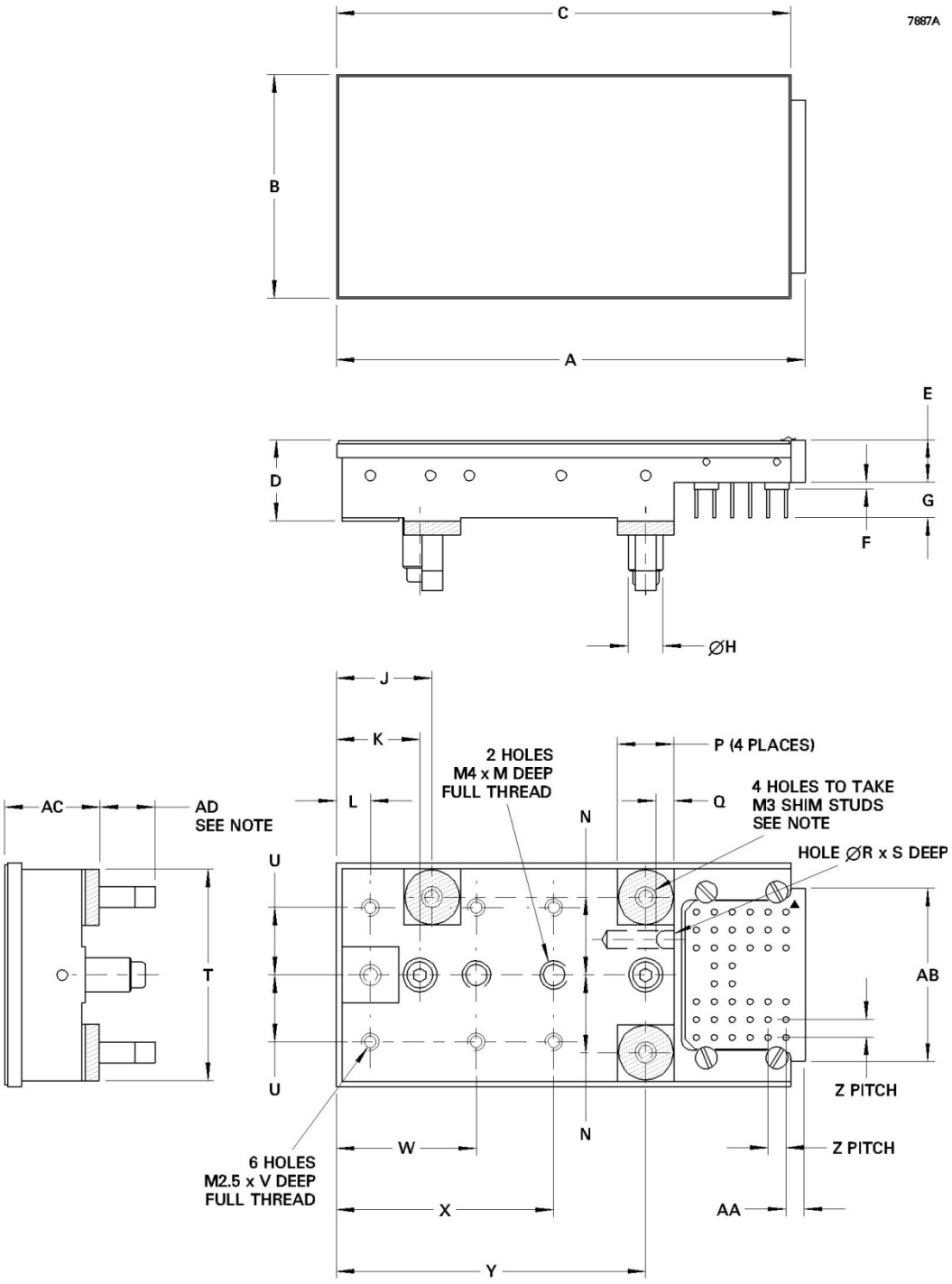
| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $T_i$ | Image clock period | 50 | 100 | (see Note 15) | µs |
| $t_{wi}$ | Image clock pulse width | 25 | 50 | (see Note 15) | µs |
| $t_{ri}$ | Image clock pulse rise time (10 to 90%) | 1 | 10 | 0.5 $t_{oi}$ | µs |
| $t_{fi}$ | Image clock pulse fall time (10 to 90%) | $t_{ri}$ | 10 | 0.5 $t_{oi}$ | µs |
| $t_{oi}$ | Image clock pulse overlap | 5 | 10 | 0.2 $T_i$ | µs |
| $t_{li}$ | Image clock pulse, two phase low | 10 | 20 | 0.2 $T_i$ | µs |
| $t_{dir}$ | Delay time, IØ stop to RØ start | 10 | 20 | (see Note 15) | µs |
| $t_{dri}$ | Delay time, RØ stop to IØ start | 1 | 2 | (see Note 15) | µs |
| $T_r$ | Output register clock cycle period | 1 | (see Note 16) | (see Note 15) | µs |
| $t_{rr}$ | Clock pulse rise time (10 to 90%) | 100 | 0.1 $T_r$ | 0.3 $T_r$ | ns |
| $t_{fr}$ | Clock pulse fall time (10 to 90%) | $t_{rr}$ | 0.1 $T_r$ | 0.3 $T_r$ | ns |
| $t_{or}$ | Clock pulse overlap | 50 | 0.5 $t_{rr}$ | 0.1 $T_r$ | ns |
| $t_{wx}$ | Reset pulse width | 50 | 0.1 $T_r$ | 0.2 $T_r$ | ns |
| $t_{rx}$ | Reset pulse rise and fall times | 20 | 0.5 $t_{rr}$ | 0.2 $T_r$ | ns |
| $t_{dx}$ | Delay time, ØR low to RØ3 low | 50 | 0.5 $T_r$ | 0.8 $T_r$ | ns |

**Notes:**

16. No maximum other than that necessary to achieve an acceptable dark signal at the longer read-out times
17. As set by the read-out period.

# PACKAGE DETAIL

### Package Schematic




| Ref | Dimension (mm) |
|---|---|
| A | 66.64 max |
| B | 31.72 ± 0.01 |
| C | 64.28 ± 0.01 |
| D | 11.65 |
| E | 6.00 |
| F | 1.00 |
| G | 5.00 |
| H | 4.800 ± 0.005 |
| J | 13.55 |
| K | 11.80 |
| L | 4.80 |
| M | 6.00 min |
| N | 11.00 |
| P | 8.00 |
| Q | 2.50 |
| R | 2.50 |
| S | 6.50 |
| T | 30.00 |
| U | 9.50 |
| V | 5.50 min |
| W | 19.80 |
| X | 30.80 |
| Y | 43.80 |
| Z | 2.54 |
| AA | 2.70 |
| AB | 24.5 |
| AC | 14.00 ± 0.01 |
| AD | 8.50 ± 0.1 |

The device is supplied with 3 studs to be used to hold it onto the customer's mounting plate. The default position of the studs is the offset location, shown by dimensions J, Y and U in the figure above. The optional position of the stud at dimension J is the position on the center line of the package denoted by the open square. This non-default configuration would be referred to as the "alternative stud position".

A detailed interface drawing DAS544542AT is available on request.

# ADDITIONAL INFORMATION

### Handling CCD Sensors

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

### High Energy Radiation

Performance parameters will begin to change if the device is subject to ionizing radiation.

Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

### Temperature Range

| | |
|---|---|
| Operating temperature range: | 153 - 323 K |
| Non-operating temperature limit: | 73 - 373 K |

Full performance is only guaranteed at the nominal operating temperature of 173 K. Long term storage outside of the operating temperature range is not recommended.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.

**Part References**

All part numbers are in the format *CCD44-82-g-xxx* where 'g' denotes the device cosmetic grade (Grade 1 is the default) and 'xxx' is the variant code. Each specific variant code defines the build standard in terms of silicon type, AR coating, FF/FT and package options. All variants listed here are NIMO (non-inverted mode, non-MPP) and all are back-thinned. Full Frame variants include a temperature sensor unless specified. Frame Transfer variants cannot be supplied with a temperature sensor.

| Variant Code (-xxx) | Silicon | Coating | Notes |
|---|---|---|---|
| A43 | Standard | Astro UV | Full Frame (FF). Alternative stud position. |
| A72 | Deep Depletion | Basic ER1 | Frame Transfer (FT). |
| B23 | Standard | Astro Broadband | Full Frame (FF). |
| B24 | Standard | Astro Broadband | Full Frame (FF). Fringe suppressed. |
| B43 | Deep Depletion | Astro Broadband | Frame Transfer (FT). |
| C84 | Standard | Astro No-coat | Full Frame (FF). |
| D03 | Deep Depletion | Astro Broadband | Full Frame (FF). |
| D23 | Deep Depletion | Astro ER1 | Full Frame (FF). Fringe suppressed. |
| D26 | Deep Depletion | Astro Midband | Full Frame (FF). Alternative stud position. No Temperature Sensor. |
| D48 | Deep Depletion | Astro ER1 | Full Frame (FF). |
| E17 | Standard | Basic ER1 | Frame Transfer (FT) with store shield. |
| E93 | Deep Depletion | Astro Multi-2 | Full Frame (FF). Fringe suppressed. |

Please check with e2v for availability of any variant.