TELEDYNE e2v
Everywhereyoulook™

CCD40-11 Inverted Mode Sensor
High Performance CCD Sensor

FEATURES

- 1024 by 128 Pixel Format
- 26 mm Square Pixels
- Image Area 26.6 x 3.3 mm
- Wide Dynamic Range
- Symmetrical Anti-static Gate Protection
- Advanced Inverted Mode Operation (AIMO)
- Anti-blooming Readout Register
- Zero Light Emitting Output Amplifier

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- TDI Operation

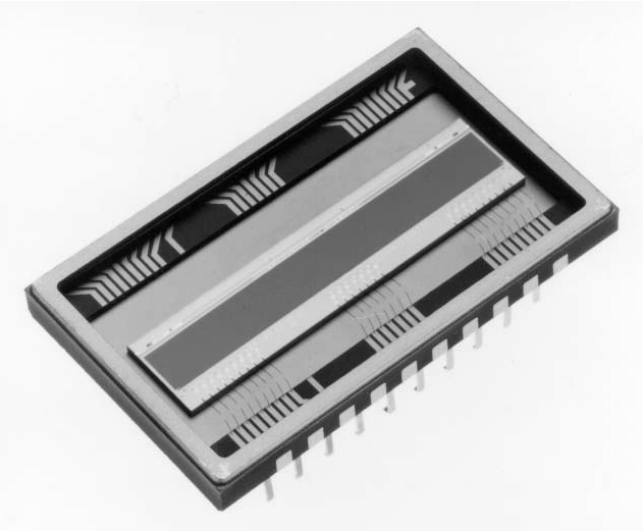
INTRODUCTION

The CCD40-11 is a high performance CCD sensor designed for use in the scientific spectroscopy instrument market. With an array of 1024 x 128 26 mm square pixels it has an imaging area The readout register is organised along the long (1024 pixel) edge of the sensor and contains an anti-blooming drain to allow high speed binning operations of low level signals which may be adjacent to much stronger signals. The novel output amplifier design has no light emission.

Standard three phase clocking and buried channel charge transfer are employed and Advanced Inverted Mode Operation (AIMO) is included as standard. The AIMO format gives the same dark current suppression as with standard IMO devices whilst minimising the reduction in full-well capacity.

The CCD40-11 is packaged in a 20-pin DIL ceramic package and is pin compatible (but not completely clock compatible) with the CCD30-11.

Designers are advised to consult Teledyne e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

Pixel readout frequency……..20 – 5000 kHz
Output amplifier sensitivity……1.5 mV/e^-
Peak signal……..500 ke^-/pixel
Dynamic range……75 000:1
Spectral range……...420 – 1060nm
Readout noise (at 253 K, 20 kHz)……..……4 e^- rms
Q.E. at 700 nm ……..……47 %
Peak Output voltage ……..……750 mV

OVERVIEW

Format

Image area ……...26.6 x 6.7 mm
Active pixels (H)……...1024
(V)……128 (127 usable)
Pixel size ……26 x 26mm

Package

Package size ……32.89 x 20.07 mm
Number of pins 20
Inter-pin spacing ……..2.54 mm
Inter-row spacing…..24 mm
Window material …… ……quartz or removable glass

Teledyne e2v (UK) Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne e2v (UK) Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact Teledyne e2v by e-mail: Enquiries@Teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	400k	500k	–	e^-/pixel
Peak output voltage (unbinned)	–	750	–	mV
Dark signal at 293 K (see note 2)	–	250	500	e^-/pixel/s
Charge transfer efficiency (see note 3): Parallel Serial	 – –	 99.9999 99.9993	 – –	 % %
Output amplifier sensitivity	–	1.5	–	µV/e^-
Readout noise at 253 K (see note 4)	–	4	6	rms e^-/pixel
Readout frequency (see note 5)	–	20	5000	kHz
Response non-uniformity (std. deviation)	–	3	–	% of mean
Dark signal non-uniformity at 293 K (std. deviation)	–	100	200	e^-/pixel/s
Output node capacity relative to image section	–	2.0	–	

PERFORMANCE

Electrode capacitances (measured at mid-clock level):

	Min	Typical	Max	
IØ/IØ interphase	–	2.0	–	nF
RØ/RØ interphase	–	70	–	pF
IØ/SS	–	6	–	nF
RØ/SS	–	185	–	pF
Output impedance	–	300	–	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 and 300 K is given by:

   Qd/Qd0 = 1.14 x 106T3e79080/T

   Where Q_{d0} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant
3. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
4. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 ms integration period
5. Readout above 5000 kHz can be achieved but performance to the parameters given cannot be guaranteed

BLEMISH SPECIFICATION

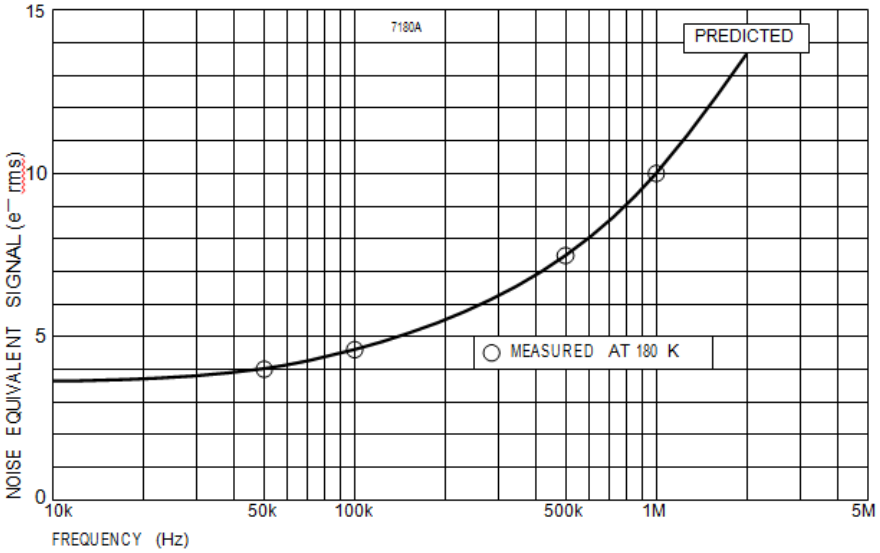
Traps	Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 253 K
Slipped columns	Are counted if they have an amplitude greater than 200 e^-
Black Spots	Are counted when they have a responsivity of less than 90% of the local mean signal illuminated at approximately half saturation
White Spots	Are counted when they have a generation rate 100 times the specified maximum dark signal generation rate at 293 K (measured between 233 and 273 K). The typical temperature dependence of white spot blemishes is different from that of the average dark signal and is given by: $Q_d/Q_{d0} = 122T^3e^{-6400/T}$
White Column	A column which contains at least 9 white defects.
Black Column	A column which contains at least 9 black defects

Grade	0	1	2
Column defects:			
black or slipped	0	1	6
white	0	0	0
Black spots:			
<3 pixels	1	2	8
3 – 5 pixels	1	1	4
6 – 10 pixels	0	0	1
>10 pixels	0	0	0
Traps >200 e^-	1	2	5
White spots	6	10	15

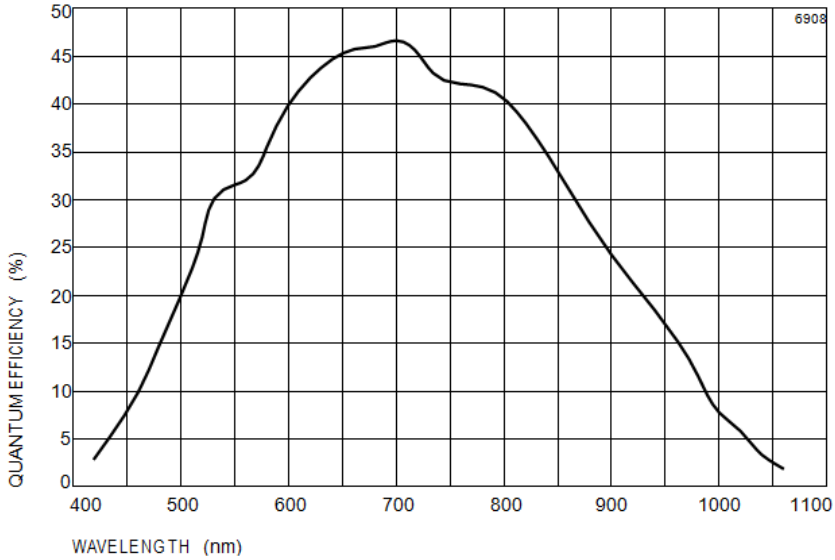
Minimum separation between
adjacent black columns …….. 50 pixels

Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

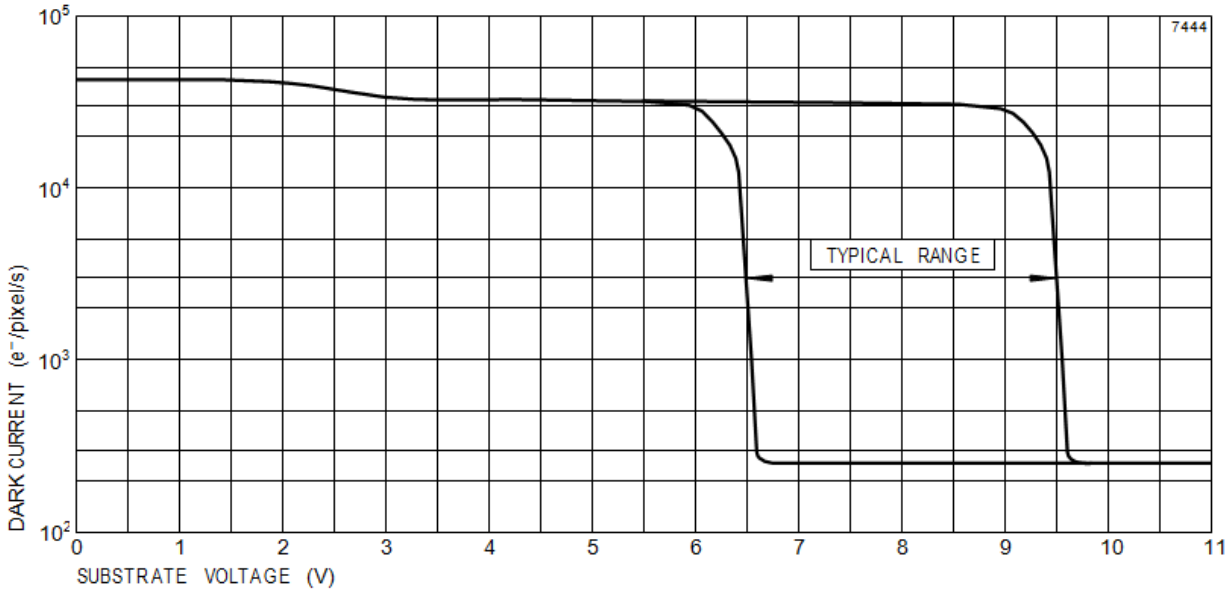
TYPICAL OUTPUT CIRCUIT NOISE (measured using clamp and sample)



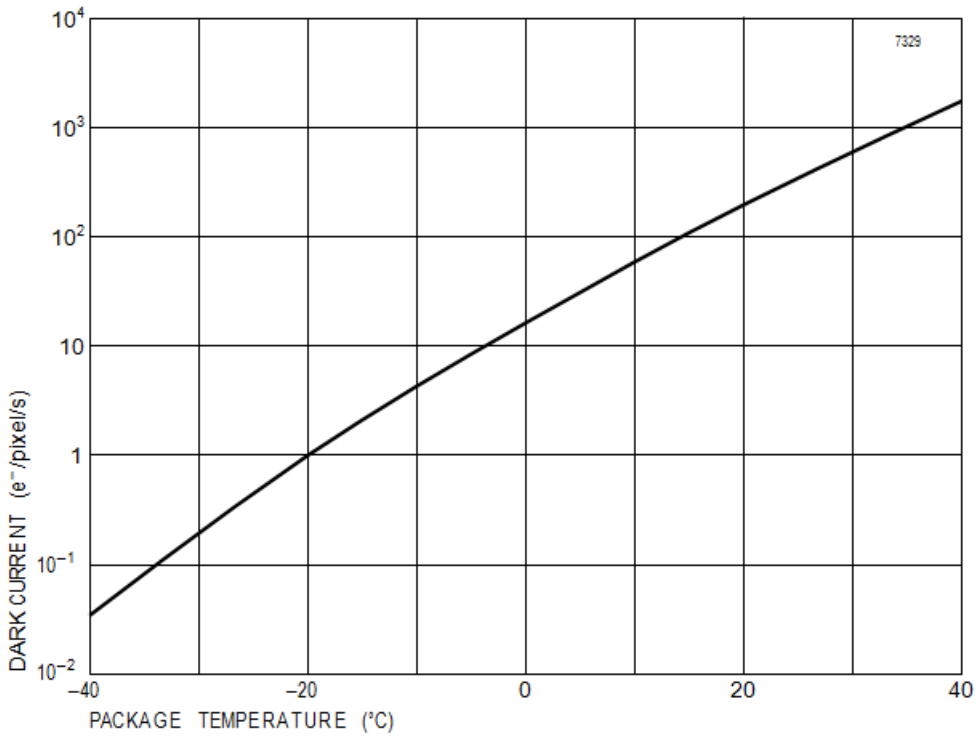
TYPICAL SPECTRAL RESPONSE (No window)



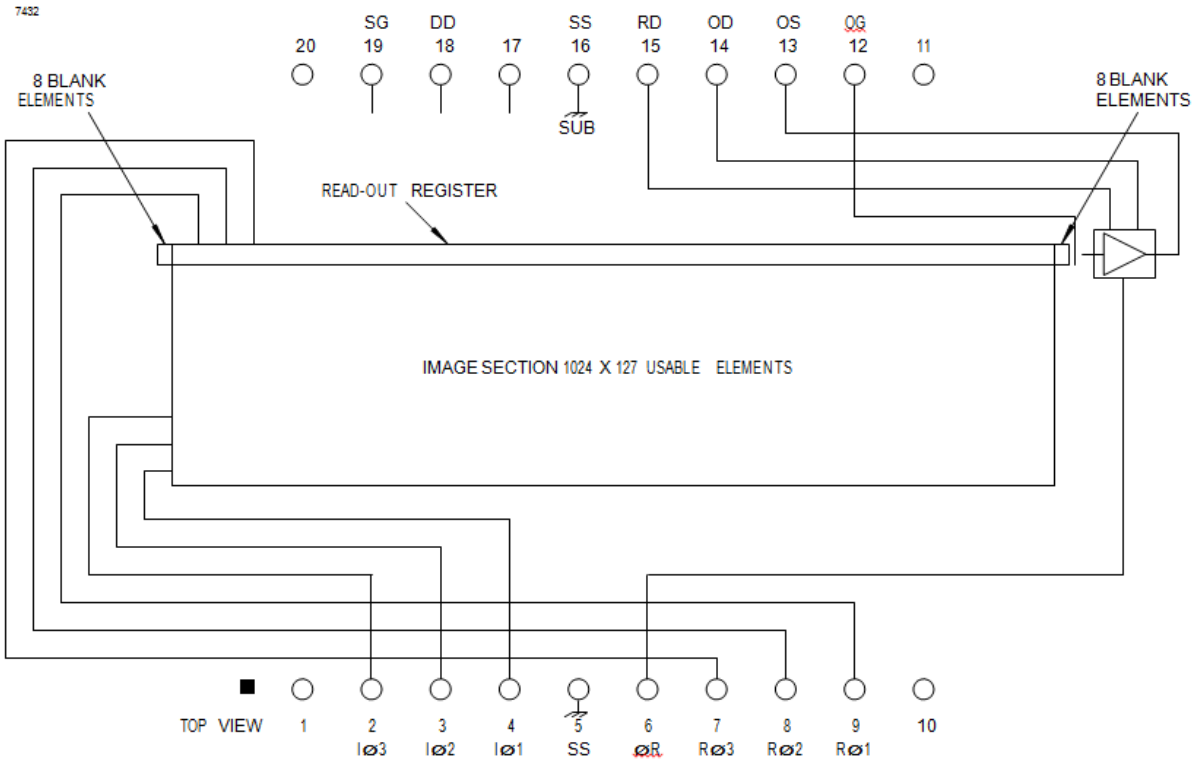
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



DEVICE SCHEMATIC

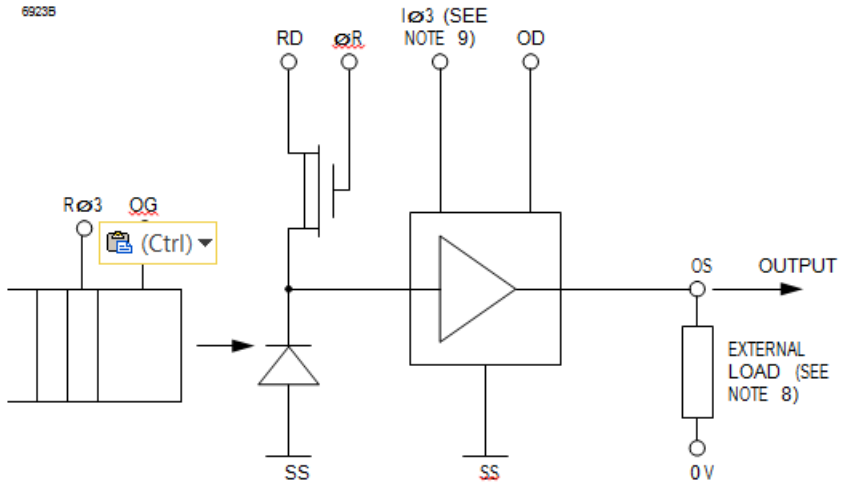


CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 6) Min	Typical	Max	MAXIMUM RATINGS with respect to V_{SS}
1	–	No connection		–		–
2	IØ3	Image section, phase 3 (clock pulse)	10	12	15	±20 V
3	IØ2	Image section, phase 2 (clock pulse)	10	12	15	±20 V
4	IØ1	Image section, phase 1 (clock pulse)	10	12	15	±20 V
5	SS	Substrate	8	9.5	11	–
6	ØR	Output reset pulse	10	12	15	±20 V
7	RØ3	Readout register, phase 3 (clock pulse)	10	12	15	±20 V
8	RØ2	Readout register, phase 2 (clock pulse)	10	12	15	±20 V
9	RØ1	Readout register, phase 1 (clock pulse)	10	12	15	±20 V
10	–	No connection		see note 7		–
11	–	No connection		see note 7		–
12	OG	Output gate	2	3.5	5	±20 V
13	OS	Output transistor source		see note 8		-0.3 to +25 V
14	OD	Output drain	27	29	32	−0.3 to +25 V
15	RD	Reset transistor drain	17	18	19	−0.3 to +25 V
16	SS	Substrate	8	9.5	11	–
17	–	No connection		–		–
18	DD	Diode drain	20	22	25	−0.3 to +25 V
19	SG	Spare gates	0	0	V_{SS}+19	±20 V
20	–	No connection		–		–

If all voltages are set to the 'typical' values, operation at or close to specification should be obtained. Some adjustment within the minimum – maximum range specified may be required to optimise performance.
Voltage between pairs of pins: OS to OD + 15 V.
Maximum current through any source or drain pin: 10 mA

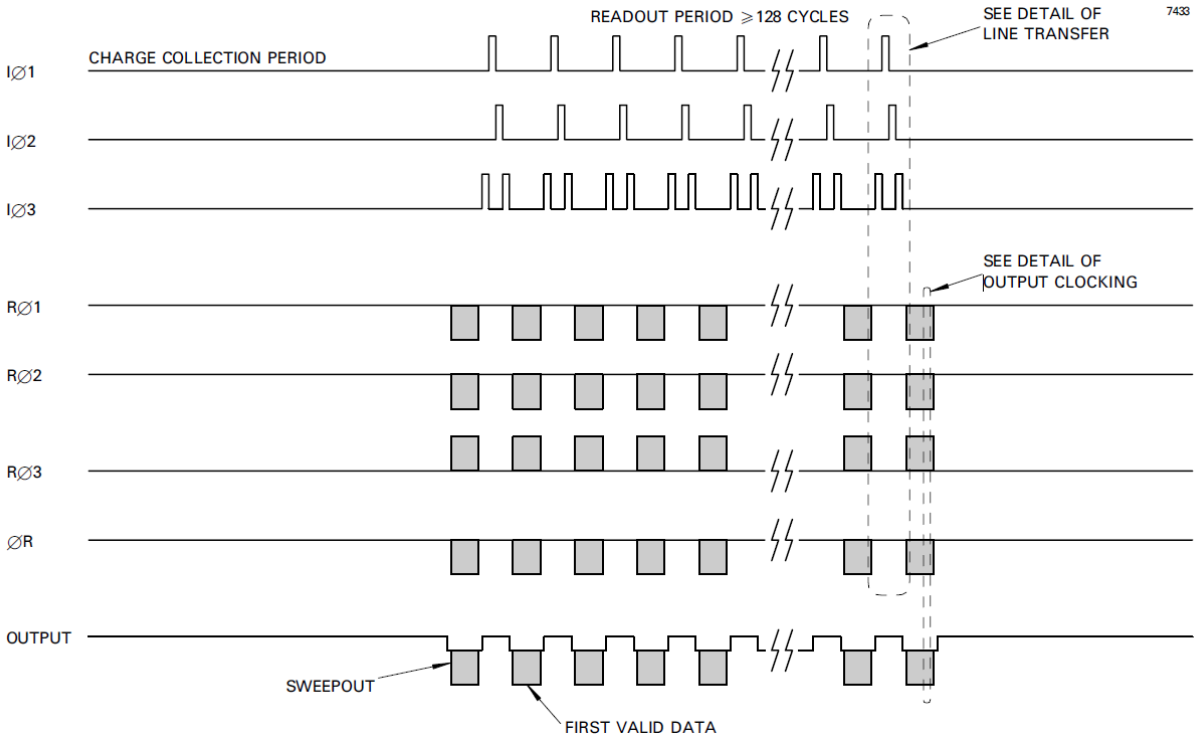
OUTPUT CIRCUIT



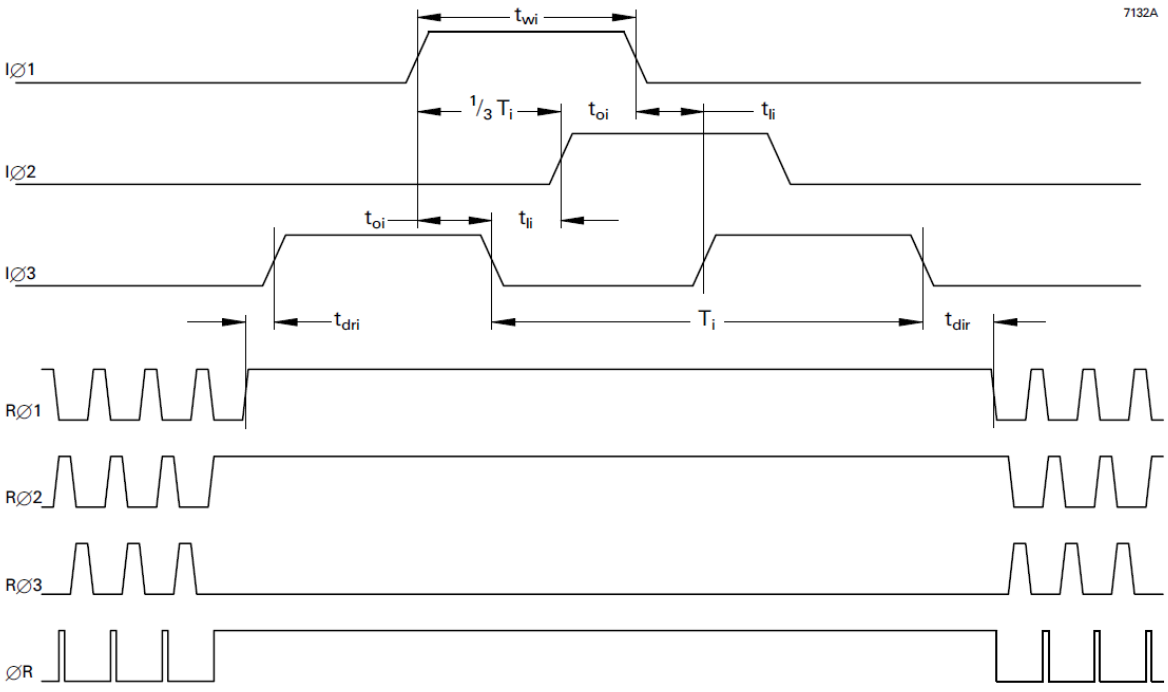
Notes (Cont'd)

6. Image clock pulse low levels 0 ± 0.5 V; other clock low levels +1 V.
7. There are no temperature sensing diodes in the CCD40-11.
8. Not critical; can be a 1 – 5 mA constant current source, or 5 – 10 kΩ resistor.
9. The amplifier has a DC restoration circuit, which is activated internally whenever Iø3 is pulsed high.

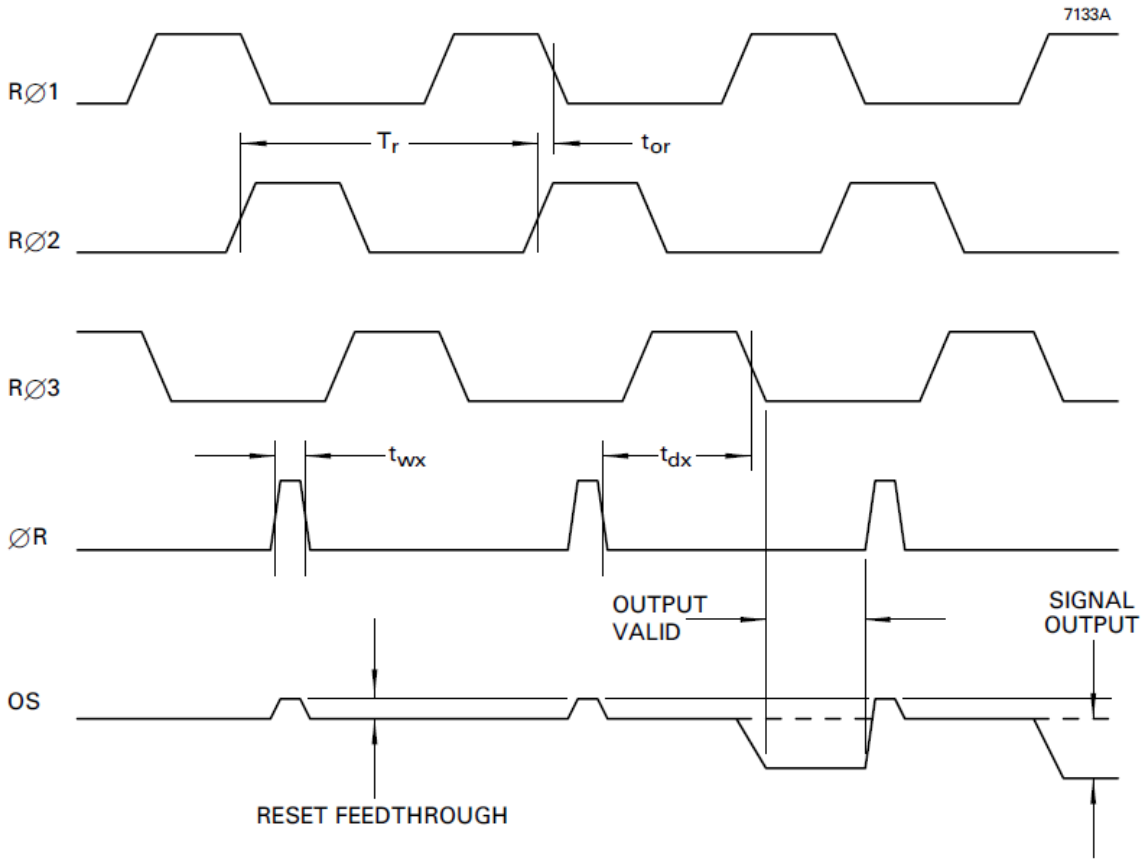
FRAME READOUT TIMING DIAGRAM



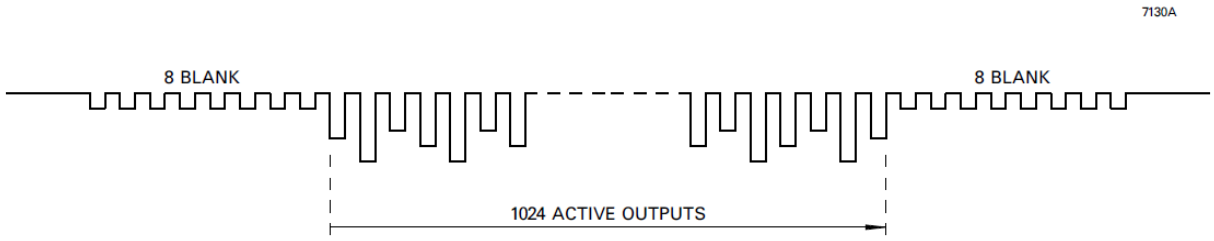
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



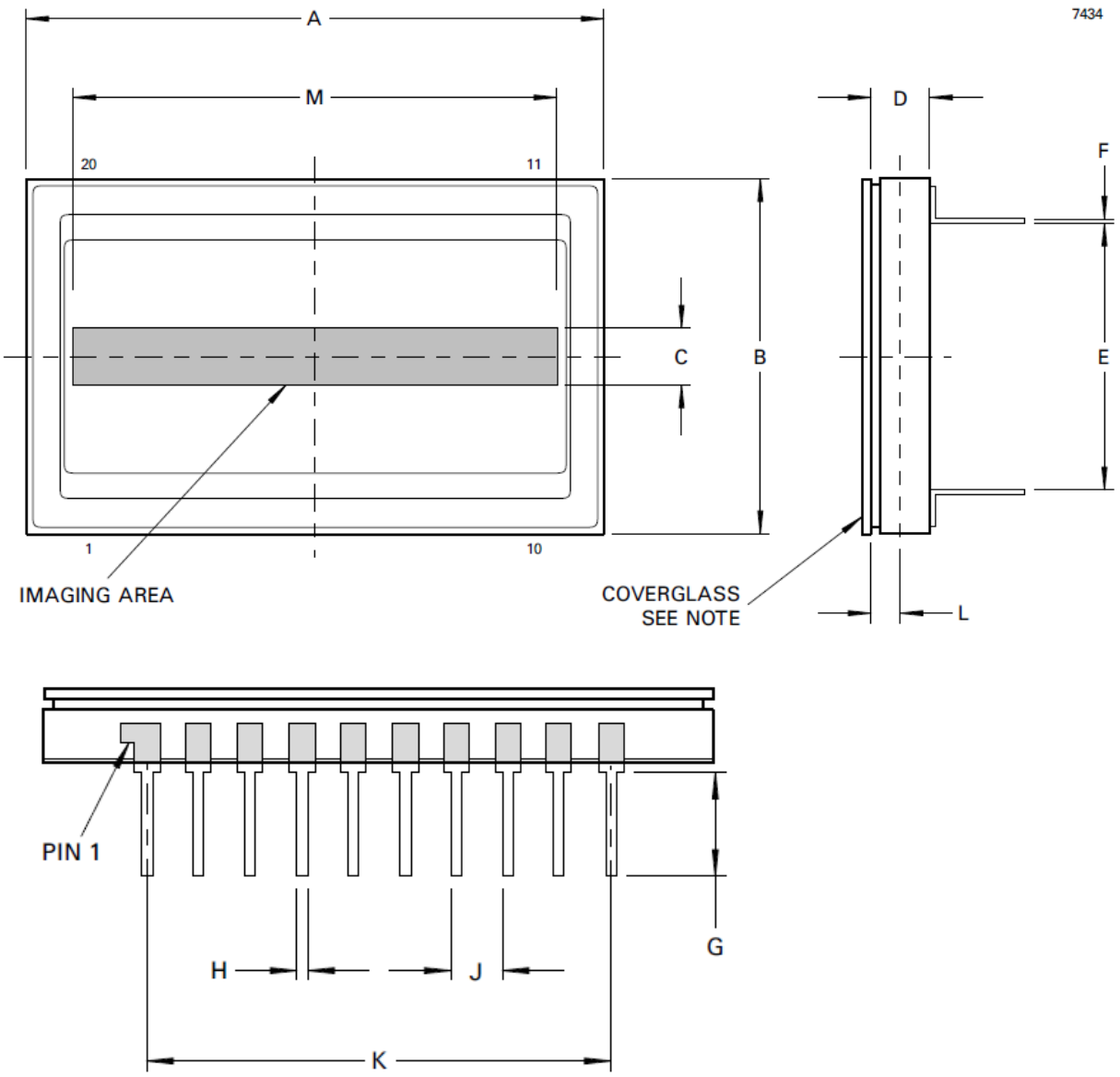
CLOCKING TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	15	30	see note 10	ms
t_{wi}	Image clock pulse width	7	15	see note 10	ms
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	2	$0.5t_{oi}$	ms
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	2	$0.5t_{oi}$	ms
t_{oi}	Image clock pulse overlap	3	5	$0.2T_i$	ms
t_{li}	Image clock pulse, two phase low	2	5	$0.2T_i$	ms
t_{dir}	Delay time, I1 stop to R1 start	3	5	see note 10	ms
t_{dri}	Delay time, R1 stop to I1 start	1	2	see note 10	ms
T_r	Output register clock cycle period	200	see note 11	see note 10	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, 1R low to R13 low	30	$0.5T_r$	$0.8T_r$	ns

Notes (Cont'd)

10. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
11. As set by the read out period.

OUTLINE (All dimensions without limits are nominal)



Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required

Ref	Millimetres
A	32.89 ± 0.38
B	20.07 ± 0.25
C	3.3
D	3.30 ± 0.33
E	15.24± 0.25 ± 0.051
F	0.254 -0.025
G	5.2
H	0.46 ± 0.05
J	2.54 ± 0.13
K	22.86 ± 0.13
L	1.65 ± 0.56
M	26.6

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window

For further information on the performance of these and other options, please contact Teledyne e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 104 rads.
Certain characterisation data are held at Teledyne e2v. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	-	373	K
Operating	73	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage

Maximum device heating/cooling 5 K/Min