CCD290-99 Back Illuminated Scientific CCD Sensor
9216 x 9232 Pixels, Sixteen Outputs
Non-inverted Mode Operation

INTRODUCTION

The CCD290 extends e2v's family of scientific CCD sensors and has been designed to provide a large image area for demanding astronomical and scientific imaging applications. Back-illuminated spectral response combined with very low read-out noise give exceptional sensitivity.

DESCRIPTION

The sensor has an image area having 9216 × 9232 pixels with registers at both top and bottom each with eight outputs for short read-out times. The pixel size is 10 μm square. The image area has two separately connected sections to allow full-frame or split full-frame read-out modes. Depending on the mode, the read-out can be through 8 or 16 of the output circuits. A fixed-barrier dump drain is also provided to allow fast dumping of unwanted data.

The output amplifier is designed to give very low noise at read-out rates of up to 3 MHz. The low output impedance simplifies the interface with external electronics and the optional dummy outputs are provided to facilitate common mode rejection.

The package provides a compact footprint with guaranteed flatness at cryogenic temperatures. Connections are made at the top and bottom of the device via two flexi connectors that also provide a thermal break. The sides may be close butted if needed.

Specifications are tested and guaranteed at 173K (–100 °C).

The CCD290 is a non-inverted (non-MPP) type.

VARIANTS

Standard silicon and deep-depletion silicon device types can be supplied with a range of AR coatings. Graded coatings and two-layer coatings are available as custom variants.

Devices with other formats (e.g. 4608 × 4608, or 6144 × 6144 pixels) or fewer outputs (4 or 8) may also be available to custom order.

Consult e2v technologies for further information on any of the above options.

SUMMARY PERFORMANCE (Typical)

Number of pixels	9216 (H) × 9232 (V)
Pixel size	10 μm square
Image area	92.2 mm × 92.4 mm
Outputs	16
Package size	98.5 × 93.7 mm
Package format	Silicon carbide with two flexi connectors
Focal plane height, above base	20.0 mm
Connectors	Two 51-way micro-D
Flatness	20 μm (peak to valley)
Amplifier sensitivity	7.5 μV/e^-
Read-out noise	4 e^- at 0.5 MHz 2.5 e^- at 50 kHz
Maximum pixel data rate	3 MHz
Charge storage (pixel full well)	90,000 e^-
Dark signal	4 e^-/pixel/hour (at –100 °C)

Quoted performance parameters given here are "typical" values. Specification limits are shown later.

Part References

CCD290-99-g-xxx

g = cosmetic grade
xxx = device-specific part number

CCD290-99-1-F24 Grade-1, deep depletion, astro multi-2

CCD290-99-1-F81 Grade-1, deep depletion, astro multi-7

CCD290-99-1-F82 Grade-1, standard silicon, astro multi-2

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PERFORMANCE SPECIFICATIONS

Parameter	Typical	Grade 0 and 1		Grade 2			
		Min	Max	Min	Max	Units	Note
Peak charge storage (image pixel)	90,000	70,000	-	60,000	-	e^-/pixel	2(a)
Peak charge storage (register SW)	140,000	-	-	-	-	e^-/pixel	2(b)
Output node capacity: OG low mode 1 (not factory tested) OG high mode 2 (not factory tested)	 240,000 700,000	 - -	 - -	 - -	 - -	 e^- e^-	2(c)
Output amplifier responsivity: mode 1 mode 2 (not factory tested)	 7.5 2.5	 5.5 -	 - -	 5.0 -	 - -	 μV/e^- μV/e^-	3
Non-linearity	0.5	-1.5	+1.5	-3.0	+3.0	%	
Read-out noise 50 kHz (not factory tested) 500 kHz	 2.5 4	 -	 - 7	 -	 - 10	e^- rms	4
Dark signal: at 173 K at 153 K	 4 0.02	 - -	 - 2.0	 - -	 - 4.0	 e^-/pixel/hr e^-/pixel/hr	5
Charge transfer efficiency: parallel serial	 99.9995 99.9995	 99.9990 99.9990	 - -	 99.9985 99.9985	 - -	 % %	6
Flatness peak-to-valley	20	-	30	-	50	μm	7
Focal plane package height	20.000	19.985	20.015	19.970	20.030	mm	7

NOTES

1. Device electro-optical performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency of approximately 0.1 – 1.0 MHz. Acceptance tests are performed at 173K and at a nominal 500 kHz pixel rate.
2. (a) Signal level at which resolution begins to degrade. Device is non-inverted (NIMO/non-MPP), for maximum full well.

   (b) The summing well capacity limits the charge in the register. The limiting value may change in mode-2 but is not tested.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown.
3. Under normal operation (mode 1), SW is operated as a summing well or clocked as RØ3. OG is biased at a low DC level.

   Alternatively (mode 2), SW may be operated as an output gate (and not therefore available for summing) and biased at a low DC level with OG raised to a high voltage (see note 9 later). This gives more charge-handling capacity (e.g. for higher level pixel binning). Charge transfer to the output now occurs as RØ2 goes low. In mode-2, the output noise will also increase by a factor of three. Mode-2 is not factory tested.
4. Noise is specified and measured using correlated double sampling at 500 kHz nominal read-out rate in mode 1 only. Performance at 50 kHz is also indicated (but not production-tested). Noise (as with all factory test images) is measured with differential readout, i.e. with the dummy output. The noise value reported is a single ended equivalent value with no dummy, by dividing by the $\sqrt{2}$ factor that arises from the differential subtraction. This way test system induced noise is reduced.
5. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.

   Note that this is typical performance and some variation may be seen between devices.
6. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase)
7. Mechanical parameters are measured at room temperature. The flatness measured at room temperature is extrapolated to a value at 173K based on modelling results.

SPECTRAL RESPONSESPECIFICATIONS

The table below gives guaranteed minimum values of the spectral response for several variants. PRNU is also shown.

Default Coatings

	DD silicon Astro Multi-2	Standard silicon Astro Multi-2	Pixel Response Non-Uniformity PRNU (1 σ)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Maximum PRNU (%)**
350	30	30	-
400	75	75	3
500	75	75	-
650	80	80	3
900	50	25	5

Alternative Coatings (may not be readily available)

	DD silicon Astro Broadband	DD silicon Astro Midband	DD silicon Astro ER1	DD silicon Astro Multi-7	Standard silicon Astro Broadband	Standard silicon Astro Broadband	Standard silicon Astro Midband	Pixel Response Non-Uniformity PRNU (1 σ)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Maximum PRNU (%)**
350	40	20	20	-	40	40	20	-
400	70	50	35	45	70	70	50	3
500	75	80	65	75	80	80	80	-
650	70	80	80	80	75	75	80	3
900	40	40	45	50	25	25	25	5

SPECTRAL RESPONSE NOTES

a) The above specifications are for grades 0 and 1 devices. Grade 2 device specifications are 5% absolute lower for guaranteed QE minimum values and 1% absolute higher for guaranteed PRNU maximum values.

b) Standard silicon has a nominal active thickness of 16 μm. DD is Deep Depletion silicon with a higher resistivity and a nominal active thickness of 40 μm.

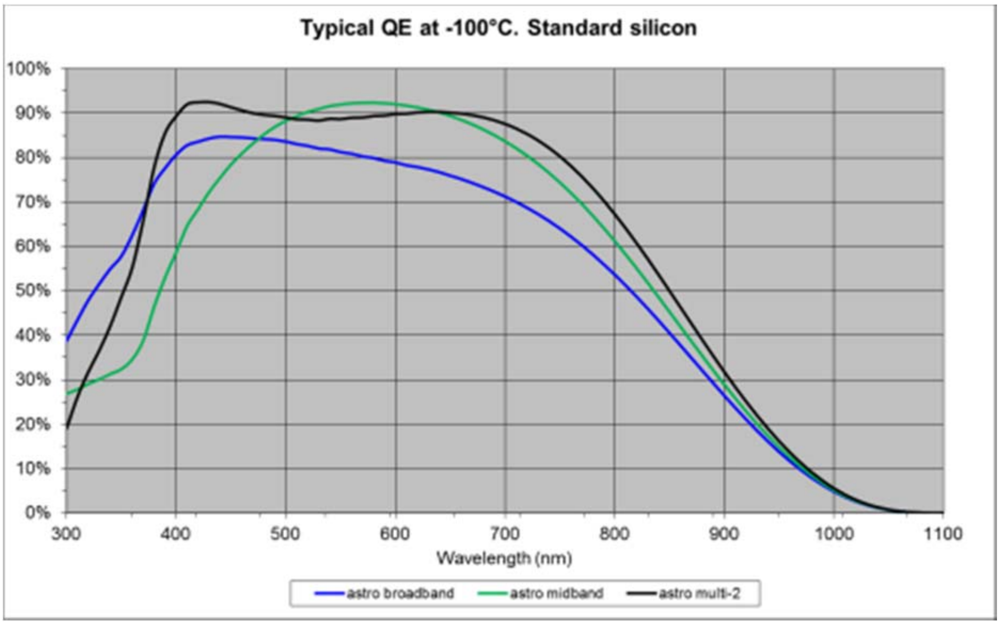
c) The multi-7 coating is designed specifically for the 500 to 1000 nm region; it has lower reflectivity (and fringing) than the multi-2 coating at the longest wavelengths.

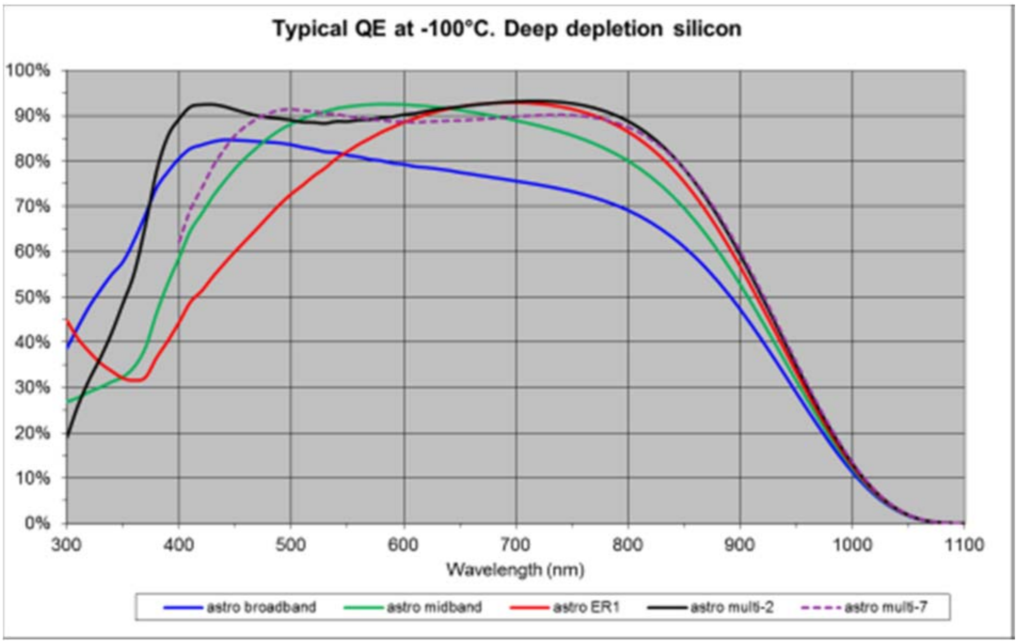
d) The availability of coatings varies depending on type; check with factory.

e) Devices with alternative or custom spectral response may be available by special request. Consult e2v technologies.

See also the typical spectral response figures below.

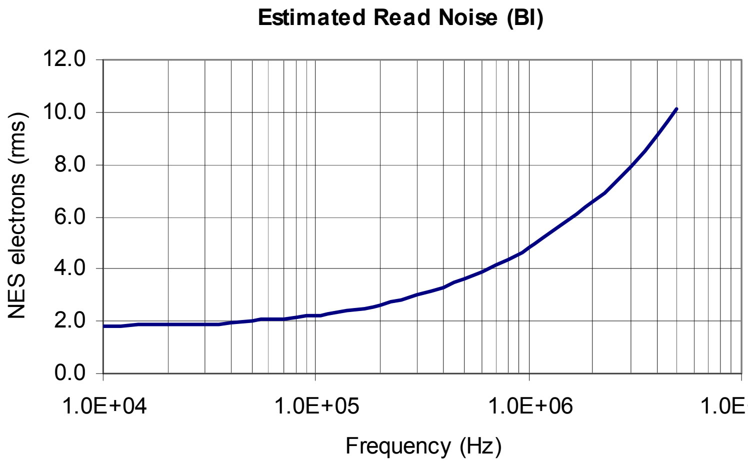
TYPICAL SPECTRAL RESPONSE CURVES





TYPICAL AMPLIFIER READ NOISE

The modelled variation of typical output amplifier read noise with operating frequency is shown below. This assumes correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1, temperature range 150 – 230 K



GRADE DEFINITIONS AND COSMETIC SPECIFICATIONS

Maximum allowed cosmetic defect levels are indicated below.

	Guaranteed Specifications			Typical Values		
Grade	**0**	**1**	**2**	**0**	**1**	**2**
Column defects - black or white	15	30	40	<5	<10	<20
White spots	1500	3000	4500	<1000	<2000	<3000
Total (black & white) spots	4000	8000	12000	<2000	<4000	<6000
Traps > 200e-	20	30	40	<10	<20	<30

Grade 1: Grade 1 is the default grade for general science use; contact the factory for upgrade to grade-0.

Grade 2: Contact the factory for availability of grade 2 devices. They are generally not made to order but may be available from time to time to be supplied as lower grade imaging devices.

Grade 5: Grade 5 devices are classed as electrical models only and as such have no performance guarantees. The will generally be supplied with all 16 outputs confirmed as operating ‘nominally’ but have no image quality guarantee. Any other test data measured will be supplied for information only.

Grade 6: Grade 6 is a mechanical model. These are not electrically functioning but do have representative mechanical parameters.

DEFECT DEFINITIONS

For cosmetic defect analysis, all image pixels are clocked to register E/F and read out using outputs OS1 to OS8 only.

Defect in Darkness Bright/White Spots	A defect in darkness is a pixel with dark generation rate ≥ 5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 5 above.
PR Defect	A PR defect dark spot is a pixel with a photo-response outside ≤ 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 400 bright or dark single pixel defects. Each defective column is only counted once.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^- at the specified test temperature.
Defect exclusion zone	Defect measurements are excluded from the outer two rows of the sensor.

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DEFINITIONS

Back-Thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (which can be particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is "passivated" and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Read-out Noise

Read-out noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated "dummy" circuit on-chip, which is of identical design to the "real" circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the "real" signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 6.

Correlated Double Sampling

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

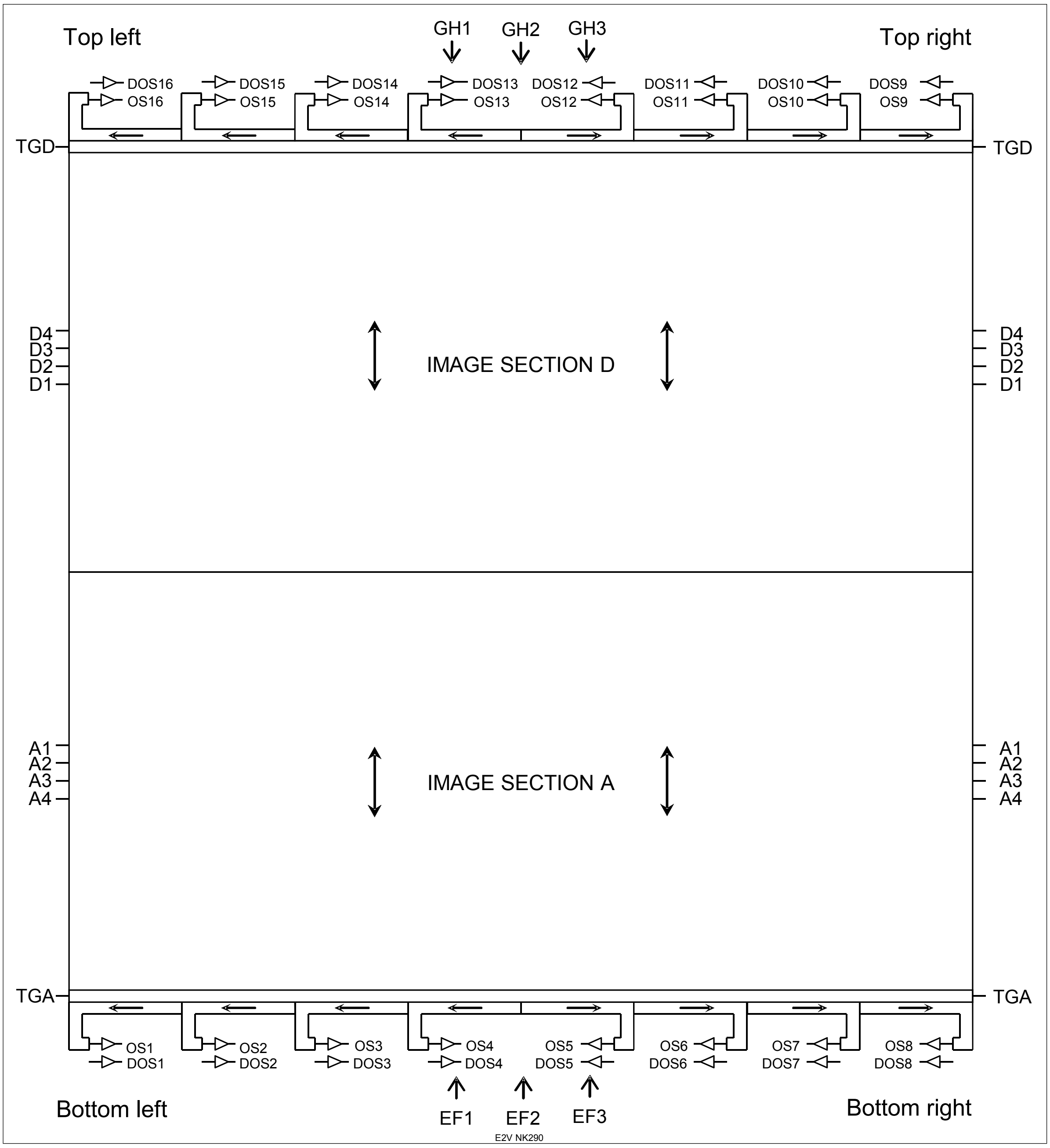
Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

ARCHITECTURE

Chip Schematic

TOP



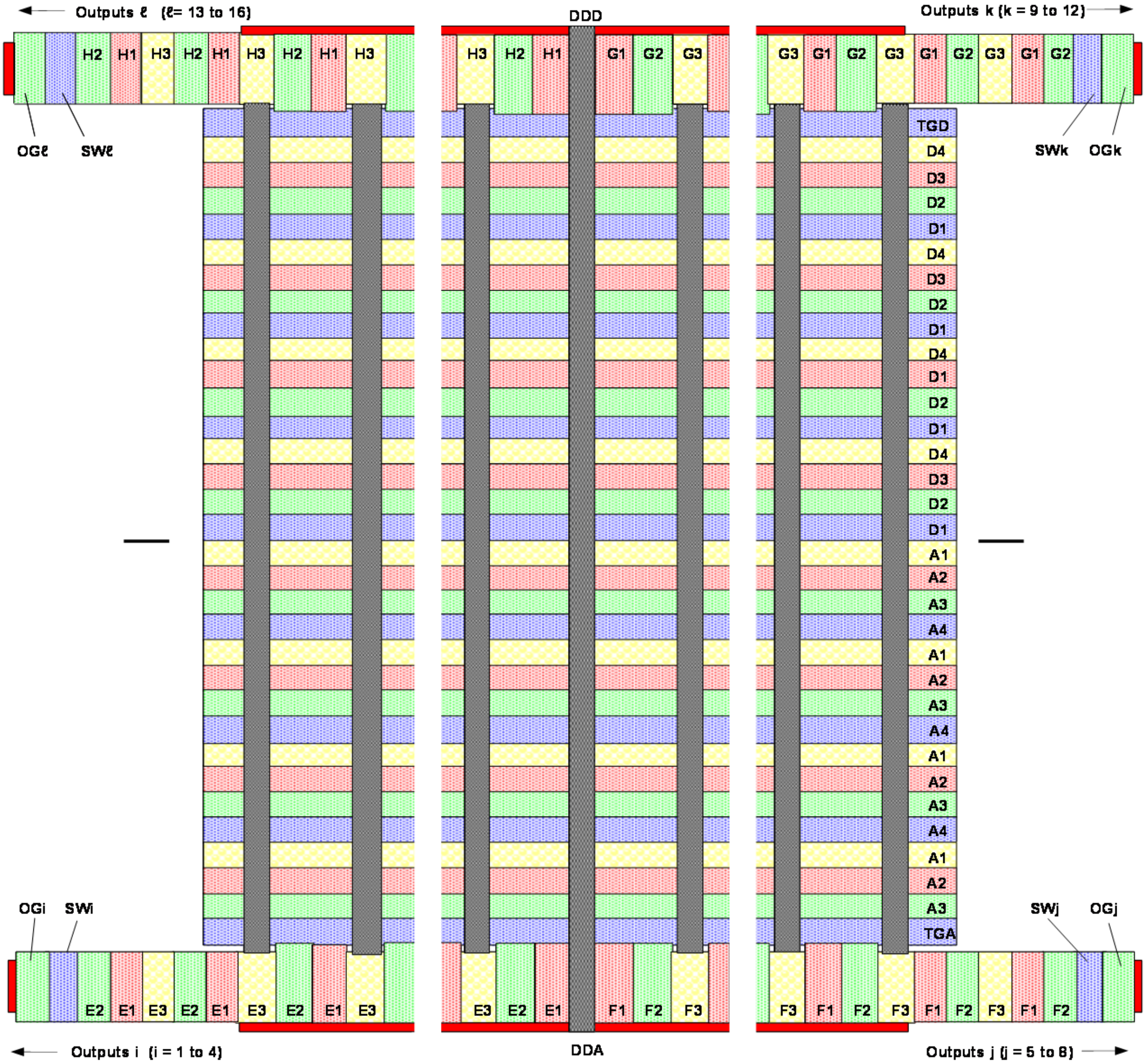
BOTTOM

Image sections A and D each have a total of 9216 (H) × 4616 (V) pixels.

Each register section has a total of 1179 elements: 1152 active and 27 pre-scan.

Connector-1 (and flexi) is at the "bottom" of the device (register EF); Connector-2 is at the "top" of the device (register GH).

ARRANGEMENT OF ELECTRODES

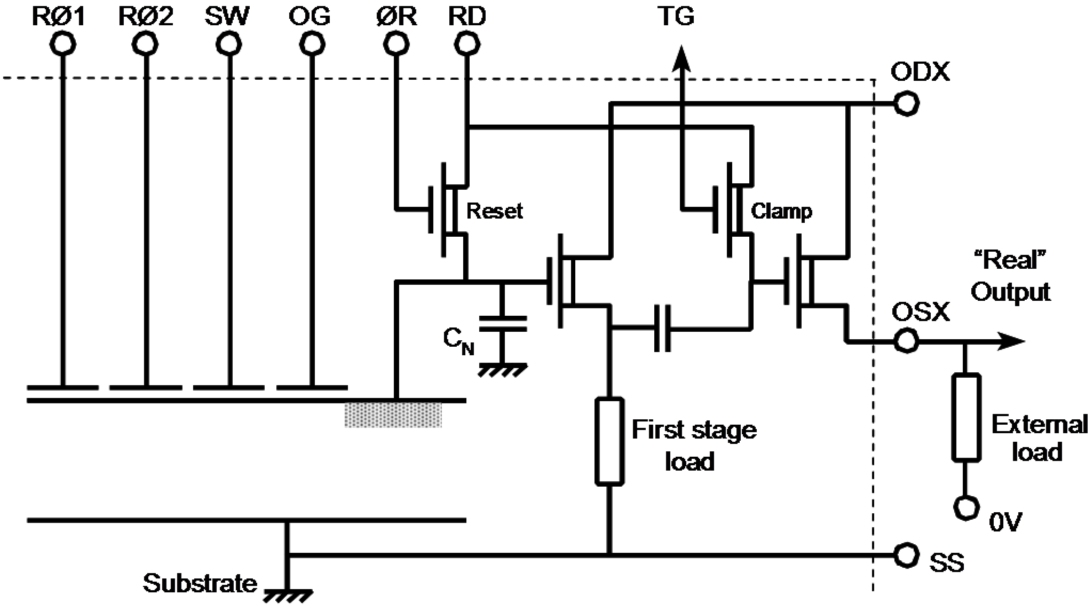


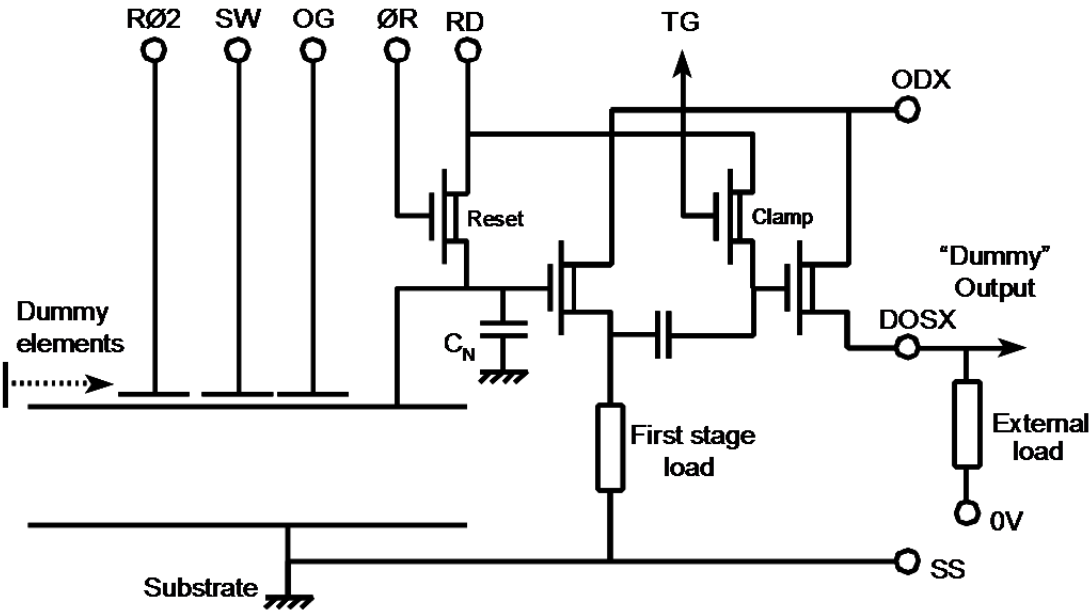
Pre-scan (blank) serial elements are not shown here.

Each output consists of real (OS) and dummy (DOS); see next page.

OUTPUT CIRCUIT

X designates a specific output, namely 1 to 16 (see the chip schematic).





The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.2 mA via SS.

The output circuit consists of two capacitor-coupled source-follower stages. The particular design has a very high responsivity to give lowest noise. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

The amplifier output impedance is typically 400 Ω.

ELECTRICAL INTERFACES

CONNECTOR 1

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (See note 10)			MAX RATINGS (V) with respect to V_{SS}
			Min	Typical	Max	
1	A1	Image Area A Clock Phase 1	9	11	12	±20
2	A2	Image Area A Clock Phase 2	9	11	12	±20
3	TGA	Image Area A Transfer gate	9	11	12	±20
4	OD1	Output Drain 1	25	29	31	-0.3 to +35
5	OS1	Output Source 1		(see note 8)		
6	OD2	Output Drain 2	25	29	31	-0.3 to +35
7	OS2	Output Source 2		(see note 8)		
8	OD3	Output Drain 3	25	29	31	-0.3 to +35
9	OS3	Output Source 3		(see note 8)		
10	OD4	Output Drain 4	25	29	31	-0.3 to +35
11	OS4	Output Source 4		(see note 8)		
12	SS	Substrate (see note 11)	0	0	10	N/A
13	ØRA	Reset Gate (A) (See note 12)	9	12	13	±20
14	SWA	Summing Well (A) (See note 9)	9	10	12	±20
15	SS	Substrate (see note 11)	0	0	10	N/A
16	OS5	Output Source 5		(see note 8)		
17	OD5	Output Drain 5	25	29	31	-0.3 to +35
18	OS6	Output Source 6		(see note 8)		
19	OD6	Output Drain 6	25	29	31	-0.3 to +35
20	OS7	Output Source 7		(see note 8)		
21	OD7	Output Drain 7	25	29	31	-0.3 to +35
22	OS8	Output Source 8		(see note 8)		
23	OD8	Output Drain 8	25	29	31	-0.3 to +35
24	TGA	Image Area A Transfer Gate	9	11	12	±20
25	A2	Image Area A Clock Phase 2	9	11	12	±20
26	A1	Image Area A Clock Phase 1	9	11	12	±20
27	A3	Image Area A Clock Phase 3	9	11	12	±20
28	A4	Image Area A Clock Phase 4	9	11	12	±20
29	RD1/2	Reset Drain (1/2)	16	17	19	-0.3 to +25
30	DOS1	Dummy Output Source 1		(see note 8)		
31	SS	Substrate (see note 11)	0	0	10	N/A
32	DOS2	Dummy Output Source 2		(see note 8)		
33	RD 3/4	Reset Drain (3/4)	16	17	19	-0.3 to +25
34	DOS3	Dummy Output Source 3		(see note 8)		
35	SS	Substrate (see note 11)	0	0	10	N/A
36	DOS4	Dummy Output Source 4		(see note 8)		
37	OGA	Output Gate (A) (See note 9)	1	2	(note 9)	±20
38	E3/F3	Register E & Register F Clock Phase 3	9	10	12	±20
39	E2/F2	Register E & Register F Clock Phase 2	9	10	12	±20
40	E1/F1	Register E & Register F Clock Phase 1	9	10	12	±20
41	DDA	Dump Drain (A) (See note 13)	15	18	20	-0.3 to +35
42	DOS5	Dummy Output Source 5		(see note 8)		
43	SS	Substrate (see note 11)	0	0	10	N/A
44	DOS6	Dummy Output Source 6		(see note 8)		
45	RD5/6	Reset Drain (5/6)	16	17	19	-0.3 to +25
46	DOS7	Dummy Output Source 7		(see note 8)		
47	SS	Substrate (see note 11)	0	0	10	N/A
48	DOS8	Dummy Output Source 8		(see note 8)		
49	RD7/8	Reset Drain (7/8)	16	17	19	-0.3 to +25
50	A4	Image Area A Clock Phase 4	9	11	12	±20
51	A3	Image Area A Clock Phase 3	9	11	12	±20

CONNECTOR 2

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (See note 10)			MAX RATINGS (V) with respect to V_{SS}
			Min	Typical	Max	
1	D4	Image Area D Clock Phase 4	9	11	12	±20
2	D3	Image Area D Clock Phase 3	9	11	12	±20
3	TGD	Image Area D Transfer gate	9	11	12	±20
4	OD9	Output Drain 9	25	29	31	-0.3 to +35
5	OS9	Output Source 9		(see note 8)		
6	OD10	Output Drain 10	25	29	31	-0.3 to +35
7	OS10	Output Source 10		(see note 8)		
8	OD11	Output Drain 11	25	29	31	-0.3 to +35
9	OS11	Output Source 11		(see note 8)		
10	OD12	Output Drain 12	25	29	31	-0.3 to +35
11	OS12	Output Source 12		(see note 8)		
12	SS	Substrate (see note 11)	0	0	10	N/A
13	ØRD	Reset Gate (D) (See note 12)	9	12	13	±20
14	SWD	Summing Well (D) (See note 9)	9	10	12	±20
15	SS	Substrate (see note 11)	0	0	10	N/A
16	OS13	Output Source 13		(see note 8)		
17	OD13	Output Drain 13	25	29	31	-0.3 to +35
18	OS14	Output Source 14		(see note 8)		
19	OD14	Output Drain 14	25	29	31	-0.3 to +35
20	OS15	Output Source 15		(see note 8)		
21	OD15	Output Drain 15	25	29	31	-0.3 to +35
22	OS16	Output Source 16		(see note 8)		
23	OD16	Output Drain 16	25	29	31	-0.3 to +35
24	TGD	Image Area D Transfer Gate	9	11	12	±20
25	D3	Image Area D Clock Phase 3	9	11	12	±20
26	D4	Image Area D Clock Phase 4	9	11	12	±20
27	D2	Image Area D Clock Phase 2	9	11	12	±20
28	D1	Image Area D Clock Phase 1	9	11	12	±20
29	RD9/10	Reset Drain (9/10)	16	17	19	-0.3 to +25
30	DOS9	Dummy Output Source 9		(see note 8)		
31	SS	Substrate (see note 11)	0	0	10	N/A
32	DOS10	Dummy Output Source 10		(see note 8)		
33	RD11/12	Reset Drain (11/12)	16	17	19	-0.3 to +25
34	DOS11	Dummy Output Source 11		(see note 8)		
35	SS	Substrate (see note 11)	0	0	10	N/A
36	DOS12	Dummy Output Source 12		(see note 8)		
37	OGD	Output Gate (D) (See note 9)	1	2	(note 9)	±20
38	G3/H3	Register G & Register H Clock Phase 3	9	10	12	±20
39	G1/H1	Register G & Register H Clock Phase 1	9	10	12	±20
40	G2/H2	Register G & Register H Clock Phase 2	9	10	12	±20
41	DDD	Dump Drain (D) (See note 13)	15	18	20	-0.3 to +35
42	DOS13	Dummy Output Source 13		(see note 8)		
43	SS	Substrate (see note 11)	0	0	10	N/A
44	DOS14	Dummy Output Source 14		(see note 8)		
45	RD13/14	Reset Drain (13/14)	16	17	19	-0.3 to +25
46	DOS15	Dummy Output Source 15		(see note 8)		
47	SS	Substrate (see note 11)	0	0	10	N/A
48	DOS16	Dummy Output Source 16		(see note 8)		
49	RD15/16	Reset Drain (15/16)	16	17	19	-0.3 to +25
50	D1	Image Area D Clock Phase 1	9	11	12	±20
51	D2	Image Area D Clock Phase 2	9	11	12	±20

NOTES

8. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

   For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

9. Default operation (mode 1) shown with OG set to OG-Low, with a +2 V nominal value. In this mode SW may be clocked as RØ3 if a summing well function is not required. OG-Low should have a maximum value of +5 V.

   For alternative operation in a low responsivity mode (mode 2) with increased charge handling, OG should be set to OG-High and SW should be operated as OG-Low (i.e. 2V typical). See below for appropriate OG-High values. Charge is now read out as RØ2 goes low.

   See note 11 also for discussion about Substrate voltage (Vss). With high substrate voltage OG-High may be set to a nominal +20 V, which offers best linearity in mode-2. With low substrate voltage, the allowed maximum value of OG-High is limited to a nominal +18 V; the lower OG-High value has a greater non-linearity.

10. To ensure that any device can be operated the camera should be designed so that any value in the range "min" to "max" can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    For the clock pulses, the high levels are shown in the table. The image clock low is set to 0 V . The register and SW clock low levels are +1 V. Reset clock low is set to 0 V.

    In all cases, specific recommended settings will be supplied with each science-grade sensor.

11. The substrate voltage (Vss) has a default value of 0 V ("low" substrate). This is particularly recommended for deep-depletion device variants, since it optimises depletion depth for best Point Spread Function. Devices may alternatively be operated at "high" substrate, with Vss = 9 V. The high substrate setting offers slightly lower dark current, although this is usually not of primary concern when the device is cryogenically cooled. See also note 19 below, referring to Vss level as prior to readout.

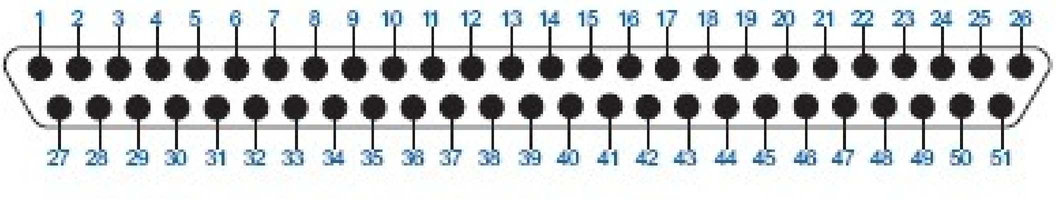
    The substrate setting has some consequence for the allowed OG upper voltage level, as discussed in note 9.

12. Standard silicon variants are expected to be used with ØR at +10 V or more; deep depletion variants require at least +12 V. A higher value will give a correspondingly higher reset feed-through signal in the device output (OS).

13. The DD function may change in future versions. Consult factory for information.

    The DD voltage level determines the level at which register overspill into the drain occurs.

PIN CONNECTIONS (View facing pins of connector)



This numbering applies to both connectors. The connector is a Glenair 51P micro D type.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase [A, D]	70	nF
IØ/SS per phase [A, D]	20	nF
Total IØ per phase (to Vss and two inter-phase)	160	nF
Transfer gates [TGA, TGD]	150	pF
RØ total per phase [each of E1/F1, G1/H1]	450	pF
RØ total per phase [each of E2/F2, G2/H2]	600	pF
RØ total per phase [each of E3/F3, G3/H3]	650	pF

The total capacitance to be driven per phase is the sum of the component to substrate and the inter-phase components to each of the adjacent phases. With 8 images phases the total parallel capacitance is 1.28 μF. Summing each of the 6 register phase capacitances gives a total serial capacitance of 3.4 nF.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from both of the parallel and serial clocking (i.e. driving the capacitive loads). The dynamic power dissipation (P) is determined separately for the serial and parallel clocking using capacitance, voltage and frequency values via the $P = CV^2f$ relationship. This will be the total clocked power and is divided between the drive buffer (off-chip) and the device (on-chip).

The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line readout using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

Read-out frequency	Frame Time	Line read time	Amplifier load	Power dissipation			
				Amplifiers	Serial clocking	Parallel clocking	Total (approx)
0.5 MHz	12.3 s	2.7 ms	5 kΩ	800 mW	~138 mW	~ 58 mW	1.0 W
1 MHz	6.8 s	1.5 ms	5 kΩ	800 mW	~275 mW	~105 mW	1.2 W
3 MHz	3.2 s	0.7 ms	5 kΩ	800 mW	~826 mW	~ 223 mW	1.8 W

Line transfer time and clock amplitudes are taken as the typical values listed in the clock timing requirements and electrical interfaces tables. 1179 register pixels are readout per register section for a total of 4616 rows.

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

Each flex-cable has a thermal conductivity of approximately 1 mW/°C.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltages for the amplifier and dump drains (OD, RD, DD) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 8) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

FRAME READ-OUT MODES

The device can be operated in a full-frame or split full-frame mode.

If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to effect the following directions of transfer.

Clock Generator Drive Pulse Name	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E register	A1	A2	A3	A4	TGA = IØ4
D section transfer towards G register	D1	D2	D3	D4	TGD = IØ1
A section transfer towards G register	A4	A3	A2	A1	TGA = "low"
D section transfer towards E register	D4	D3	D2	D1	TGD = "low"

The first two transfer sequences are for split frame read-out. The second two are for reversing the transfer direction in either section for read-out to either the top or the bottom register sections.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E/F1, G/H1, E/F2 and G/H2. These electrodes must be held at clock "high" level during the process. If the register pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below.

Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section	E1/F1	E2/F2	E3/F3
G section	G1/H1	G2/H2	G3/H3

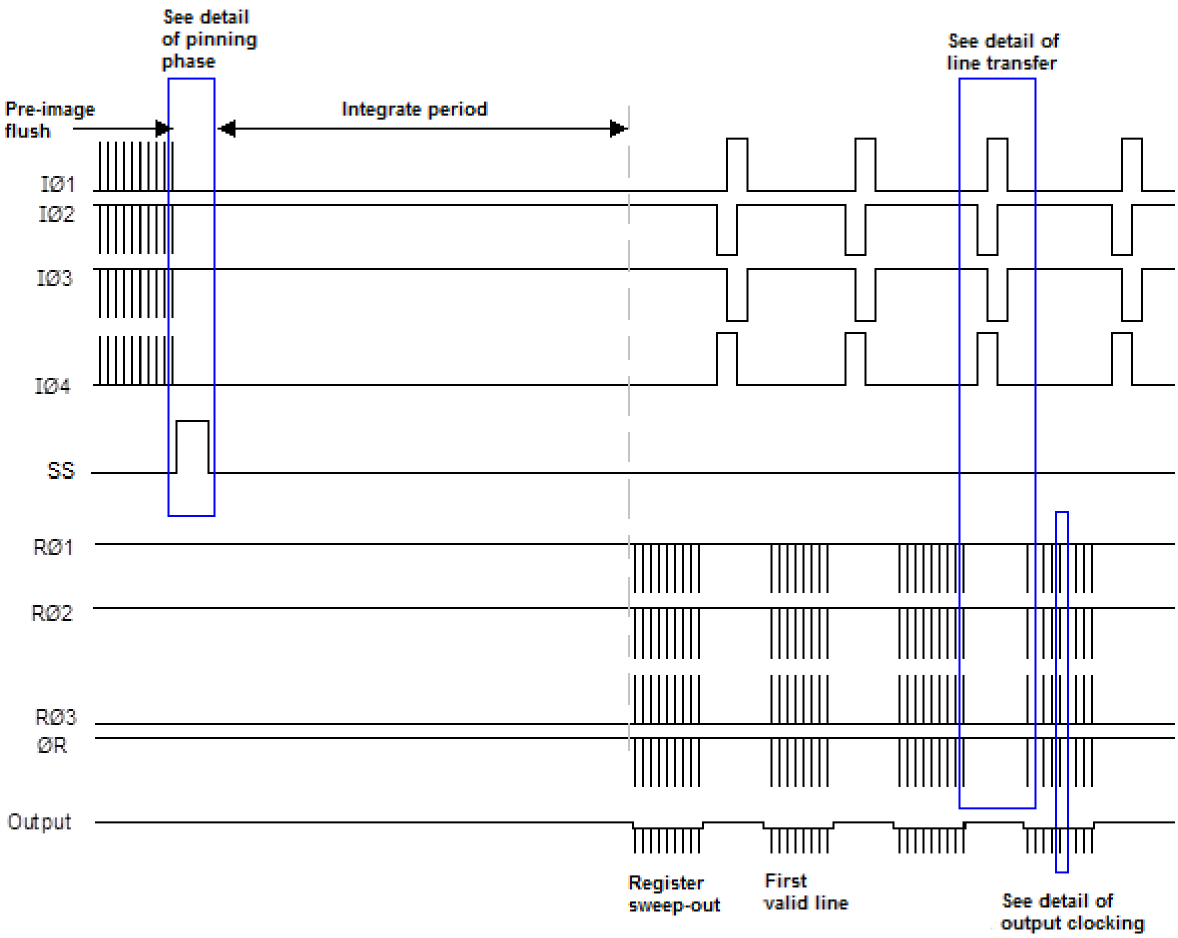
The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as RØ3. For summing, the selected SW gate is held at clock "high" level for the required number of readout cycles, and then clocked as RØ3 to output charge.

Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge now transfers into the output node as RØ2 goes low (see note 9 above also).

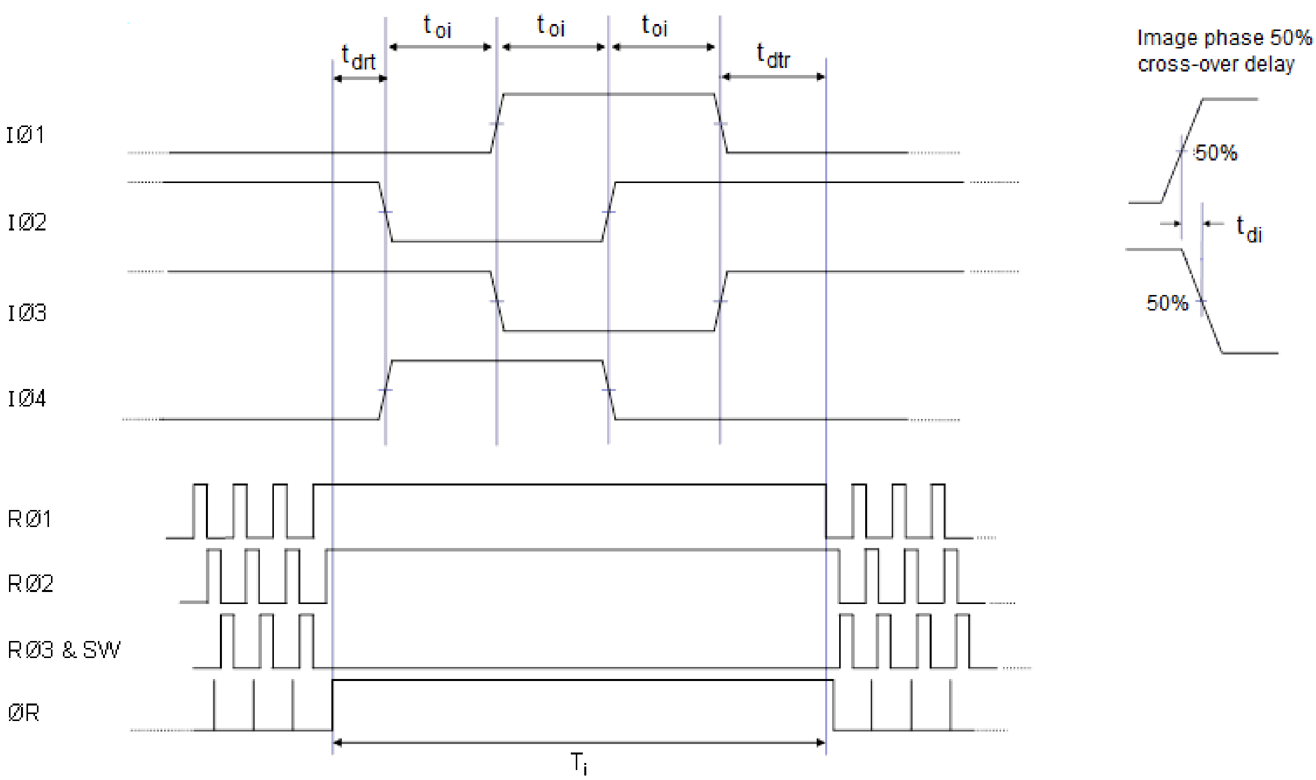
Image phases 2 and 3 should be held high during signal collection, as shown in the following figures.

The register is provided with an anti-blooming dump drain to limit the peak signal capacity. For charge dumping purposes rows of charge signals may be clocked into the register sections and any excess charge above full-well capacity spills into the drain. There must then be a single line read-out to remove the unwanted charge (i.e. which can be up to the full-well capacity) before transferring the wanted row or rows of charge signals into the register sections. However, please see note 13 above also.

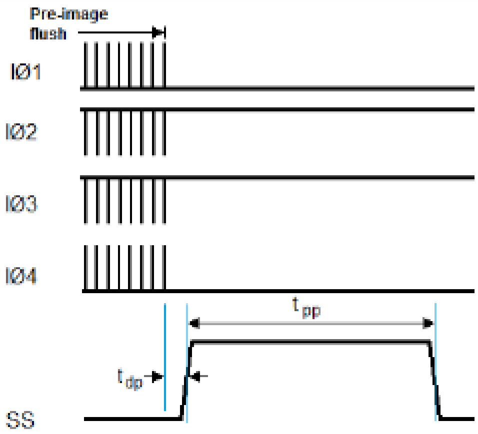
FRAME READ-OUT TIMING DIAGRAM



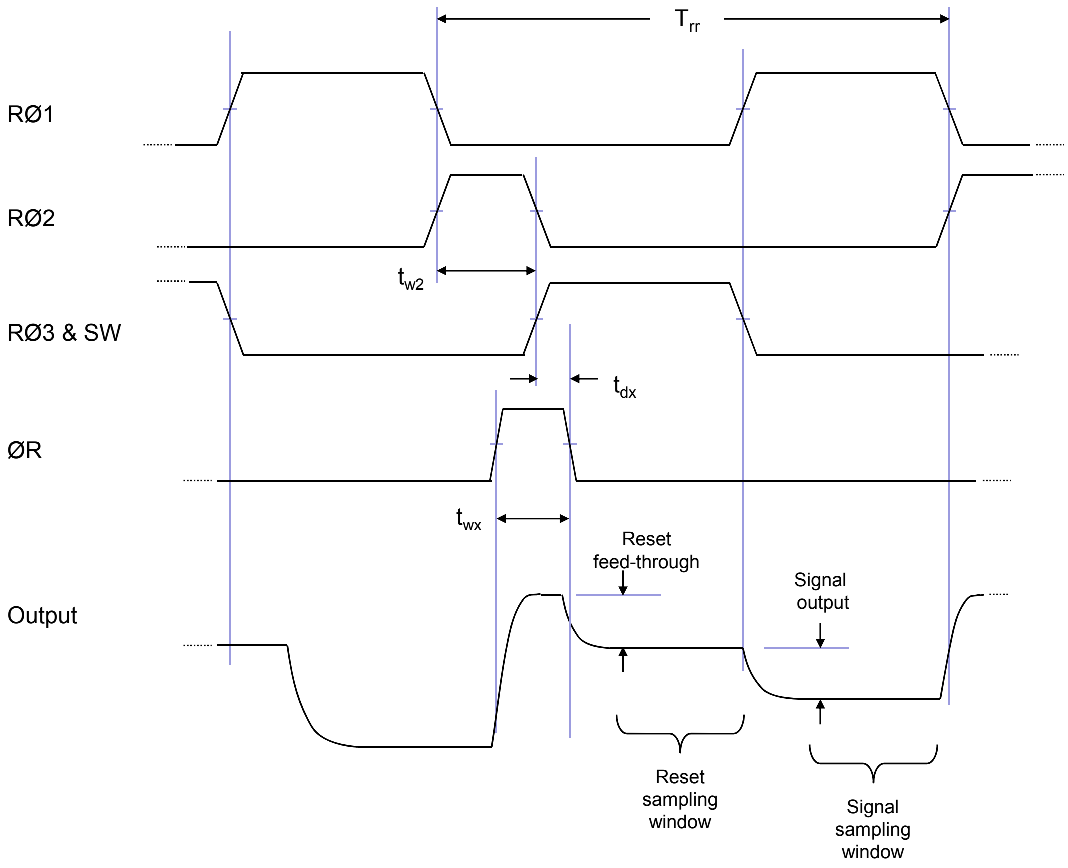
DETAIL OF LINE TRANSFER

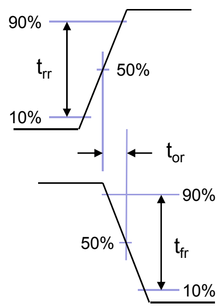


DETAIL OF PINNING PHASE (see note 19)

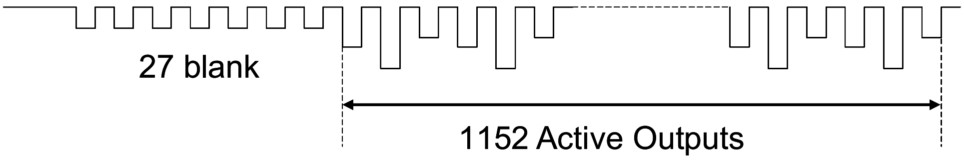


DETAIL OF REGISTER AND OUTPUT CLOCKING (with SW clocked as RØ3)





LINE OUTPUT FORMAT



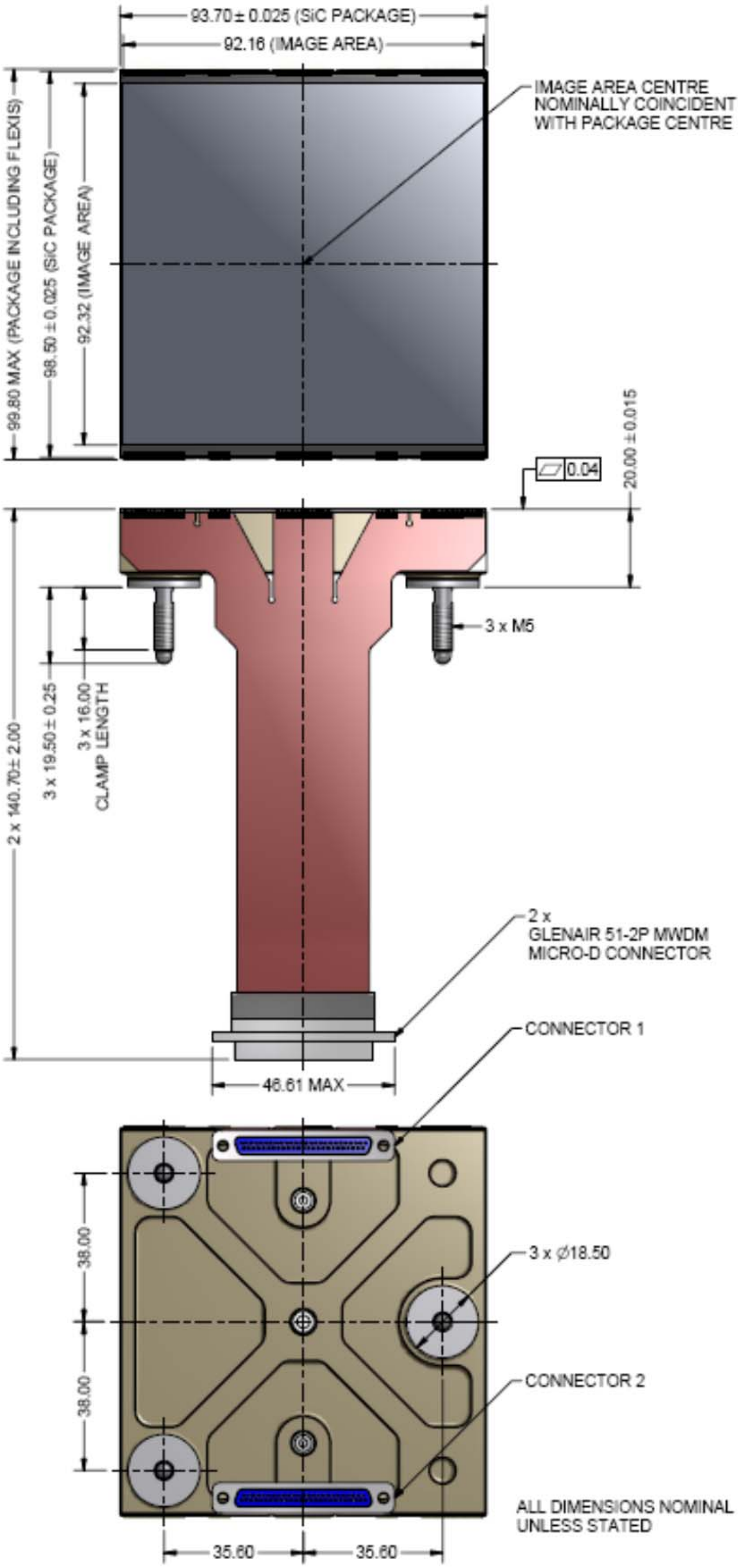
CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
T_i	Line transfer time (see note 14)	120	300	-	μs
t_{di}	Delay in falling image clock 50 % point from rising image clock 50 %point (see note 15)	0	30	500	ns
t_{oi}	Image clock pulse overlap	25	60	-	μs
t_{ri}	Image clock and transfer gate pulse rise time	2	5	0.3 t_{oi}	μs
t_{fi}	Image clock and transfer gate pulse fall time	2	5	0.3 t_{oi}	μs
t_{drt}	Delay time, RØ stop to IØ rising	15	30	-	μs
t_{dtr}	Delay time, IØ falling to RØ start	30	80	-	μs
t_{pp}	Substrate high duration during pinning phase	150	150	-	ms
t_{dp}	Delay time, last image flush clock transition to to substrate rising	3	3	-	ms
T_{rr}	Register clock period (see note 16)	300	2000	(see note 17)	ns
t_{w2}	RØ2 pulse width at 50% levels (see note 18)	$3t_{rx}$	350	$T_{rr}/3$	ns
t_{rr}	Register clock pulse rise time	10	70	$0.05T_{rr}$	ns
t_{fr}	Register clock pulse fall time	10	70	$0.05T_{rr}$	ns
t_{or}	Register clock pulse edge overlap at 50% levels	0	50	$0.05T_{rr}$	ns
t_{wx}	Reset pulse width at 50% levels	$3t_{rx}$	300	$0.2T_{rr}$	ns
t_{rx}	Reset pulse rise time	10	50	$0.2t_{wx}$	ns
t_{fx}	Reset pulse fall time	10	50	$0.2t_{wx}$	ns
t_{dx}	Delay time, RØ falling to ØR falling	$2t_{fr}$	150	-	ns

NOTES

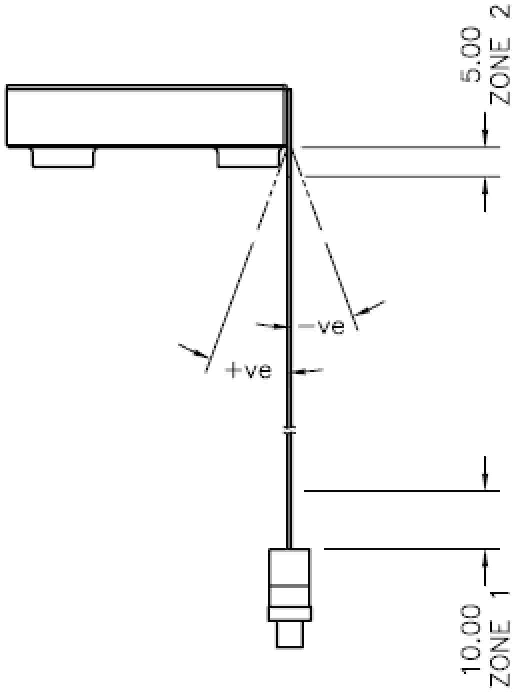
14. $T_i = t_{drt} + 3t_{oi} + t_{dtr}$.
15. The IØ1/IØ3, IØ2/IØ4, IØ3/IØ1 and IØ4/IØ2 transitions are nominally coincident with the edges overlapping at 50% amplitude.
16. The typical timing is for readout at frequencies in the region of 500 kHz, as used for factory tests.
17. For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz, then the load may be increased to 10 kΩ to reduce power consumption.
18. The RØ2 pulse-width is normally minimised, as shown, such that the RØ1 and RØ3 pulse widths can be increased to maximise the output reset and signal sampling intervals.
19. The large area and small pixel size of the CCD290 requires changes to be made to the standard mode of operation, particularly for devices manufactured from deep depletion silicon. This is because for this version of the CCD290, holes are not efficiently removed from the device with standard clocking and it is possible that the structure can be left with holes partially filling the isolation regions giving a photo-response non uniformity along each column. Visually this appears as a "tear" in the image. This effect is most visible with flat field images and is independent of image intensity. To remove this effect the substrate should be pulsed high by +10 V with respect to image clock low for a short period prior to integration, This substrate high pinning phase is implemented by e2v during acceptance testing. Alternatively, the image clocks can be reduced -10V below substrate if independent control of substrate voltage is not available.

PACKAGE DETAIL



The package base is Silicon Carbide; fitted with two flex-cable connectors and three mounting studs.

Interface drawing DAS772494AT (available on request) provides further information



The bend radius of the flexi PCB is recommended to be no less than 10 mm, with an absolute minimum of 5.8 mm. There should be no forced bending within 10mm of the connector potting (zone 1). There should be no forced bending of the flexi in the negative direction within 5 mm of the flexi to package bondline (zone 2).

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

Buttable flex-cable devices require careful handling to avoid damage to silicon, bond wires of flex cables. Avoid stress on flex cables, and contact factory for advice if needed.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range 153 - 323 K

Storage temperature range 148 - 358 K

Performance parameters are measured with the device at a temperature of 173 K and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions before the sensor taken to low ambient temperatures may give rise to ice on the surface, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.