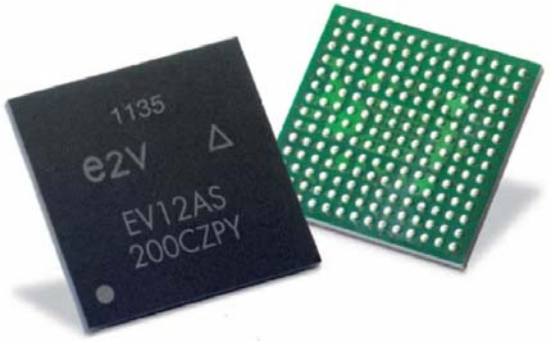
EV12AS200ZPY
ANALOG to DIGITAL CONVERTER
12-bit 1.5 Gsps ADC

Datasheet

Main Features



- Single Core ADC Architecture with 12-bit Resolution Integrating a Selectable 1:1 and 1:2 DEMUX
- Differential Input Clock (AC Coupled)
- 500 mVpp Analogue Input Voltage (Differential Full Scale and AC Coupled)
- Noise Floor of –150 dBm/HZ (13-bit ENOB in 10 MHz Bandwidth)
- Analogue and Clock Input Impedance: 100Ω Differential
- LVDS Differential Output Data
- NPR 48.5 dB (Equivalent 9.6 ENOB)
- 3 Wire Serial Interface (3WSI) Digital Interface (Write Only) with Reset Signal
- ADC Gain, Offset, Sampling Delay for Interleaving Control
- No Missing Codes at 1.5 GSps 1st and 2nd Nyquist
- Low Latency (< 5 Clock Cycles)
- Test Modes
- Data Ready Common to the 2 Output Ports
- Power Supply: 5.2V, 3.3V and 2.5V (Output Buffers)
- Power Dissipation: 3.2W
- FpBGA 196 Package (15x15 mm^2)

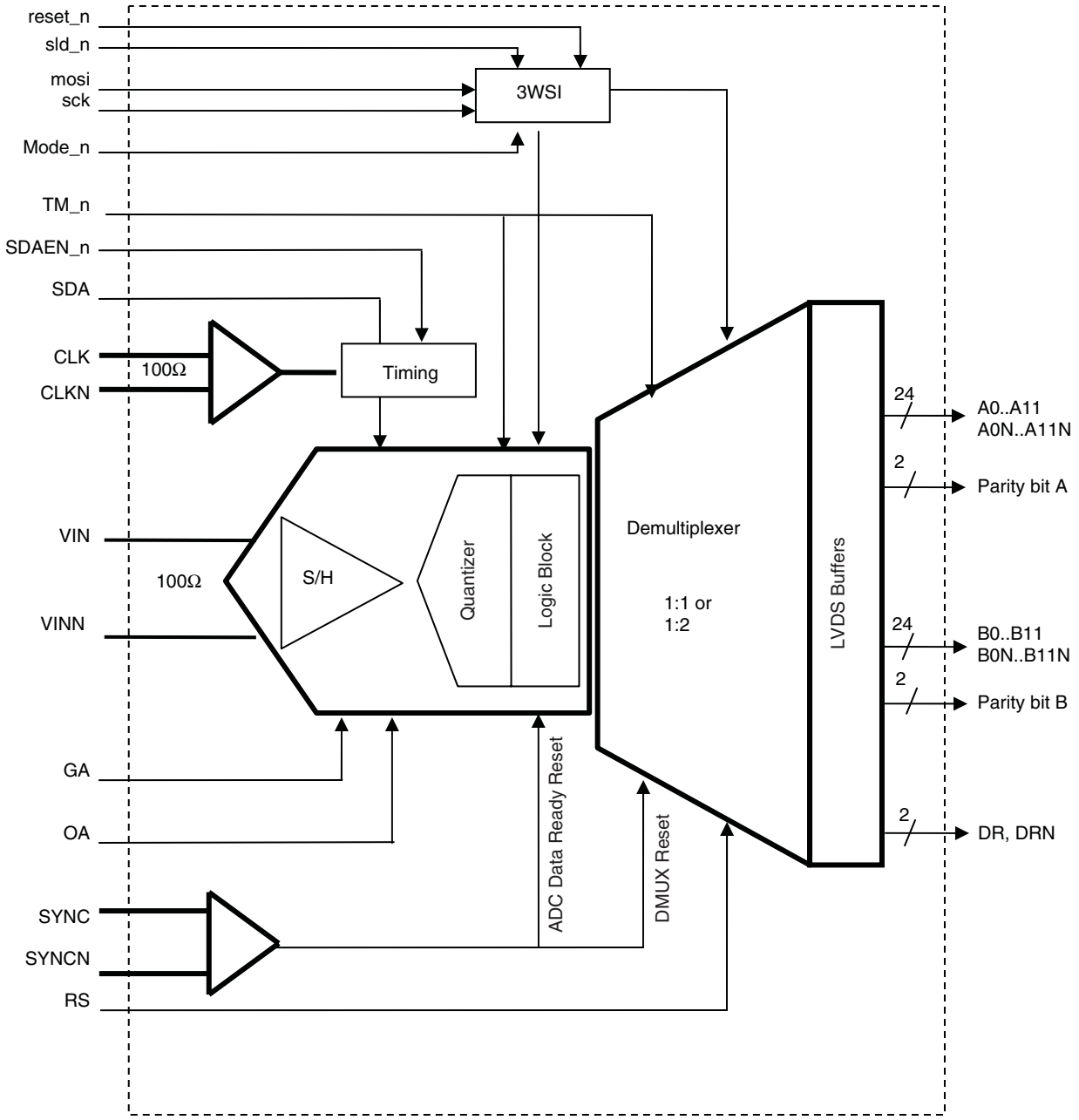
Applications

- Telecom Test Instrumentation
- Wireless Communications Systems
- Direct RF Down-conversion
- Automatic Test Equipment
- Direct L-Band RF Down Conversion
- Radar Systems

1. General Description

1.1 Block Diagram

Figure 1-1. ADC with Integrated DEMUX Block Diagram



1.2 Description

The EV12AS200 is a 12-bit 1.5 GSps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100Ω differential output buffers. It integrates 3 Wire Serial Interface (3WSI) circuit (write only), which can be activated or deactivated (via Mode signal). Main functions accessed via the 3WSI can also be accessed by hardware (OA, GA, SDA, SDAEN_n, TM_n, RS pin).

The EV12AS200 works in fully differential mode from analog inputs through digital outputs.
It operates in the first Nyquist zone up to L-Band.

DEMUX Ratio (1:1 or 1:2) can be selected with the pin RS or via the 3WSI when activated.
DEMUX outputs are synchronous on each port.

A differential Data Ready output is available to indicate when the outputs are valid. The Data Ready (Differential DR, DRN) is common to the 2 ports.

A sampling rate mode (HSR) is embedded in order to output data up to 1 GHz in mode DMUX1:1.

In order to ease the synchronization of multiple ADC the TRIGGER function can be activated.

A power up reset ensures that the first digitized data corresponds to the first acquisition. An external differential LVDS Reset (SYNC, SYNCN) can also be used. RES function allows changing the active edge of the reset signal.

The gain control pin GA and offset control OA are provided to adjust the ADC gain and offset transfer function. These functions can also be accessed via the 3WSI.

A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requesting the interleaving of multiple ADCs for example. It is enabled thanks to SDAEN_n pin. This function is also available with the 3WSI. In this case the tunable range is extended thanks to 2 bits for coarse adjustment.

For debug and testability, the following functions are provided:

- A static test mode, used to test either VOL or VOH at the ADC outputs (all bits at “0” level or “1” level respectively) – these modes are accessed only via the 3WSI when activated;
- A dynamic built-In Test (alignment pattern with period of 16), accessed by hardware (TM_n signal) or via 3WSI when activated.

A diode is provided to monitor the junction temperature, with both anode and cathode accessible.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
V_{CC5} supply voltage	V_{CC5}		GND to 6	V
V_{CC3} supply voltage	V_{CC3}		GND to 3.6	V
V_{CCO} supply voltage	V_{CCO}		GND to 3.6	V
Analog input voltages	V_{IN} or V_{INN}		min: 2.0 max: 4.0	V V
Maximum difference between V_{IN} and V_{INN}	$IV_{IN} - V_{INN}I$		2.0 4 Vpp = +13 dBm in 100Ω	V
Maximum difference between V_{CLK} and V_{CLKN}	$IV_{CLK} - V_{CLKN}I$		3	Vpp
Reset input voltage	V_{RST} or V_{RSTN}		–0.3 to V_{CC3} + 0.3	V
Analog input settings	V_A	OA, GA, SDA	0 to V_{CCA3}	V
Control inputs	V_D	SDAEN, TM0, TM1, RS0, RS1, RSTN	–0.3 to V_{CC3} + 0.3	V
Junction Temperature	T_J		170	°C
Storage Temperature	Tstg		–65 to 150	°C

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
2. Maximum ratings allow active inputs with ADC powered off.
3. Maximum ratings allow active inputs with ADC powered on.

2.2 Recommended Conditions of Use

Table 2-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Power supplies (2)	V_{CC5}		5.2	V
	V_{CC3}		3.3	V
	V_{CC0}		2.5	V
Differential analog input voltage (Full Scale)	$V_{IN} - V_{INN}$	100Ω differential	500	mVpp
Clock input power level	P_{CLK} P_{CLKN}	With 100Ω differential input With 1.3 GHz sinewave input	+4	dBm
Operating Temperature Range	T_c T_j	Commercial “C” grade Industrial “V” grade	T_c > 0°C ; T_j < 90°C T_c > –40°C ; T_j < 110°C	°C

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
2. No specific sequencing is required, however to benefit from the internal power on RESET, V_{CC3} should be applied before V_{CC5}. See Section 4.12 ”Power on Reset” on page 32.

2.3 Electrical Characteristics

Unless otherwise stated, specifications apply over the full operating temperature range (for performance) and at all power supply conditions.

Table 2-3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
RESOLUTION			12		bit	
POWER REQUIREMENTS						
Power Supply voltage						
- Analogue	VCC5	5	5.2	5.5	V	1
- Analogue Core and Digital	VCC3	3.15	3.3	3.45	V	1
- Output buffers	VCCO	2.4	2.5	2.6	V	1
Power Supply current in 1:1 DEMUX Ratio						
- Analogue	I_VCC5		200	220	mA	1
- Analogue Core and Digital	I_VCC3		550	620	mA	1
- Output buffers	I_VCCO		75	100	mA	1
Power Supply current in 1:2 DEMUX Ratio						
- Analogue	I_VCC5		200	220	mA	1
- Analogue Core and Digital	I_VCC3		550	620	mA	1
- Output buffers	I_VCCO		120	150	mA	1
Power dissipation						
- 1:1 Ratio with standard LVDS output swing	P_D		3.0	3.2	W	1
- 1:1 Ratio with standard LVDS output swing, HSR mode	P_D		3.15	3.4		1
- 1:2 Ratio with standard LVDS output swing	P_D		3.15	3.3		1
LVDS Data and Data Ready Outputs						
Logic compatibility			LVDS differential			
Output Common Mode[1]	VOCM	1.125	1.25	1.375	V	1
Differential output ([1][2]	VODIFF	200	300	400	mV	1
Output level “High”[2]	VOH	1.25	–	–	V	1
Output level “Low”[2]	VOL	–	–	1.25	V	1
Output data format			Binary			
ANALOG INPUT						
Input type			AC coupled			
Analogue input Common mode			3.12		V	1
Full scale input voltage range (differential mode)	VIN VINN		–125 to +125 +125 to –125		mV mV	1 1
Full scale analog input power level	PIN		–5		dBm	1
Analog input capacitance (die only)	CIN		0.3		pF	1
Input leakage current (VIN = VINN = 0V)	IIN		50		µA	1
Analog Input resistance (Differential)	RIN	96	100	104	Ω	1
ESD immunity (HBM model) (except CMI ref PIN)			1000 500		V	

Table 2-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
CLOCK INPUT (CLK, CLKN)						
Input type		DC or AC coupled				
Clock Input Common Mode (for DC coupled clock)	V_{ICM}		2.65		V	4
Clock Input power level (low phase noise sinewave input) 100Ω differential	P_{CLK}	0	4	+10	dBm	4
Clock input swing (differential voltage) on each clock input	V_{CLK} V_{CLKN}	±447	±708	±1410	mV	4
Clock input capacitance (die only)	C_{CLK}		0.3		pF	4
Clock Input resistance (Differential)	R_{CLK}	95	100	105	Ω	4
SYNC, SYNCN (active low)						
Logic compatibility		LVDS				
Input Common Mode	V_{ICM}	1.125	1.25	1.375	V	4
Differential input	V_{IDIFF}	250	350	450	mV	4
Input level “High”	V_{IH}			1.8	V	4
Input level “Low”	V_{IL}	0.7			V	4
DIGITAL INPUTS (RS, SDAEN_n, TM_n)						
Logic low - Resistor to ground - Voltage level - Input current	 R_{IL} V_{IL} I_{IL}	 0		 10 0.5 450	 Ω V µA	4
Logic high - Resistor to ground - Voltage level - Input current	 R_{IH} V_{IH} I_{IH}	 10k 2.0		 10^5 150	 Ω V µA	4
OFFSET, GAIN & SAMPLING DELAY ADJUST SETTINGS (OA, GA, SDA)						
Min voltage for minimum Gain, Offset or SDA	Analog_min	$2*V_{CC3}/3 - 0.5$			V	4
Max voltage for maximum Gain, Offset or SDA	Analog_max			$2*V_{CC3}/3 + 0.5$	V	4
Input current for min setting	I_{min}			200	µA	4
Input current for nominal setting	I_{nom}			50	µA	4
Input current for max setting	I_{max}			200	µA	4
3WSI (sck, sld_n, mosi, reset_n, mode_n)						
Logic compatibility		3.3V CMOS				
Low Level input voltage	V_{IL}	0		1	V	4
High Level input voltage	V_{IH}	2.3		V_{CC3}	V	4
Low Level input current			100		µA	4
High Level input current			100		µA	4

Table 2-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
DC ACCURACY						
Missing codes	M_{CODES}		None allowed			
Differential Non Linearity (for information only)	DNL+		+1		LSB	1
Differential Non Linearity (for information only)	DNL-		0.8		LSB	1
Integral Non Linearity (for information only)(5)	INL+		7		LSB	1
Integral Non Linearity (for information only)(5)	INL-		6		LSB	1
Gain central value(3)	ADC_{GAIN}	0.8	1.0	1.2		1
Gain error drift versus temperature (over 15°C)				0.15	dB	1
ADC offset(4) nominal	ADC_{OFFSET}	1948	2048	2148	LSB	1

Notes:
1. Assuming 100Ω termination ASIC load.
2. VOH min and VOL max can never be 1.25V at the same time when VODIFFmin.
3. The ADC Gain center value can be tuned to 1.0 using Gain adjust function.
4. The ADC offset can be tuned to mid code 2048 using Offset adjust function.
5. INL values and form is stable and can be subtracted using a look up table.

2.4 Dynamic Performance

Unless otherwise stated, min and max values apply over the full operating temperature range assuming an external clock jitter of 75 fs rms in differential mode. Typical values are given for nominal conditions.

Table 2-4. Dynamic Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
AC Analog Inputs						
Full power Input Bandwidth	FPBW		2.3		GHz	
Gain Flatness (from 50 to 200 MHz) (Fclk=1.33GSps)			0.1		dB	
Gain Flatness (from 200 to 1300 MHz) (Fclk=1.33GSps)			0.6		dB	
Gain Flatness (from 1300 to 1800 MHz) (Fclk=1.33GSps)			0.9		dB	
–1 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1.33 Gsps Fin = 665 MHz (1)		54.7/51.7	56.4/54			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		52.9/50.5	55.2/52.7			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		53.5/50.5	55.8/53.5			1
FS = 1.5 Gsps Fin = 740 MHz (1)	SINAD	–	55.5/52		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	55/52			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			55.8/53.8			4
Effective Number of Bits						
FS = 1.33 Gsps Fin = 665 MHz (1)		8.8/8.3	9.1/8.7			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		8.5/8.1	8.9/8.5			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		8.6/8.1	9.0/8.6			1
FS = 1.5 Gsps Fin = 740 MHz (1)	ENOB	–	8.9/8.4		Bit FS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	8.8/8.4			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			9.0/8.6			4
Signal to Noise Ratio						
FS = 1.33 Gsps Fin = 665 MHz (1)		57/57	57.8/57.8			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		56.2/56.2	56.8/56.8			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		56.5/56.5	57.3/57.3			1
FS = 1.5 Gsps Fin = 740 MHz (1)	SNR	–	57.2/57.2		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	56/56			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			57.4/57.4			4
Total Harmonic Distortion (25 harmonics)						
FS = 1.33 Gsps Fin = 665 MHz (1)		56/52	62/56			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		54/51	60/54			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		55/52	62/56			1
FS = 1.5 Gsps Fin = 740 MHz (1)	|THD|	–	61/53		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	62/55			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			61.2/55.8			4

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Spurious Free Dynamic Range						
FS = 1.33 Gsps Fin = 665 MHz (1)		60/53	68/58			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		55/52	63/55			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		60/53	68/57			1
FS = 1.5 Gsps Fin = 740 MHz (1)	|SFDR|	–	65/54		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	67/55			4
DMUX1 :1 HSR mode						
FS = 1.33 Gsps Fin = 663 MHz (1)			65.1/57.1			4
–3 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1.33 Gsps Fin = 665 MHz (1)		54.7/52.3	56.4/55.2			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		53.5/51.1	55.5/53.4			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		53.5/50.5	56.4/54			1
FS = 1.5 Gsps Fin = 740 MHz (1)	SINAD	–	55/54		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–				4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			56.5/55			4
Effective Number of Bits						
FS = 1.33 Gsps Fin = 665 MHz (1)		8.8/8.4	9.1/8.9			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		8.6/8.2	9.0/8.6			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		8.6/8.2	9.1/8.7			1
FS = 1.5 Gsps Fin = 740 MHz (1)	ENOB	–	9.1/8.8		Bit FS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	8.9/8.6			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			9.1/8.8			4
Signal to Noise Ratio						
FS = 1.33 Gsps Fin = 665 MHz (1)		57/57	58.2/58.2			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		56.8/56.8	57.4/57.4			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		57/57	57.8/57.8			1
FS = 1.5 Gsps Fin = 740 MHz (1)	SNR	–	57.7/57.7		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	56.8/56.8			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			57.9/57.9			4
Total Harmonic Distortion (25 harmonics)						
FS = 1.33 Gsps Fin = 665 MHz (1)		56/54	63/58			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		55/52	61/56			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		56/53	63/57			1
FS = 1.5 Gsps Fin = 740 MHz (1)	|THD|	–	62.5/58		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	62/56			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			62/58			4

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Spurious Free Dynamic Range						
FS = 1.33 Gsps Fin = 665 MHz (1)		60/56	68/60			1
FS = 1.33 Gsps Fin = 1300 MHz (1)		58/53	63/55			1
FS = 1.33 Gsps Fin = 1000 MHz (1)		60/54	69/58			1
FS = 1.5 Gsps Fin = 740 MHz (1)	|SFDR|	–	68/58		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz (1)		–	67/57			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz (1)			67/60			4
–8 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1.33 Gsps Fin = 665 MHz		54.7	57.6			1
FS = 1.33 Gsps Fin = 1300 MHz		54.7	57			1
FS = 1.33 Gsps Fin = 1000 MHz		54.7	57.6			1
FS = 1.5 Gsps Fin = 740 MHz	SINAD	–	57.6		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	57			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			57.1			4
Effective Number of Bits						
FS = 1.33 Gsps Fin = 665 MHz		8.8	9.3			1
FS = 1.33 Gsps Fin = 1300 MHz		8.8	9.2			1
FS = 1.33 Gsps Fin = 1000 MHz		8.8	9.3			1
FS = 1.5 Gsps Fin = 740 MHz	ENOB	–	9.3		Bit FS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	9.2			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			9.2			4
Signal to Noise Ratio						
FS = 1.33 Gsps Fin = 665 MHz		58	58.6			1
FS = 1.33 Gsps Fin = 1300 MHz		57.7	58.3			1
FS = 1.33 Gsps Fin = 1000 MHz		57.7	58.5			1
FS = 1.5 Gsps Fin = 740 MHz	SNR	–	58.6		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	58.2			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			58.4			4
Total Harmonic Distortion (25 harmonics)						
FS = 1.33 Gsps Fin = 665 MHz		57	63			1
FS = 1.33 Gsps Fin = 1300 MHz		57	64			1
FS = 1.33 Gsps Fin = 1000 MHz		57	65			1
FS = 1.5 Gsps Fin = 740 MHz	|THD|	–	64		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	62			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			63			4

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Spurious Free Dynamic Range						
FS = 1.33 Gsps Fin = 665 MHz		58	68			1
FS = 1.33 Gsps Fin = 1300 MHz		58	69			1
FS = 1.33 Gsps Fin = 1000 MHz		58	70			1
FS = 1.5 Gsps Fin = 740 MHz	(SFDR)	–	69		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	67			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			67			4
–12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1.33 Gsps Fin = 665 MHz		55.3	57.6			1
FS = 1.33 Gsps Fin = 1300 MHz		55.3	57.6			1
FS = 1.33 Gsps Fin = 1000 MHz		55.3	57.6			1
FS = 1.5 Gsps Fin = 740 MHz	SINAD	–	58.2		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	57.6			4
DMUX1 :1 HSR mode						
FS = 1.00 Gsps Fin = 663 MHz			57.7			4
Effective Number of Bits						
FS = 1.33 Gsps Fin = 665 MHz		8.9	9.3			1
FS = 1.33 Gsps Fin = 1300 MHz		8.9	9.3			1
FS = 1.33 Gsps Fin = 1000 MHz		8.9	9.3			1
FS = 1.5 Gsps Fin = 740 MHz	ENOB	–	9.5		Bit FS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	9.3			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			9.3			4
Signal to Noise Ratio						
FS = 1.33 Gsps Fin = 665 MHz		58	58.9			1
FS = 1.33 Gsps Fin = 1300 MHz		58	58.7			1
FS = 1.33 Gsps Fin = 1000 MHz		58	58.8			1
FS = 1.5 Gsps Fin = 740 MHz	SNR	–	59		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	58.7			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			58.7			4
Total Harmonic Distortion (25 harmonics)						
FS = 1.33 Gsps Fin = 665 MHz		58	65			1
FS = 1.33 Gsps Fin = 1300 MHz		58	66			1
FS = 1.33 Gsps Fin = 1000 MHz		58	67			1
FS = 1.5 Gsps Fin = 740 MHz	THD	–	65		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	63			4
DMUX1 :1 HSR mode						
FS = 1.33 Gsps Fin = 663 MHz			65			4

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Spurious Free Dynamic Range						
FS = 1.33 Gsps Fin = 665 MHz		59	70			1
FS = 1.33 Gsps Fin = 1300 MHz		62	72			1
FS = 1.33 Gsps Fin = 1000 MHz		59	72			1
FS = 1.5 Gsps Fin = 740 MHz	SFDR	–	69		dBFS	4
FS = 1.5 Gsps Fin = 1490 MHz		–	68			4
DMUX1 :1 HSR mode						
FS = 1 Gsps Fin = 663 MHz			69			4
Broadband performance						
Noise Power Ratio Notch centered on 225 MHz, Notch width 12.5 MHz on 10 MHz 450 MHz band 1.5 Gsps at optimisation factor loading –14 dBFS	NPR		48.5		dB	4
NPR 2e Nyquist						4
IMD3 differential 2Fin1 - Fin2, 2 Fin2 - Fin1, unfilterable 3rd order intermodulation products at –7 dBFS Fin1 = 700 MHz Fin2 = 710 MHz	IMD3		77		dBc	4
IMD3 differential 2Fin1 - Fin2, 2 Fin2 - Fin1, unfilterable 3rd order intermodulation products at –7 dBFS Fin1 = 1450 MHz Fin2 = 1460 MHz	IMD3		67		dBc	4

Notes: 1. Values are given : with LUT correction/without LUT correction
LUT correction uses a generic look up table available on request. Contact hotline-bdc@e2v.com
Note at signal levels of –8 dBFS and below LUT correction is not required.
See Section 6.3.2 "Improving SFDR and ENOB using a LUT" on page 44, for more information.

2.5 Timing Characteristics and Switching Performances

Unless otherwise stated min or max requirements apply over the full operating temperature range and at all power supply conditions. Typical values are given for nominal conditions.

Table 2-5. Timing characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
SWITCHING PERFORMANCE AND CHARACTERISTICS						
Maximum clock frequency(1)						4
1:1 DEMUX Ratio HRS mode disabled HRS mode enabled 1:2 DEMUX Ratio				750 1000 1500	MHz	4
Minimum clock frequency(1)		300			MHz	4
Maximum Output Rate per port (Data and Data Ready)						4
1:1 DEMUX Ratio						4
HRS mode disabled			665	750	Msps	4
HRS mode enabled			1000			4
1:2 DEMUX Ratio			665	750		4
Analogue input frequency		10		1800	MHz	4
BER				1×10^{-12}	Error/sample	4
TIMING						
ADC settling time (VIN-VINN = 400 mVpp)	TS		250		ps	4
Overvoltage recovery time	ORT			300	ps	4
ADC step response (10% to 90%)			120		ps	4
Overshoot			0.2		%	4
Ringback			0.2		%	4
Sampling Clock duty cycle		48	50	52	%	4
Minimum clock pulse width (high)	TC1	0.3		1.5	ns	4
Minimum clock pulse width (low)	TC2	0.3		1.5	ns	4
Aperture delay(1)	TA		75		ps	4
Internal clock Jitter				100	fsrms	4
Output rise/fall time for DATA (20% to 80%)(3)	TR/TF	300	360	430	ps	4
Output rise/fall time for DATA READY (20% to 80%)(2)	TR/TF	300	350	400	ps	4
Data output delay(4)	TOD	2.7	3	3.1	ns	4
Data Ready output delay(4)	TDR	2.7	3	3.1	ns	4
	|TOD – TDR|		0		ps	4
Output Data to Data Ready propagation delay(5)	TD1		700		ps	4
Data Ready to Output Data propagation delay(5)	TD2		633		ps	4

Table 2-5. Timing characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Output Data Pipeline delay						
1:1 DEMUX Ratio 1:2 DEMUX Ratio port A&B	TPD		4 4.5		Clock cycle	4
Data Ready Pipeline delay						4
1:1 DEMUX Ratio	TPDR		4.5		Clock cycle	4
1:2 DEMUX Ratio port A&B			5.5			4
SYNC to DR, DRN						4
1:1 DEMUX Ratio	TRDR		2.5		ns	4
1:2 DEMUX Ratio			2.6			4
SYNC min pulse duration		1			Clock cycle	4
SYNC Signal valid timing (see Figure 2-5 on page 17)	T1 T2	120 120			ps	4
Skew between data			70		ps	4

Notes:
1. See Definition Of Terms.
2. Data Ready outputs are active on both rising and falling edges (DR/2 mode)
3. 100Ω// C_{LOAD} = 2 pF // 2 nH termination (for each single-ended output). Termination load parasitic capacitance derating value: 50 ps/pF (LVDS).
4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only.
5. Values for TD1 and TD2 are given for a 1.5 Gsps external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: TD1 = T/2 + (TOD-TDR) and TD2 = T/2 - (TOD-TDR), where T = clock period. This places the rising edge (True-False) od the differential Data ready signal in the middle of the Output Data Valid window. This gives maximum setup and hold times for external acquisition. The difference (TD1-TD2) gives information if Data Ready is centered on the output data. If Data Ready is in middle TD1 = TD2 = Tdata/2.
   This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition.

2.6 Timing Diagrams

Figure 2-1. Principle of Operation, DMUX 1:1

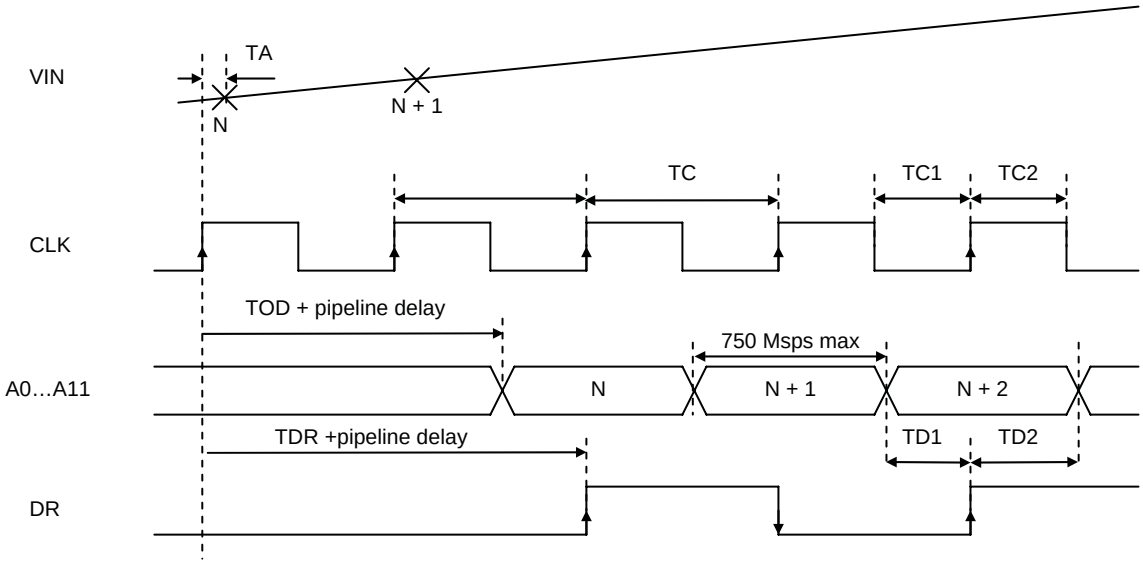


Figure 2-2. Principle of Operation, DMUX 1:2

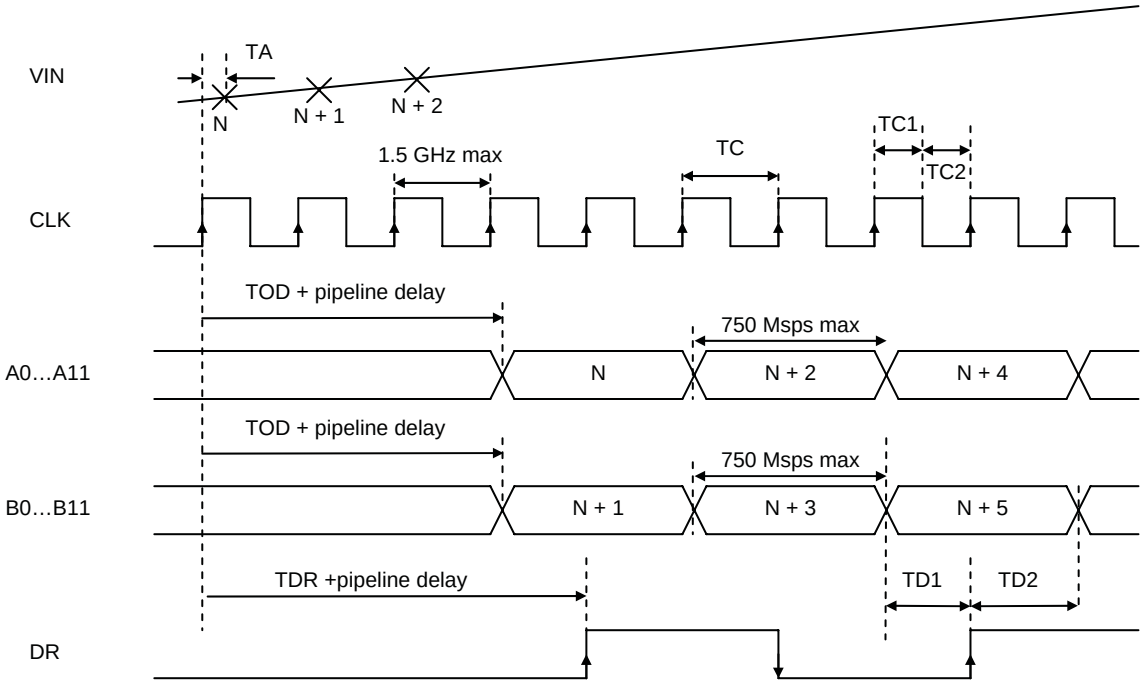
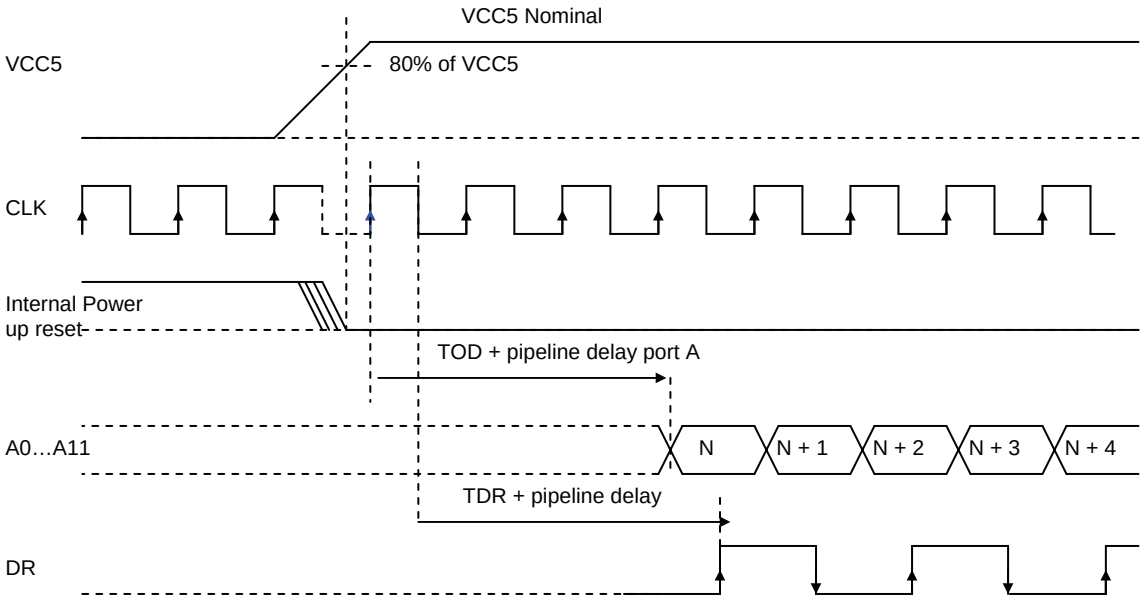
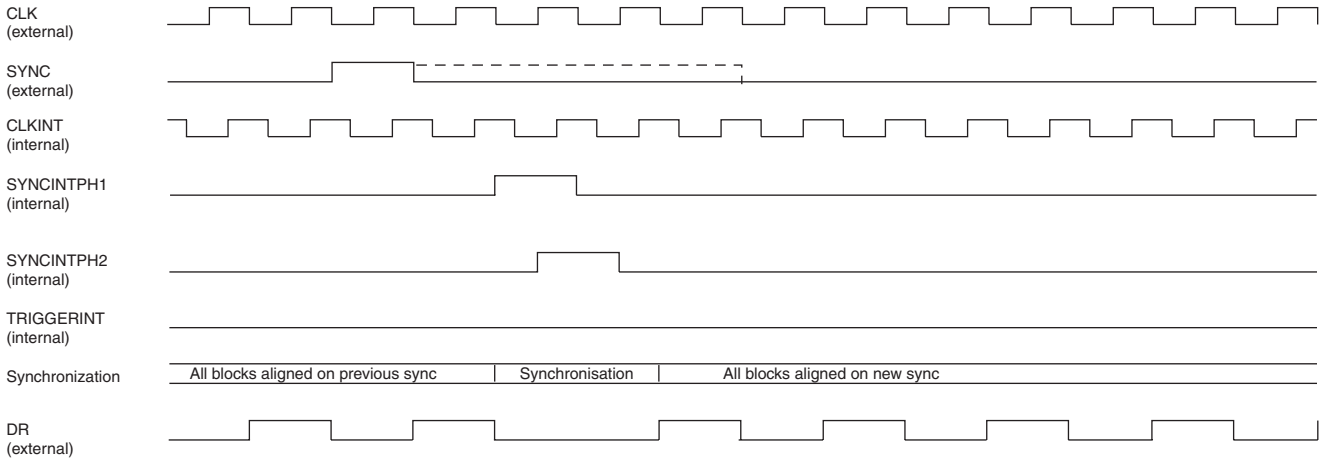


Figure 2-3. Power up Reset Timing Diagram (1:1 DMUX)



Note V_{CC3} should be applied before V_{CC5}.

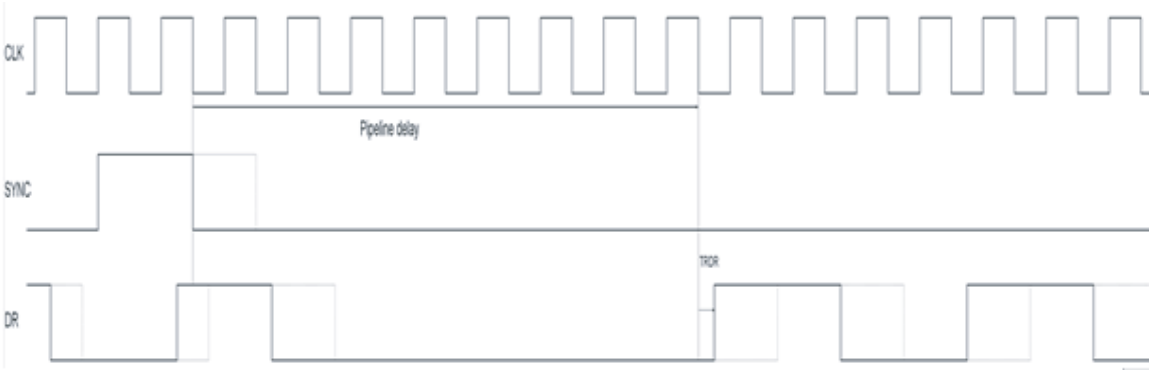
Figure 2-4. SYNC Timing Diagram (1:1 DMUX)



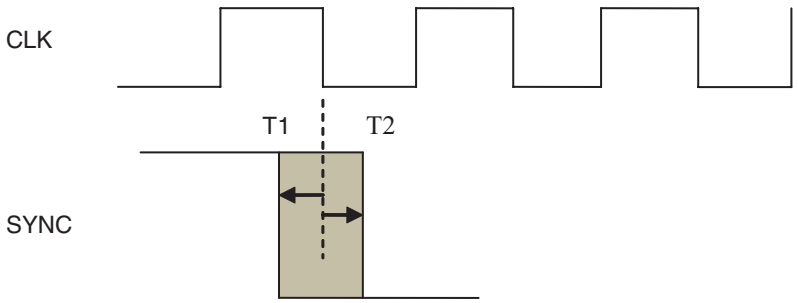
For Trigger mode function of this pin refer to Figure 4-2 on page 32.

Figure 2-5. SYNC Timing

SYNC timing diagram (DEMUX 1:2 & Reset Edge : Falling)



T1 & T2 diagram



Forbidden Zone

The SYNC signal should be timed so that it does not fall in the forbidden zone described in the image above.

The SYNC signal is timed from the falling edge of the input clock.

2.7 Definition of Terms

Table 2-6. Definition of Terms

Abbreviation	Term	Definition
(Fs max)	*Maximum Sampling Frequency*	Performances are guaranteed up to Fs max (unless specified.)
(Fs min)	*Minimum Sampling frequency*	Performances are guaranteed for sampling frequency above Fs min.
(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ±128 LSB from the correct code.
(FPBW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (–1 dBFS).
(SSBW)	*Small Signal Input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –10 dB (–10 dBFS).
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale (–1 dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics.
(THD)	*Total harmonic distortion*	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (i.e, related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(ENOB)	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$ Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (V_{IN},V_{INN}) is sampled.
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	*Settling time*	Time delay to achieve 0.2% accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(ORT)	*Overvoltage recovery time*	Time to recover 0.2% accuracy at the output, after a 150% full scale step applied on the input is reduced to midscale.
(TOD)	*Digital data Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TDR)	*Data ready output delay*	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.

Table 2-6. Definition of Terms (Continued)

Abbreviation	Term	Definition
(TD1)	*Time delay from Data transition to Data Ready*	This gives maximum setup and hold times for external acquisition. The difference (TD1-TD2) gives information if Data Ready is centered on the output data. If Data Ready is in middle TD1 = TD2 = Tdata/2.
(TD2)	*Time delay from Data Ready to Data*	This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	*Pipeline Delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TRDR)	*Data Ready reset delay*	Delay between the falling edge of the Data Ready output asynchronous Reset signal (RSTN) and the reset to digital zero transition of the Data Ready output signal (DR).
(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (ie. 99% power transmitted and 1% reflected).

2.8 Explanation of Test Levels

1	100% production tested at +25°C(1).
2	100% production tested at +25°C(1), and sample tested at specified temperatures.
3	Sample tested only at specified temperatures.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only guaranteed by design only.

Note: Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

Notes: 1. Unless otherwise specified.
2. If applicable, please refer to “Ordering Information”

2.9 Coding

Table 2-7. ADC Coding Table

Differential analog input	Voltage level	Digital output Binary MSB (bit 11)…….....LSB (bit 0)
> + 250.25 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1
+ 250.25 mV + 249.75 mV	Top end of full scale + ½ LSB Top end of full scale – ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
+ 125.25 mV + 124.75 mV	3/4 full scale + ½ LSB 3/4 full scale – ½ LSB	1 1 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1
+ 0.25 mV – 0.25 mV	Mid scale + ½ LSB Mid scale – ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
–124.75 mV –124.25 mV	1/4 full scale + ½ LSB 1/4 full scale – ½ LSB	0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
–249.75 mV –250.25 mV	Bottom end of full scale + ½ LSB Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
< –250.25 mV	< Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0

3. Pin Description

Figure 3-1. Pin Mapping FpBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	A8	A10N	A10	A11	A11N	NC DGND	DR	B11N	B11	B10	B10N	B8	DGND	A
B	NC DGND	NC DGND	A8N	NC DGND	A9	NC DGND	NC DGND	DRN	NC (DGND)	B9	NC DGND	B8N	NC DGND	NC DGND	B
C	A6N	NC DGND	NC DGND	NC DGND	A9N	NC DGND	DGND	DGND	NC (DGND)	B9N	NC DGND	NC DGND	NC DGND	B6N	C
D	A6	A7	A7N	DGND	DGND	VCCO	VCCO	VCCO	VCCO	DGND	DGND	B7N	B7	B6	D
E	NC (DGND)	PCB_AN	PCB_A	DGND	DGND	VCCO	VCCO	VCCO	VCCO	DGND	DGND	PCB_B	PCB_BN	NC (DGND)	E
F	NC (DGND)	A5	A5N	VCCO	VCCO	AGND	AGND	AGND	AGND	VCCO	VCCO	B5N	B5	NC (DGND)	F
G	A4	A4N	NC (DGND)	NC (DGND)	DGND	AGND	AGND	AGND	AGND	DGND	NC (DGND)	NC (DGND)	B4N	B4	G
H	A3	A3N	NC (DGND)	NC (DGND)	DGND	AGND	AGND	AGND	AGND	DGND	NC (DGND)	NC (DGND)	B3N	B3	H
J	A2N	A0	A0N	VCC3	VCC3	AGND	AGND	AGND	AGND	VCC3	VCC3	B0N	B0	B2N	J
K	A2	NC (DGND)	NC (DGND)	DGND	DGND	AGND	VCC5	VCC5	AGND	DGND	DGND	NC DGND	NC DGND	B2	K
L	A1	NC (DGND)	NC (DGND)	DGND	RS	VCC5	VCC5	VCC5	VCC5	DGND	mosi	mode_n	NC DGND	B1	L
M	A1N	NC (DGND)	GA	OA	TM_n	VCC5	VCC5	AGND	AGND	SDA	SDAEN_ n	reset_n	NC DGND	B1N	M
N	NC (DGND)	DIODEC	SYNCN	DGND	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	SA	reserved	CMIREF	N
P	DGND	DIODEA	SYNC	DGND	CLK	AGND	AGND	AGND	VIN	VINN	AGND	sclk	sld_n	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 3-1. Pin Description FpBGA

Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
POWER SUPPLIES				
V_{CC5}	L6, L7, L8, L9, M6, M7, K7, K8	5.2V analog supply (Front-end Track & Hold circuitry) Referenced to AGND	N/A	
V_{CC3}	J4;J5;J10;J11	3.3V power supply (ADC Core, Regeneration and Logic, DEMUX circuitry and Timing circuitry) Referenced to AGND	N/A	
V_{CCO}	F4;F5;D6;E6;D7;E7;D8;E8;D9;E9; F10;F11	2.5V digital power supply (output buffers) Referenced to DGND	N/A	

Table 3-1. Pin Description FpBGA (Continued)

Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
DGND	A1;A14;C7;C8;D4;D5;D10;D11;E4; E5;E10;E11;G5;G10;H5;H10;K4; K5;K10;K11;L4;L10;P1;P14,N4, P4	Digital Ground DGND should be separated from AGND on board (the two planes can be reunited via 0 ohm resistors)	N/A	
AGND	F6;F7;F8;F9;G6;G7;G8;G9;H6;H7 H8;H9;J6.J7;J8;J9;K6;K9;M8;M9;N6 N7;N8;N9;N10;N11;P6;P7;P8;P11	Analogue Ground AGND should be separated from DGND on board (the two planes can be reunited via 0 ohm resistors)	N/A	
ANALOG INPUTS				
VIN VINN	P9 P10	Analogue input (differential) with internal common mode Analogue input is sampled and converted (12-bit) on each positive transition of the CLK input. Equivalent internal differential 100Ω input resistor.	I	
CLOCK INPUTS				
CLK CLKN	P5 N5	Master sampling clock input (differential) with internal common mode. It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	
RESET INPUT				
SYNC SYNCN	P3 N3	Reset input (active low). It is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is Synchronous, it is LVDS compatible.	I	
DIGITAL OUTPUTS				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	J2;J3 L1;M1 K1;J1 H1;H2 G1;G2 F2;F3 D1;C1 D2;D3 A2;B3 B5;C5 A4;A3 A5;A6	In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0…11) Differential LVDS signal A0 is the LSB, A11 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio. Each of these outputs should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 3-1. Pin Description FpBGA (Continued)

Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	J13;J12 L14;M14 K14;J14 H14;H13 G14;G13 F13;F12 D14;C14 D13;D12 A13;B12 B10;C10 A11; A12 A10;A9	In-phase (Bi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0…11) Differential LVDS signal B0 is the LSB, B11 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio. Each of these outputs should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	
PCB_A PCB_AN	E3; E2	Parity Check Bit port A	O	
PCB_B PCB_BN	E12 E13	Parity Check Bit port B	O	
DR DRN	A8 B8	In-phase (DR) and inverted phase (DRN) global data ready digital output clock Differential LVDS signal The differential digital output clock is used to latch the output data on rising and falling edge. The differential digital output clock rate is (CLK/2) divided by the DMUX ratio. This differential digital output clock should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	
ADDITIONAL FUNCTIONS				
reserved	N13	Reserved/ To keep NC	I	Driving by resistor: 10 ohm or 10 kohm Driving by voltage: 0.5 V or 2V
TM_n	M5	Test Mode	I	
RS	L5	DEMUX Ratio Selection	i	
SDAEN_n	M11	Sampling delay adjust enable	I	
SDA	M10	Sampling delay adjust	I	Variation on AP node: from 2/(VCC3/3) –0.5V to 2/(VCC3/3) + 0.5V
GA	M3	Gain Adjust	I	
OA	M4	Offset Adjust	i	
SA	N12	Reserved	I	must be connected to 2.2V through a potential divider or NC
mode_n	L12	3WSI Enable “1” ‡ 3WSI not active “0” --< 3WSI active	I	
sclk	P12	3WSI write only clock. Serial data on mosi signal is shifted into 3WSI synchronously to this signal on positive transition of sclk	I	
mosi	L11	3WSI write only serial data input. Shifted into 3WSI while sld_n is active (low).	I	

Table 3-1. Pin Description FpBGA (Continued)

Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
Sld_n	P13	3WSI write only Serial load enable input. When this signal is active (low), sclk is used to clock data present on mosi signal.	I	
CMIRef	N14	Input common mode		Should not be connected.
Reset_n	M12	3WSI write only asynchronous reset input signal. This signal allows to reset internal values of the 3WSI to their default value.	I	
DIODEA	P2	Die Junction temperature monitoring (anode)		
DIODEC	N2	Die Junction temperature monitoring (cathode)		
NC(DGND)	A7;B1;B2;B4;B6;B7;B9;B11;B13;B14 C2;C3;C4;C6;C9;C11;C12;C13 E1;F1;E14;F14;G3;G4;G11;G12;H3 H4;H11;H12;K2;K3;K12;K13;L13;L2 L3;M2;M13;N1	Non connected pins, to be connected on board to DGND		

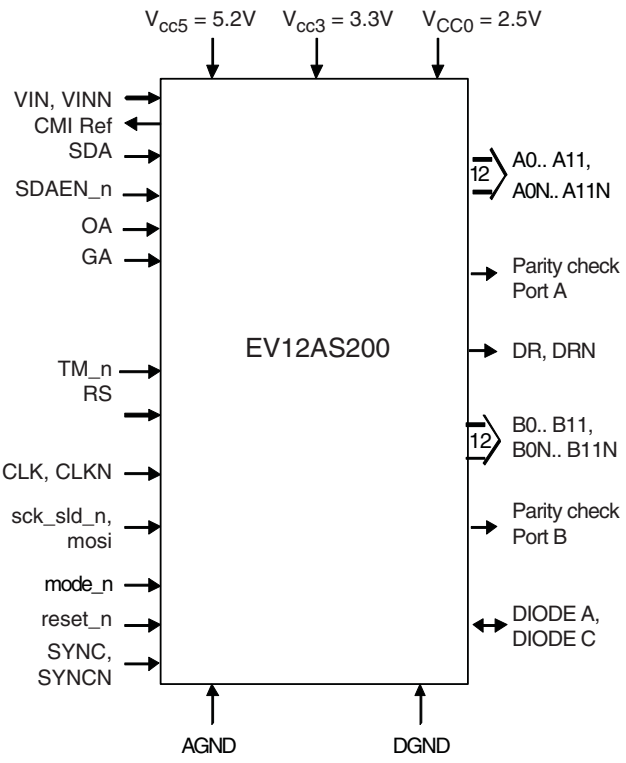
4. Functional Description

4.1 List of Functions

- External synchronous LVDS reset (SYNC, SYNCN)
- Write only 3WSI-like digital interface (gain, offset, sampling delay adjust, DMUX ratio selection, test modes)
- ADC Gain adjust
- ADC Offset adjust
- Sampling delay adjust
- Dynamic Test Mode (alignment sequence)
- Data Ready common to the 2 output ports
- HSR function (High speed mode)
- RES function (Reset function)
- TRIGGER function
- Power on RESET

Table 4-1. Function Descriptions

Name	Function
V_{CC5}	5.2V Power supply
V_{CC3}	3.3V Power supply
V_{CC0}	2.5V Power supply
GND	Ground
GNDO	Digital Ground for outputs
VIN,VINN	Differential Analog Input
CLK,CLKN	Differential Clock Input
[A0:A11] [A0N:A11N]	Differential Output Data on port A
PCB_A, PCB_AN	Parity check bit port A
[B0:B11] [B0N:B11N]	Differential Output Data on port B
PCB_B, PCB_BN	Parity check bit port B
DR,DRN	Global Differential Data Ready
RS	DEMUX Ratio select
SYNC, SYNCN	External reset
TM_n	Test Mode Enable
SDA	Sampling Delay Adjust input
SDAEN_n	Sampling Delay Adjust Enable
GA	Gain Adjust input.
OA	Offset adjust input
DIODEA, DIODEC	Diode for die junction temperature monitoring
Sck, sld_n, reset_n, mosi, mode_n	3WSI write only pins
CMIRef	Input common mode



The different functions could be enabled by external dedicated command pin and/or 3WSI interface according the table below.

Table 4-2. ADC Mode Settings – Summary of External Control by the 3WSI

Function	3WSI	External command pin	Description
TM_n	yes	yes	Test mode ON/OFF (Active LOW)
TESTTYPE	yes (2 bits)	no	Test Type: dynamic or static pattern (static pattern: 3WSI only)
SDAEN_n	yes	yes (fine only)	Sampling Delay Adjust ON/OFF (Active LOW)
SDA_fine	yes (8 bits)	yes (2,2V ±0,5V)	SDA Fine tuning (0 -> 255 for 3wsi or 1,7V -> 2,7V external)
SDA_coarse	yes (2 bits)	no	SDA Coarse tuning (3WSI Only) : "00" -> 0ps, "01" -> 30ps, "10" -> 60ps, "11" -> 90ps
RS	yes	yes	Demux Ratio Select : "1" : 1:2 mode, "0" : 1:1 mode
GAIN ADJUST	yes (10 bits)	yes (2,2V ±0,5V)	Gain Adjust (0 -> 1023 for 3wsi or 1,7V -> 2,7V external)
OFFSET ADJUST	yes (10 bits)	yes (2,2V ±0,5V)	Offset Adjust (0 -> 1023 for 3wsi or 1,7V -> 2,7V external)
mode_n	no	yes	3wsi ON/OFF (Active LOW, all other settings are external if OFF)
trig_sel_n	yes	no	SYNC Behavior : "1" : Trigger Mode, "0" : Syncronization Mode
RES	yes	no	SYNC Active Edge ("1" : falling, "0" : rising)
HSR	yes	no	Sampling Rate Mode (1:1 demux ratio) : "1" : Half speed, "0" : Full Speed

4.2 External Reset (SYNC, SYNCN)

An external LVDS reset (SYNC, SYNCN) is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is LVDS compatible. It is active high but the logical value could be changed using the RES function, see Section 4.10 ”RES Function” on page 32. It is asynchronous but is relatched internally to the sampling clock.

4.3 Mode (mode_n) Function

It is possible to activate the digital interface via the mode_n signal, external command.

The coding table for the mode is given in Table 4-3.

Table 4-3. Mode Coding

Function	Logic Level	Electrical Level	Description
Mode_n	0	10Ω to ground	Digital interface active
	1	10 KΩ to ground	Digital interface inactive (default mode)
		N/C	

Description of the 3WSI interface is provided in Section 4.13 on page 33.

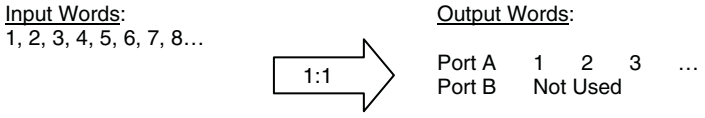
When the 3WSI functions are activated (mode_n active), the hardware commands are disabled.

When the hardware commands are activated (mode_n disabled), the values of the register can not be modified and are set to default.

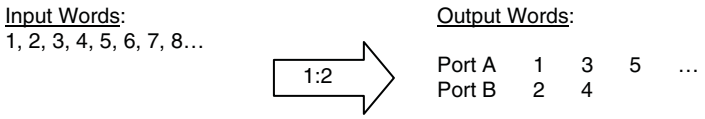
4.4 DEMUX Ratio Select (RS) Function

Two DEMUX Ratios can be selected via the RS pin or via the 3WSI.

ADC in 1:1 Ratio



ADC in 1:2 Ratio



Note that Data of the different ports are synchronous: they appear at the same instant on each port.

4.4.1 DEMUX ratio selection with the external command (RS pin)

Two DEMUX Ratios can be selected using the pin RS according to the table below.

Table 4-4. Ratio Select Coding

Function	Logic Level	Electrical Level	Description
RS	0	10Ω to ground	1:1 DEMUX Ratio (Port A)
	1	10 KΩ to ground	1:2 DEMUX Ratio (Ports A and B)
		N/C	

4.4.2 DEMUX Ratio Selection with 3WSI

This mode is selectable when WSI interface (Mode_n = 0) is activated and when the bit D0 of the state register is set to 0.

Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

Table 4-5. State Register Coding

Label		Coding	Description	Default Value
RS	D0	0	1:1 DMUX mode	1
		1	1:2 DMUX mode	

4.5 Test Mode (TM_n) Function

This mode can be selected using pin TM_n according to the table below or 3WSI interface.

4.5.1 Test Mode with the external command (TM_n pin)

One dynamic test mode is made available in order to test the outputs of the ADC; this test mode corresponds to a pseudo random sequence with a period of 16.
The coding table for the Test mode is given in Table 4-6.

Table 4-6. Test Mode Coding

Function	Logic Level	Electrical Level	Description
TM_n	0	10Ω to ground	Alignment pattern ON (period of 16) see Figure 4-1
	1	10 KΩ to ground	Normal conversion mode (default mode)
		N/C	

4.5.2 Test Mode with 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated and when the bit D2 of the stare register is set to 0.

Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

Description

Table 4-7. Test Register Coding (Address 0101)

Label	Coding	Description	Default Value
TEST TYPE <1:0>	00	VOL Test mode ON	11
	01	VOH Test mode ON	
	10	Unused	
	11	Alignment Pattern ON (period 16)	

Test Mode functionalities

Notes: Alignment pattern is described in Figure 4-1 on page 29.

The alignment pattern is used to provide validation at full speed of interface between ADC and FPGA in both DMUX 1:1 or DMUX 1:2 modes. Verification of synchronization of output data between different ADC (Output data shift after external synchronization pulse).

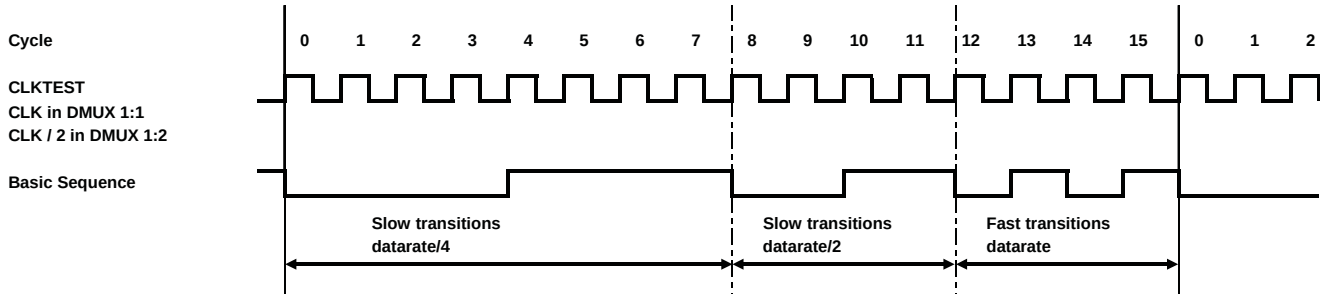
Basic Sequence

Period of 16 cycles of output datarate.
Slow transitions at datarate/4 or datarate/2 (full swing).
Fast transitions at datarate (reduced swing).
Easy to use for synchronization (start with four consecutive “0”).

Output Data

Adapted to DMUX mode to have validation at full datarate in each mode.
Same data between port A and Port B in DMUX 1:2 mode
Parity Bit (PC) handled like other bits (no parity calculation) during Test mode.

Figure 4-1. Alignment Pattern Timing Diagram



4.6 Sampling Delay Adjust (SDA)

Sampling delay adjust (SDA pin) allows to tune the sampling ADC aperture delay (TA) around its nominal value.

This feature is particularly useful for interleaving ADCs to increase sampling rate.

This function can be activated either by external command or the 3WSI.

4.6.1 Sampling Delay Adjust (SDA) Function with the External Command (SDA Pin)

This functionality is enabled by the SDAEN_n signal, which is active at low level (when tied to ground) and inactive at high level (10 KΩ to Ground, or tied to V_{CC3} = 3.3V, or left floating).

The coding table for the SDAEN_n is given in Table 4-8.

Table 4-8. SDAEN_n Coding

Function	Logic Level	Electrical Level	Description
SDAEN_n	0	10 Ω to ground	Sampling delay adjust enabled
	1	10 KΩ to ground	Sampling delay adjust disabled
		N/C	

Description :

With the external command (SDA pin), it is possible to tune the sampling ADC aperture delay by applying a control voltage on SDA pin.

Typical tuning range is from 0 to 30 ps for applied control voltage varying between ± 0.5V around $2*V_{CC3}/3$.on SDA pin.

This tunable delay is in addition to the default value for coarse SDA fixed in the 3WSI register (~60 ps). If not used, this function should be disabled via SDAEN_n set to high level.

4.6.2 Sampling Delay Adjust (SDA) Function with 3WSI Interface

This mode is selectable when 3WSI interface (Mode_n = 0) is activated and when the bit D1 (SDAEN_n) of the stare register is set to 0.

Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

Description

Table 4-9. SDA Register Mapping (Address 0011)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NC	NC	SDA coarse<1:0>		SDA fine <7:0>							

Table 4-10. SDA Register Description

Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
Sampling Delay Adjust coarse	0x02	60 ps	0x03	90 ps	0x00	0 ps	30 ps
Sampling Delay Adjust fine	0x00	0 ps	0xFF	30 ps	0x00	0 ps	120 fs

Total SDA delay is given by SDA coarse value in addition to SDA fine value.
SDA coarse register [1:0] allows a variation step of 0, 30 ps, 60 ps or 90 ps.
SDA fine register [7:0] allows a fine step of 120fs between a range of 0 to 30 ps

So the Sampling Delay adjusts with the 3WSI interface could vary from 0 ps up to 120 ps with a step of 120 fs.

4.7 Gain Adjust (GA) Function

This function allows adjusting ADC Gain so that it can always be tuned to 1.0
This function can be activated either by external command or the 3WSI.

4.7.1 Gain Adjust Function with the External Command (GA Pin)

The ADC Gain can be tuned by ±10% by tuning the voltage applied on GA by ± 0.5V around $2*V_{CC}/3$.

4.7.2 Gain Adjust Function with the 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated.

Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

Description

Table 4-11. GA Register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

The ADC Gain can be tuned by ±10% by step of 0.8 LSB.

Table 4-12. GA Register Description

Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
GA register <9:0>	0x200	1 (500 mVpp 4096 LSB)	0x3FF	1.10 (550 mVpp 4506 LSB)	0x000	0.90 (450 mVpp 3686 LSB)	0.0002 (0.097 mV 0.8 LSB)

4.8 Offset Adjust (OA) Function

This function allows to adjust ADC Offset so that it can always be tuned to mid-code 2048.
This function can be activated either by external command or the 3WSI.

4.8.1 Offset Adjust Function with the External Command (OA Pin)

The ADC Offset can be tuned by ±150 LSB (typ) (± 18.3 mV) by tuning the voltage applied on OA by ± 0.5V around $2*V_{CC3}/3$.

$2*V_{CC3}/3+0.5V$ gives the most negative offset variation and $2*V_{CC3}/3-0.5V$ gives the most positive offset variation.

4.8.2 Offset Adjust Function with the 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated.
Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

Description

Table 4-13. OA Register Mapping (Address 0010)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		OA<9:0>									

The ADC offset can be tuned by ±195 LSB by step of 0.38 LSB.

Table 4-14. OA Register Description

Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
Offset Adjust	0x200	0 LSB	0x000	±150 LSB (±18.3 mV)	0x3FF	–195 LSB (–23.8 mV)	0.38 LSB (0.046 mV)

4.9 HSR (High Sampling Rate) Function

This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

In DMUX1:1 it allows to output data faster up to 1 GHz instead of half speed (by default) by increasing current of output stages.

Note: There is a small consumption increase.

4.10 RES Function

This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 33.

This function allows changing the active edge of the SYNC signal

4.11 TRIGGER Function

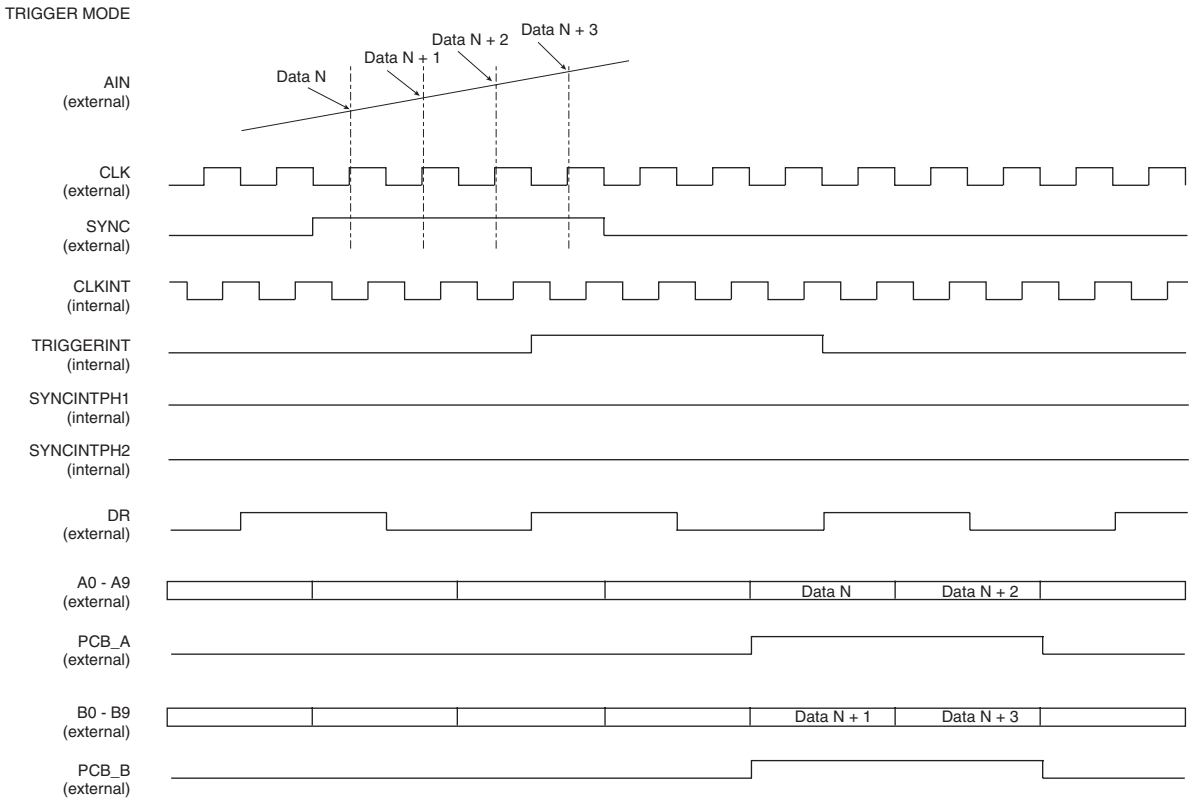
This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.13 on page 33.

This function allows to help to synchronise multiple ADCs.

The pulse applied on SYNC is output after pipeline delay on the Parity Check pins (PCB_A) & (PCB_B) in DMUX 1:2.

Figure 4-2. Trigger Mode Diagram



4.12 Power on Reset

A power on reset ensures synchronisation of internal signals and ensures output data to be properly ordered. It is generated internally by the digital section of the ADC (on V_{CC3} power supply) and is deactivated when V_{CC5} reaches 80% of its steady state.

If V_{CC3} is not applied before V_{CC5} RSTN should be used to synchronize the ADC signals.

4.13 ADC 3WSI Description (ADC Controls)

The digital interface of the ADC is activated via the mode_n signal (active low).

4.13.1 3WSI Timing Description

The 3WSI is a synchronous write only serial interface made of 4 wires:

- “reset_n” : asynchronous 3WSI reset, active low
- “sck” : serial clock input
- “sld_n ” : serial load enable input
- “mosi” : serial data input.

The 3WSI gives a “write-only” access to up to 16 different internal registers of up to 12 bits each. The input format is fixed with always 4 bits of register address followed by always 12 bits of data. **Address and data are entered MSB first.**

The write procedure is fully synchronous with the clock rising edge of “sclk” and described in the write chronogram hereafter.

“sld_n” and “mosi” are sampled on each rising clock edge of “sclk” (clock cycle).
“sld_n” must be set at “1” when no write procedure is done.

A write starts on the first clock cycle with “sld_n” at “0”. “sldn” must stay at “0” during the complete write procedure.

In the first 4 clock cycles with “sld_n” at “0”, 4 bits of register address from MSB (a[3]) to LSB (a[0]) are entered.

In the next 12 clock cycles with “sld_n” at “0”, 12 bits of data from MSB (d[11]) to LSB (d[0]) are entered.

This gives 16 clock cycles with “sld_n” at “0” for a normal write procedure.

A minimum of one clock cycle with “sld_n” returned at “1” is requested to end the write procedure, before the interface is ready for a new write procedure.

Any clock cycle with “sld_n” at “1” before the write procedure is completed interrupts this procedure and no data transfer to internal registers is done.

Additional clock cycles with “sld_n” at “0” after the parallel data transfer to the register (done at 15th consecutive clock cycle with “sld_n” at “0”) do not affect the write procedure and are ignored.

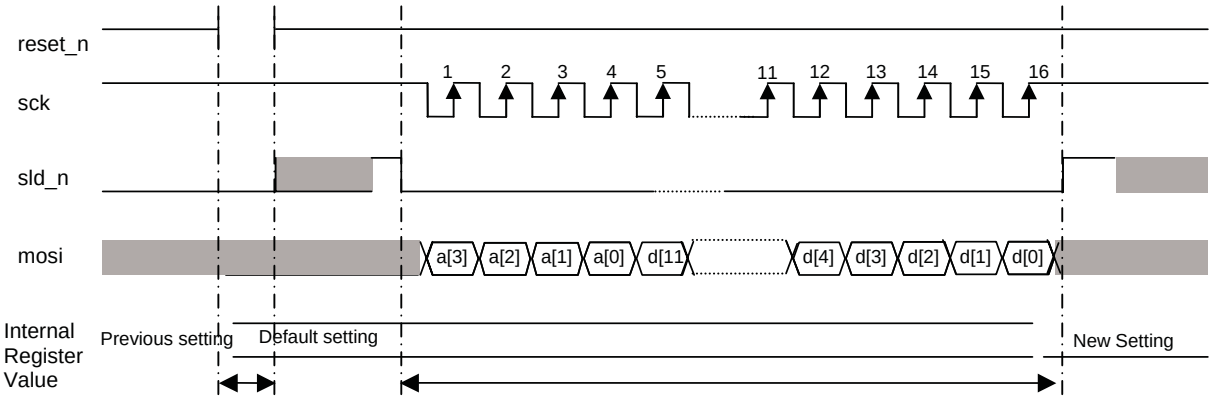
It is possible to have only one clock cycle with “sld_n” at “1” between two following write procedures.

12 bits of data must always be entered even if the internal addressed register has less than 12 bits. Unused bits (usually MSB’s) are ignored. Bit signification and bit position for the internal registers are detailed in the chapter “Registers”.

The “reset” pin combined with the “sld_n” pin can be used as a reset to program the chip to the “reset setting”.

- “reset_n” high: no effect
- “reset_n” low and “sld_n” low: programming of registers to default values

Figure 4-3. 3WSI Timing Diagram



Timings related to 3WSI are given in the table below

Table 4-15. 3WSI Timings

Name	Parameter	Min	Typ	Max	Unit	Note
Tsck	Period of sck	10			ns	
Twsck	High or low time of sck	5			ns	
Tssld_n	Setup time of sldn before rising edge of sck	4			ns	
Thsld_n	Hold time of sld_n after rising edge of sck	2			ns	
Tsmosi	Setup time of mosibefore rising edge of sck	4			ns	
Thmosi	Hold time of sdata after rising edge of sck	2			ns	
Twlreset_n	Minimum low pulse width of reset	5			ns	
Tdreset_n	Minimum delay between an edge of reset and the rising edge of sck	10			ns	

4.13.2 3WSI: Address and Data Description

This 3WSI is activated with the control bit sld_n going low (please refer to “write timing” in next section).
The length of the word is 16 bits: 12 for the data and 4 for the address.
The maximum serial logic clock frequency is 100 MHz.

Table 4-16. Registers Mapping

Address	Label	Description	Default Setting
0000	State Register	DMUX ratio Selection Sampling Delay Adjust Enable Test Mode Enable Output clock division ratio selection Trigger mode selection	0x7FF
0001	GA Register	Gain adjust register	0x200
0010	OA Register	Offset adjust register	0x200
0011	SDA Register	Sampling delay adjust register	0x002
0100		Reserved	0x1F
0101	Test Register	Test modes register	0x03
0110		Reserved	
0111		Reserved	
1000 to 1111		Reserved	

4.13.3 State Register (Address 0000)

Table 4-17. State Register Mapping (Address 0000)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved			TRIG_SEL_N	RES	HSR	Reserved			TM_n	SDAEN_n	RS

Table 4-18. State Register Coding (Address 0000)

Label		Coding	Description	Default Value
RS	D0	0	1:1 DMUX mode	1
		1	1:2 DMUX mode	
SDAEN_n	D1	0	Sampling Delay Adjust function Enabled	1
		1	Sampling Delay Adjust function Disabled	
TM_n	D2	0	Test Mode ON (refer to register at address 0101)	1
		1	Test Mode OFF	
Reserved	D3	1	Should be connected to 1	1
Reserved	D4	1	Should be connected to 1	1
Reserved	D5	1	Should be connected to 1	1
HSR	D6	0	Full Sampling rate mode in 1:1 DMUX Mode ON	1
		1	Half Sampling rate mode in 1:1 DMUX Mode ON	
RES	D7	0	RESET edge select: rising edge	1
		1	RESET edge select: falling edge	
TRIG_SEL_N	D8	0	Trigger mode (Trigger pulse on PCB_X if positive pulse on SYNC. Internal synchronization inhibited, where X = A or B)	1
		1	Synchronization mode (Synchronization of internal functions on positive pulse on SYNC)	
Reserved	D9			1
Reserved	D10			1
Reserved	D11			1

Notes:
1. HSR: when the digital interface is not active, default mode is DMUX 1:1 at half sampling speed. When HSR is set to 0, power consumption will slightly increase in order to allow for 1 GSps operation in DMUX 1:1.
2. Test pattern function “Always running” : Internal synchronization not affected by mode (TM_n) change.
3. Bit D3, D4, D5, D9, D10, D11 are reserved.
4. Synchronization and Trigger modes.

4.13.4 GA Register (Address 0001)

Table 4-19. GA Register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

4.13.5 OA Register (Address 0010)

Table 4-20. OA Register Mapping (Address 0010)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		OA<9:0>									

4.13.6 SDA Register (Address 0011)

Table 4-21. SDA Register Mapping (Address 0011)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		SDA coarse<1:0>		SDA fine <7:0>							

Table 4-22. Registers 0001 to 0100 Summary

Address	Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
0001	Gain Adjust	0x200	1 (500 mVpp 4096 LSB)	0x3FF	1.10 (550 mVpp 4506 LSB)	0x000	0.90 (450 mVpp 3686 LSB)	0.032 (0.195 mV 1.6 LSB)
0010	Offset Adjust	0x200	0 LSB	0x000	+50 LSB (typ) (+18.3 mV)	0x3FF	–50 LSB (typ) (–18.3 mV)	0.25 LSB (0.03 mV)
0011	Sampling Delay Adjust coarse	0x02	60 ps	0x03	90 ps	0x00	0 ps	30 ps
	Sampling Delay Adjust fine	0x00	0 ps	0xFF	30 ps	0x00	0 ps	120 fs

Note: 1. Reserved.

4.13.7 Test Register (Address 0101)

Table 4-23. Test Register Mapping (Address 0101)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<Unused>										TEST TYPE	

5. Characterisation Information

Figure 5-1. Normalized Full Power Input Bandwidth at –1 dBFS and –10 dBFS

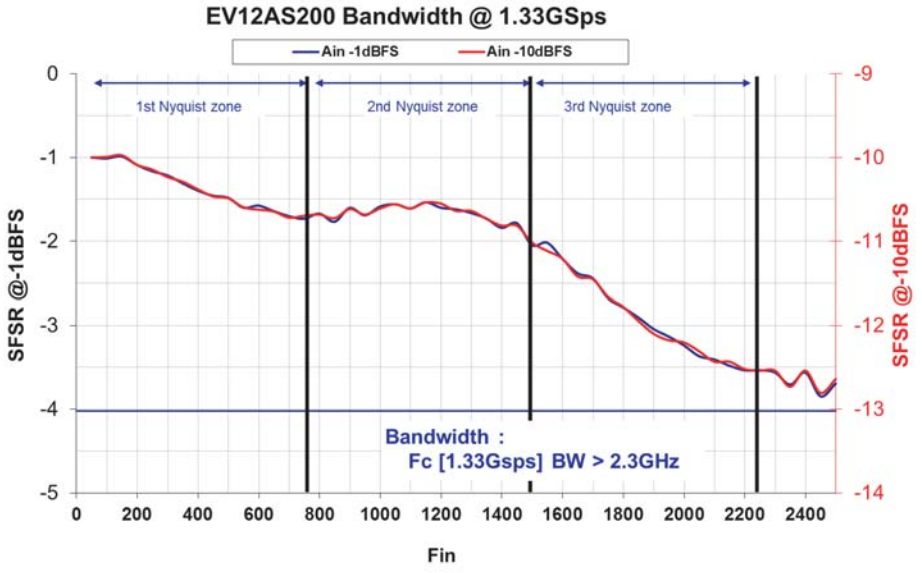


Figure 5-2. ENOB vs Fin Fclk = 1.5 GHz (No Look Up Table Correction)

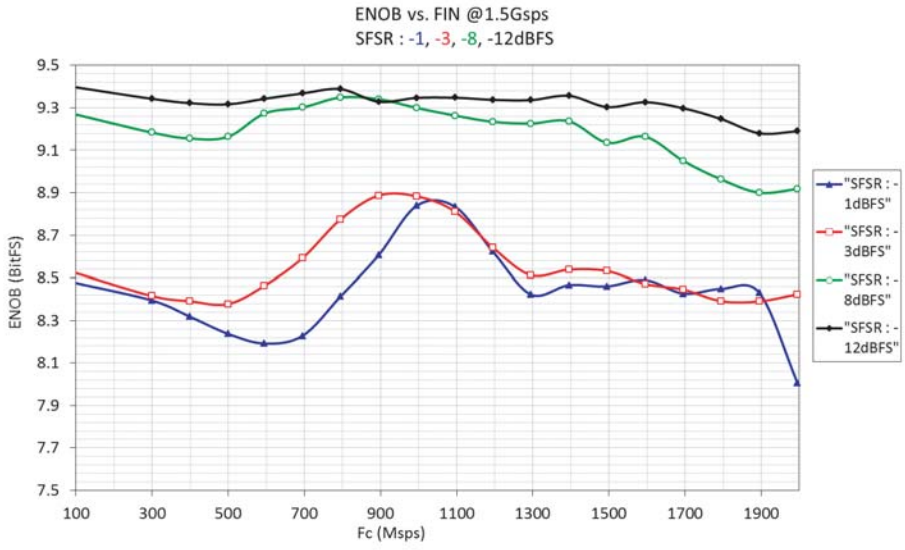


Figure 5-3. SFDR vs Fin (No Look Up Table correction).

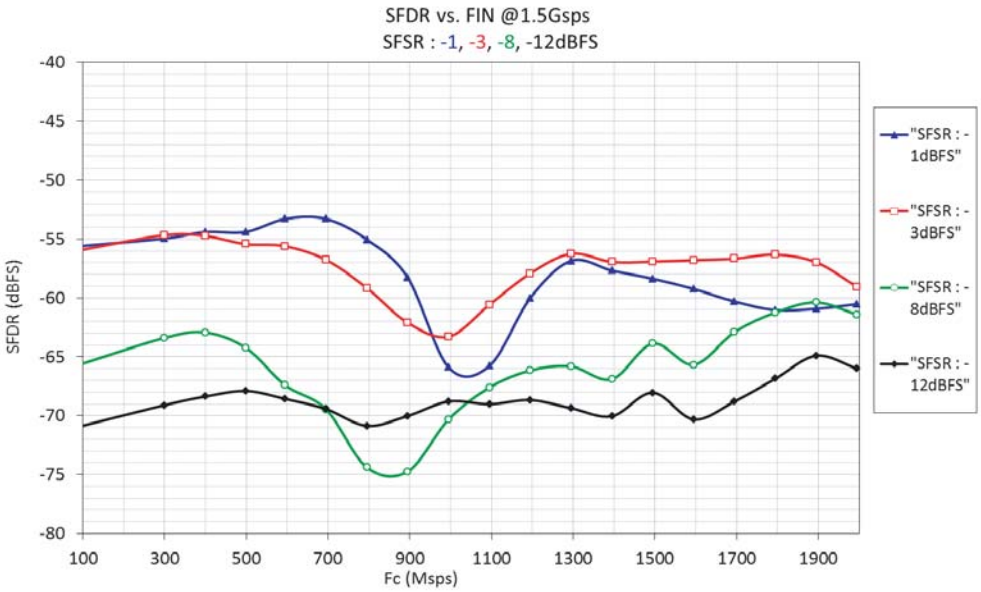


Figure 5-4. Spectral Purity (non-signal dependant spurs < –90 dBc)

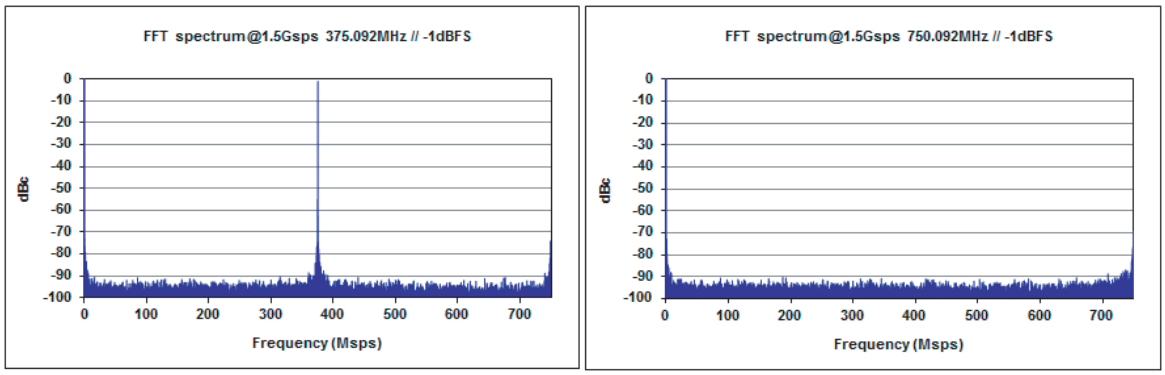
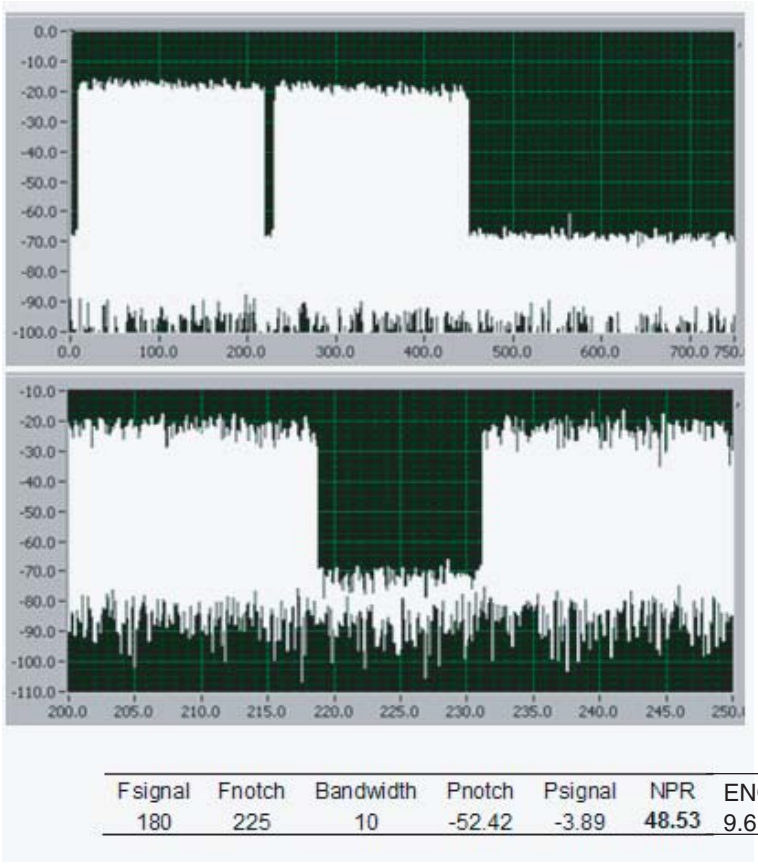


Figure 5-5. NPR Measurement using notch centred on 225 MHz



Fsignal	Fnotch	Bandwidth	Pnotch	Psignal	NPR	ENOB
180	225	10	-52.42	-3.89	48.53	9.6

Figure 5-6. 3rd Order Intermodulation Products Fin 1460 MHz 1450 MHz

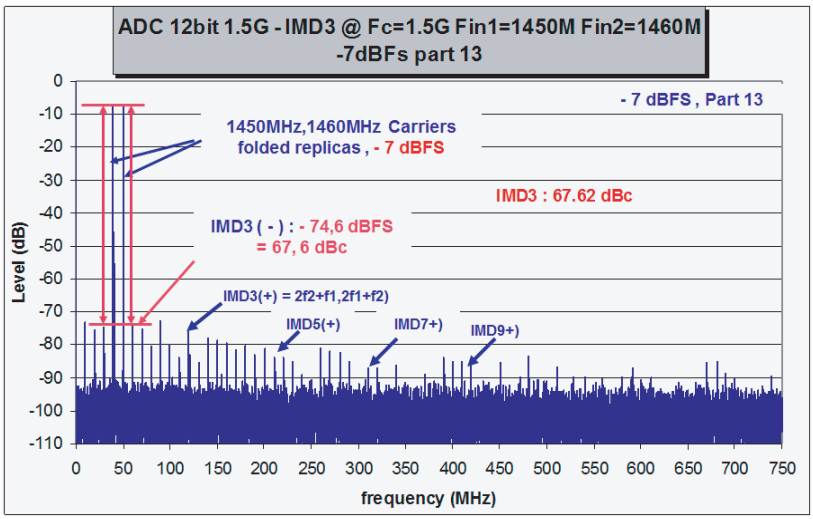
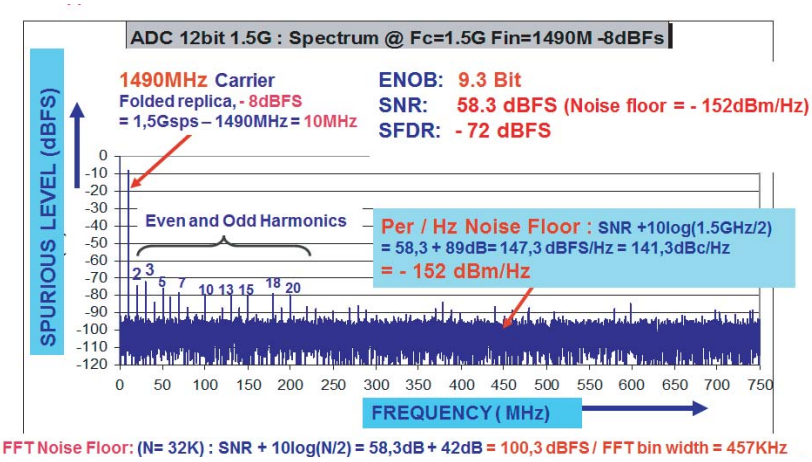


Figure 5-7. Noise Floor



- Single tone Noise Performance (SNR): –1 dBFS
  SNR = 56.5 dBFS, –1 dBFS at 1.5 Gsps Fin 1490 MHz
  (-> ADC intrinsic (measured) Jitter = ~100 fs rms)
- Noise Floor performance @ 1.5 Gsps / Fin = 1500 MHz, –1 dBFS
  SNR + 10log (1.5 GHz/2) = 56.5 dB + 10log (750 MHz) = 56.5 dB + 89 dB
  = 145.5 dBFS/Hz = 144.5 dBc/Hz = –150.5 dBm/Hz

  Reminder: (ADC Full Scale Input Power: 0.5 Vpp / 100Ω = –5 dBm)

- A noise Floor of –150 dBm Hz corresponds to:
- In 750 MHz Bandwidth (1st Nyquist or 2nd Nyquist): 9.1 Bit ENOB
  (= Full Nyquist region: entire 2nd Nyquist Band)
  (from SNR = 56.6 dBFS at 1.5 Gsps / Fin = 1490 MHz, –1 dBFS)
- In 10 MHz Bandwidth: 13 Bit ENOB !
  (from 150 dBm – 10log(10 MHz) = 150 – 70 dB = 80 dB : = 13 Bit ENOB

6. Applications

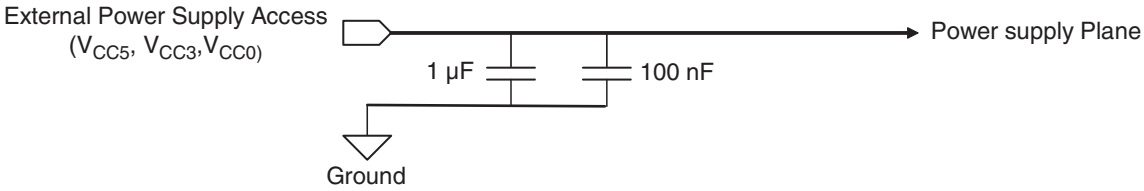
6.1 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Each incoming power supply should be bypassed at the board input by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor. Each power supply is decoupled as close as possible to the EV12AS200ZPY device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

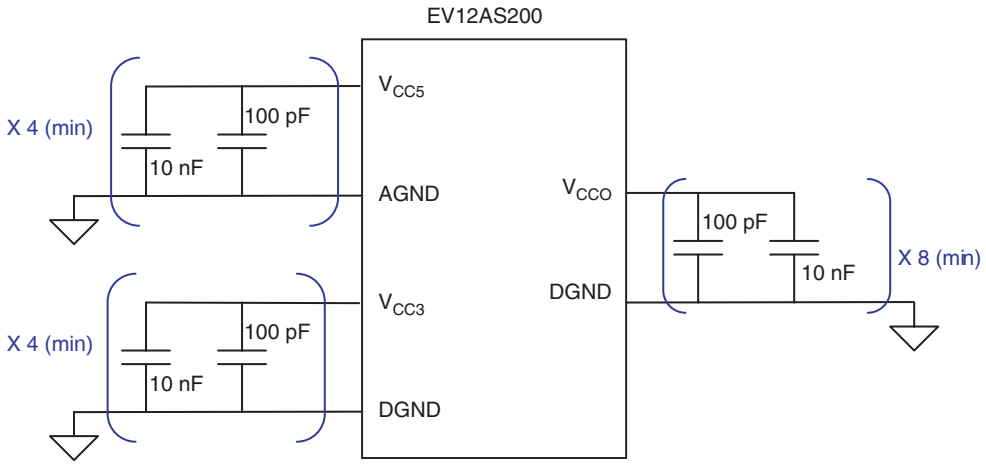
Figure 6-1. EV12AS200 Power Supplies Decoupling and Grounding Scheme



Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required number of pairs of capacitors by power supply type is:
4 for V_{CC5}
4 for V_{CC3}
8 for V_{CCO}

Figure 6-2. EV12AS200 Power Supplies Bypassing Scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 1µF capacitors.

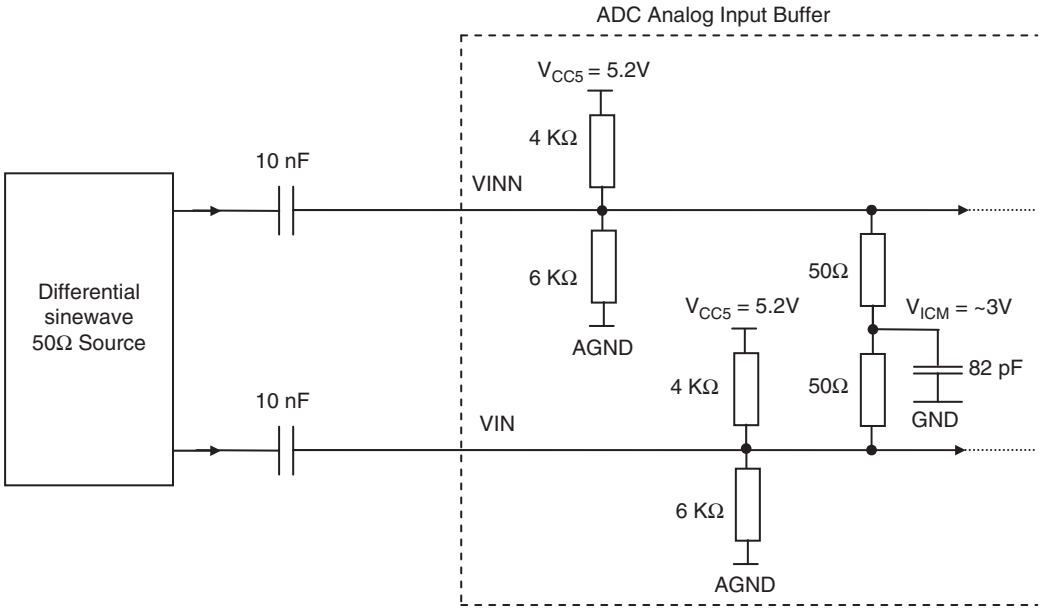
6.2 Analogue Inputs (VIN/VINN)

The analogue input should be used in differential mode. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

6.2.1 Differential Analog Input

The analogue input should be AC coupled as described in Figure 6-3.

Figure 6-3. Differential Analogue Input Implementation (AC Coupled)

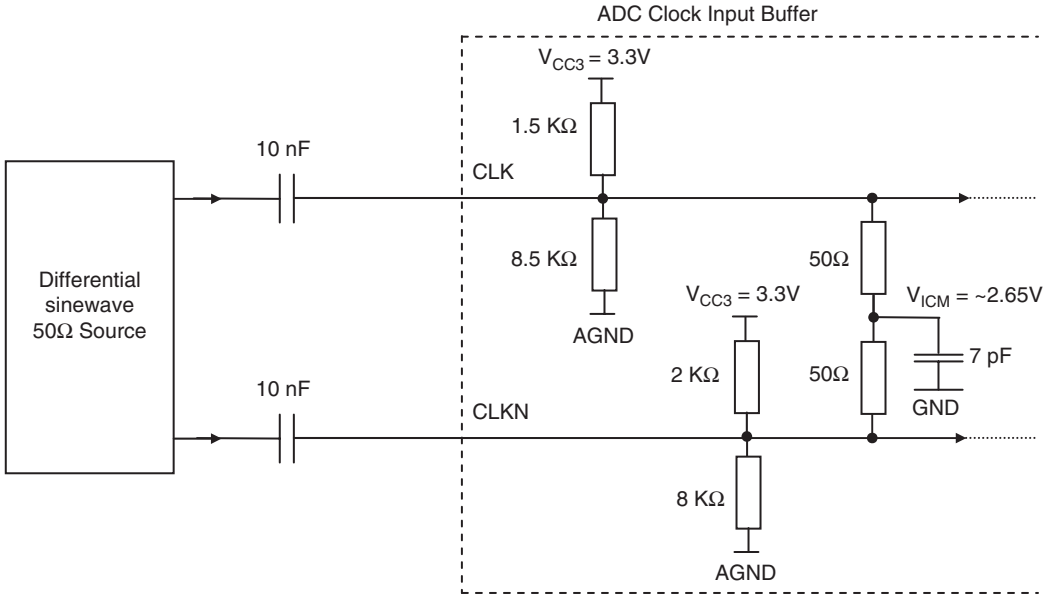


6.3 Clock Inputs (CLK/CLKN)

Differential mode is the recommended input scheme. Single-ended clock input is not recommended due to performance limitations. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

Since the clock input common mode is 2.65V, we recommend to AC couple the input clock as described in Figure 6-4.

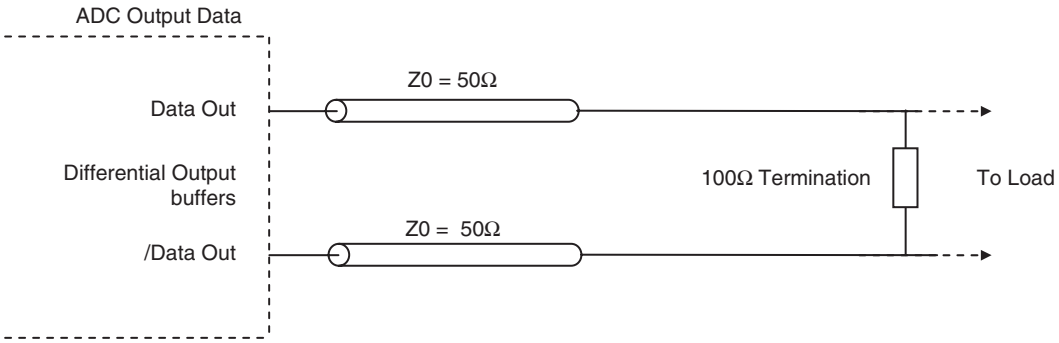
Figure 6-4. Differential Clock Input Implementation (AC Coupled)



6.3.1 Digital Outputs

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 6-5. Differential Digital Outputs Terminations (100Ω LVDS)



If the ADC is used in 1:1 or 1:2 DMUX modes, the unused ports can be left open (no external termination required).

6.3.1.1 Analogue Inputs/Clock Input

The following dimensions are recommended.

50Ω lines matched to ± 0.1 mm (in length) between VIN and VINN or CLK and CLKN.

6.3.1.2 Digital Output Data

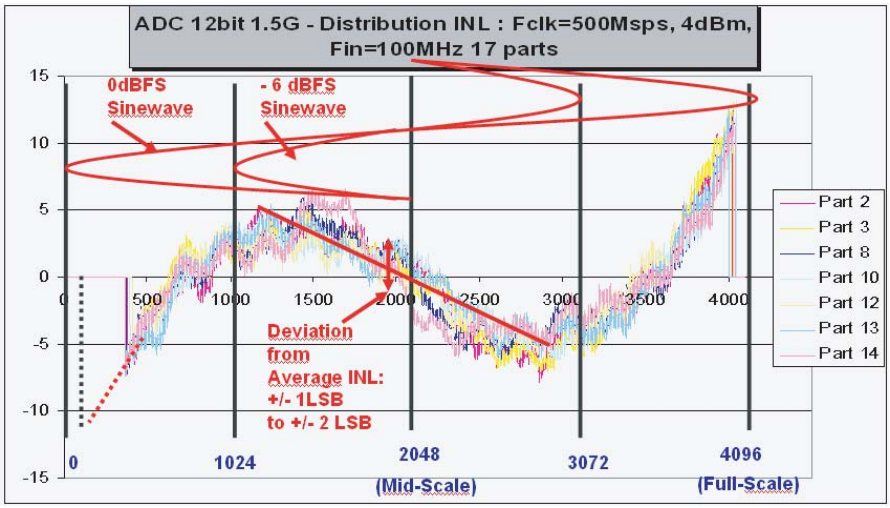
The high speed differential output signals (digital output, data ready output), should be routed in parallel with 50 ohm impedance, 370 µm width and a pitch of 0.77 mm.

Max difference between any two signals = ±1 mm. (implying ± ~12 ps skew)

6.3.2 Improving SFDR and ENOB using a LUT

The plot of the INL shows an S shape. This causes a high third harmonic at larger input signal amplitudes.

Figure 6-6. INL Curve

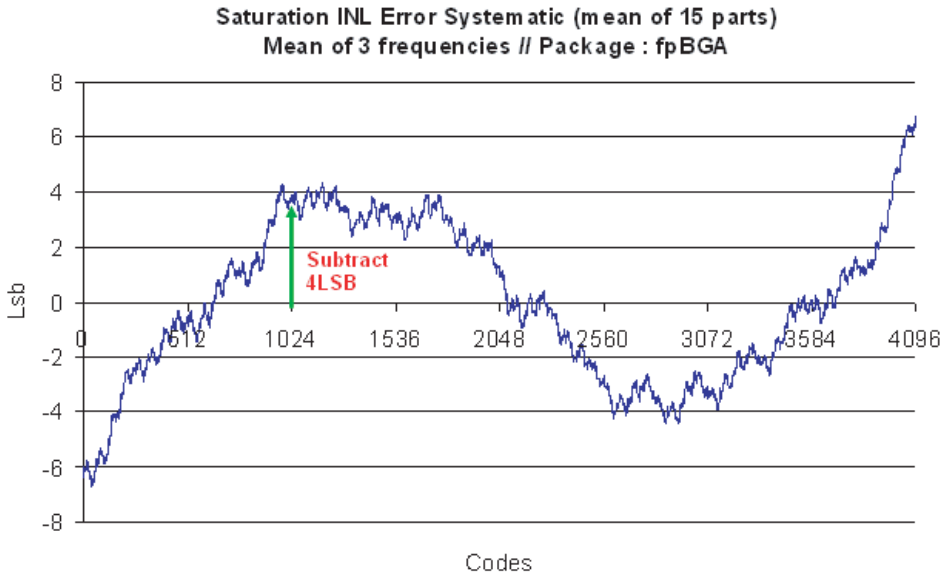


The figure above shows that a large amplitude signal will see large variation in INL which will cause non-linearity of response and hence higher harmonics; whereas the smaller signals are mainly in a linear part of the INL curve.

The INL shape has been measured over multiple parts and over temperature and supply and has been seen to be stable. This gives the possibility to calibrate for the INL in a post processing stage.

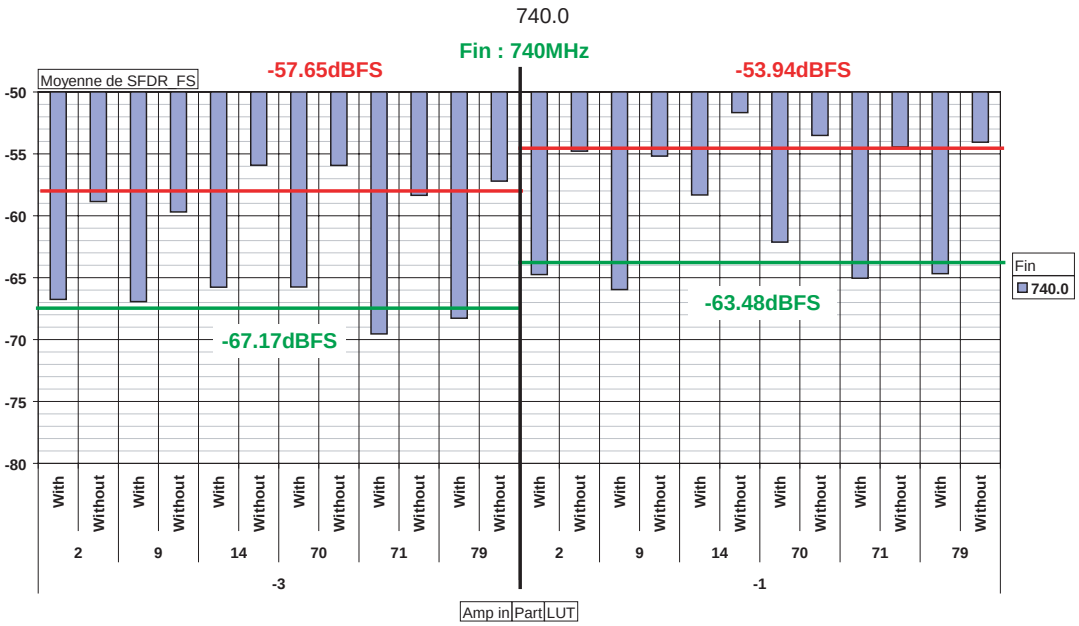
This calibration stage simply adds or subtracts a the relevant number of LSBs given by the INL calibration shape for the amplitude of the sampled signal.

Figure 6-7. INL Calibration



The image below shows the improvement gained in SFDR by using this calibration look up table.

Figure 6-8. Look Up Table Improvement on SFDR



The image shows the improvement obtained using the LUT on 6 parts at an input amplitude of –1 dBFS and –3 dBFS.

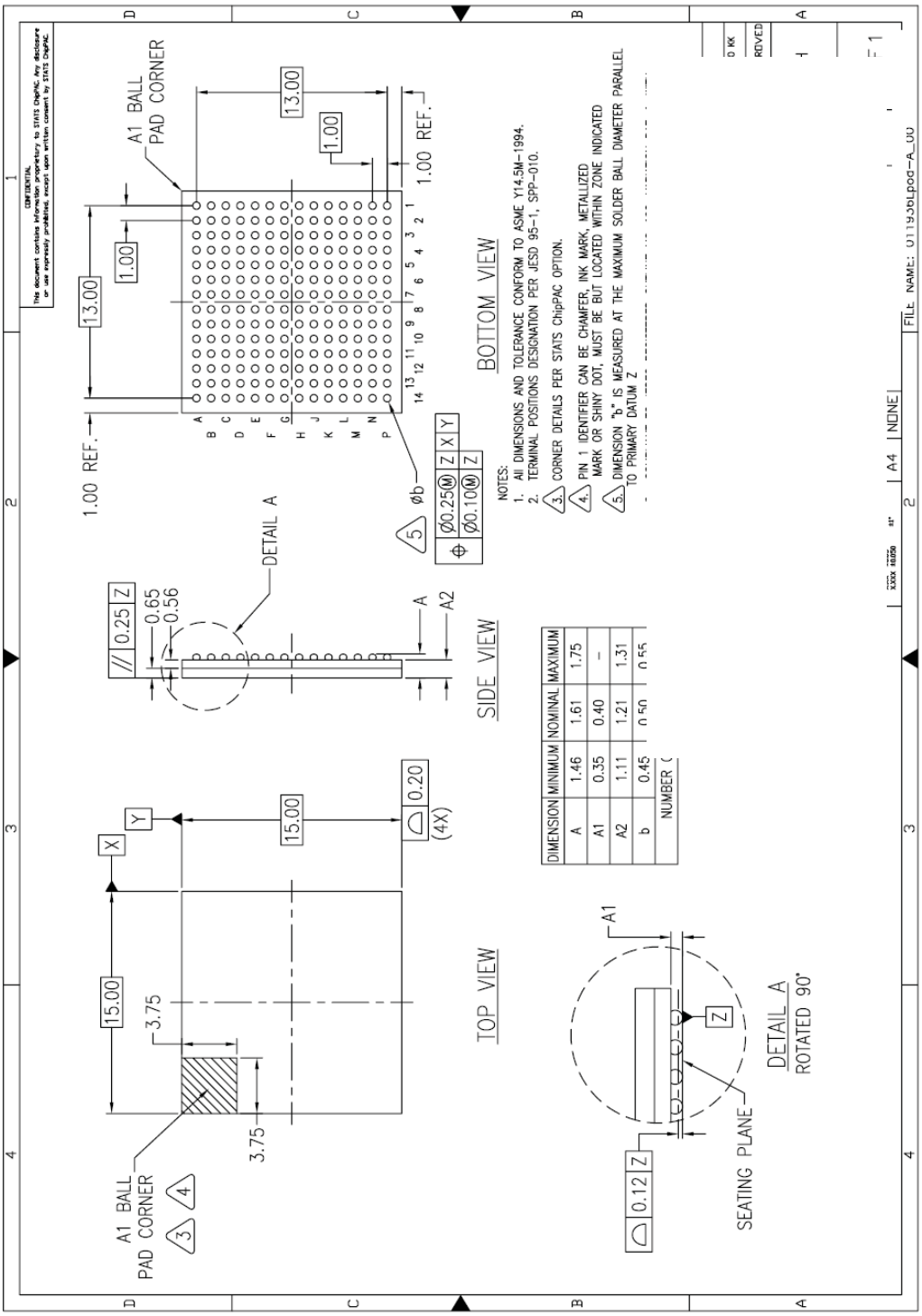
6.3.3 Operation at 1.5 GSps

Operation at 1.5 GSps will be achieved more easily if the conditions outlined below are followed:

1. T_J <= 90°C
2. V_{CCA3} at higher limit of range.
3. The interface system (typically an FPGA) allows the fine delay adjustment of each data bit with respect to the Data Ready signal. Also the PCB traces of each data bit and the Data Ready signal should be matched to ±1 mm maximum.

7. Package Description

7.1 FpBGA Package Outline



7.2 Thermal Characteristics fpBGA196

7.2.1 Thermal Resistance

Assumptions:

- Still air
- Pure conduction
- No radiation
- Heating zone = 8% of die surface

Rth Junction -bottom of Balls = 12.8°C/W

Rth Junction - board (JEDEC JESD-51-8) = 17.2°C/W

Rth Junction -top of case = 13.5°C/W

Assumptions:

- Heating zone = 5% of die surface
- Still air, Jedec condition

Rth Junction - ambient (JEDEC) = 31.2 °C/W

8. Ordering Information

Table 8-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12AS200ZPY	fpBGA196 RoHS	Ambient	Prototype	
EV12AS200ZPY-EB	fpBGA196 RoHS	Ambient	Prototype	Evaluation board
EV12AS200CZPY	fpBGA196 RoHS	Commercial $0°C < T_C$ $T_J < 90°C$	Standard	
EV12AS200VZPY	fpBGA196 RoHS	Industrial $–40°C < T_C$ $T_J < 110°C$	Standard	
EV12AS200ZPY-DK		Demonstration kit		Consult e2v for avaibility

Table of Contents

How to reach us

Home page: www.e2v.com

Sales offices:

Europe Regional sales office

e2v ltd

106 Waterhouse Lane

Chelmsford Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax: +44 (0)1245 492492

mailto: enquiries@e2v.com

e2v sas

16 Burospace

F-91572 Bièvres Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

mailto: enquiries-fr@e2v.com

e2v Aerospace and defense inc

765 Sycamore Drive

Milpitas

California 95035

USA

Tel: +33 (0) 1 408 737 0992

Fax: +33 (0) 1 408 736 8708

mailto: e2v-us.com

Americas

e2v inc

520 White Plains Road

Suite 450 Tarrytown, NY 10591

USA

Tel: +1 (914) 592 6050 or 1-800-342-5338,

Fax: +1 (914) 592-5148

mailto: enquiries-na@e2v.com

Asia Pacific

e2v ltd

11/F.,

Onfem Tower,

29 Wyndham Street,

Central, Hong Kong

Tel: +852 3679 364 8/9

Fax: +852 3583 1084

mailto: enquiries-ap@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

mailto: hotline-bdc@e2v.com