TMC208K, TMC28KU

CMOS Multiplier

8 x 8 Bit, 45ns, 65ns

The TMC208K and TMC28KU are high-speed 8 x 8 bit parallel multipliers which operate at a 45 or 65ns cycle time (22.2 or 15.3MHz multiplication rate). The multiplicand and multiplier are both two's complement numbers in the TMC208K and unsigned magnitude numbers in the TMC28KU, yielding a full precision 16-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are constructed using positive-edge-triggered D-type flip-flops. Built with TRW's OMICRON-C™ CMOS process, the TMC208K and TMC28KU are pin and function compatible with the MPY008H and MPY08HU yet operate with greater speeds at much less power dissipation.

Features

- 45 or 65ns Multiply Time
- 8 x 8 Bit Parallel Multiplication With 16-Bit Product Output
- Three-State Outputs
- Single +5V Power Supply
- TTL Compatible
- Available In A 40 Pin CERDIP Or Plastic DIP

TMC208K

- Pin Compatible With MPY008H
- Two's Complement Multiplication

TMC28KU

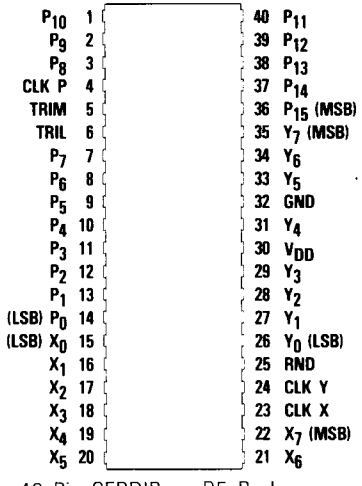
- Pin Compatible With MPY08HU
- Unsigned Magnitude Multiplication

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

I

Pin Assignments



40 Pin CERDIP – B5 Package
40 Pin Plastic DIP – N5 Package

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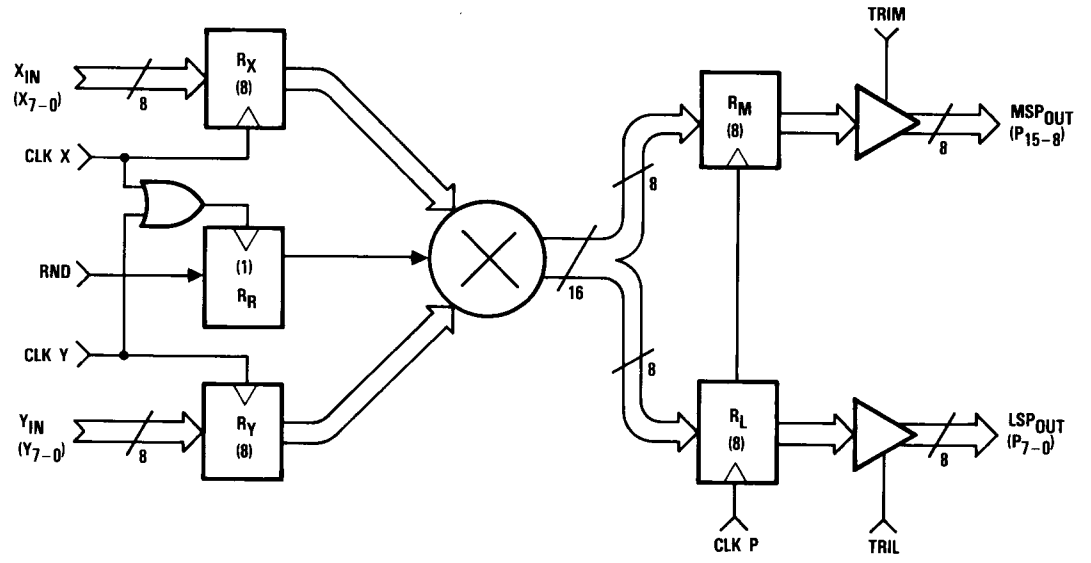
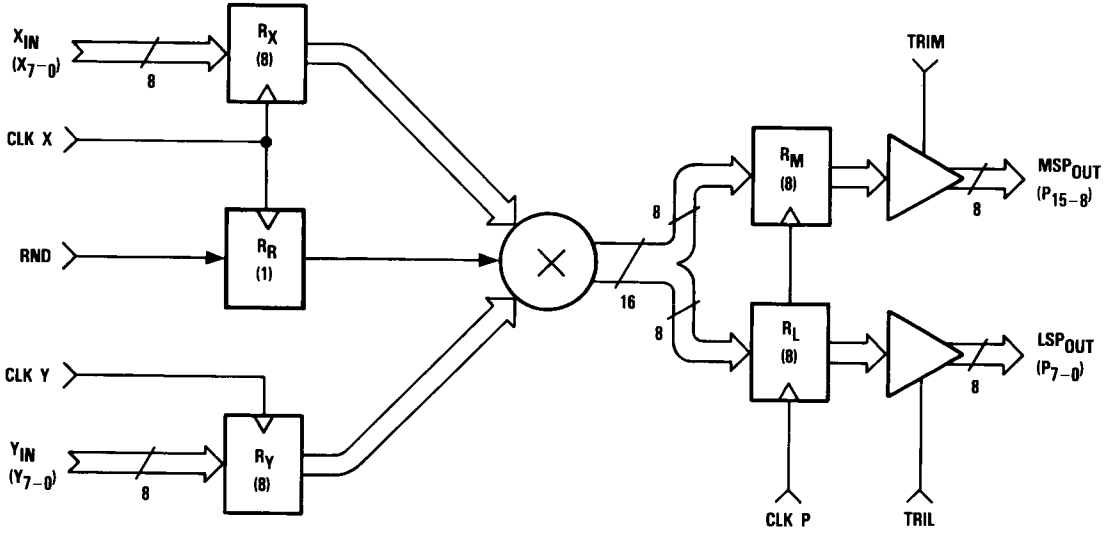
TMC208K Functional Block Diagram



TMC28KU Functional Block Diagram



Functional Description

General Information

The TMC208K and TMC28KU have three functional sections: input registers, an asynchronous multiplier array and output registers. The input registers store the two 8-bit numbers which are to be multiplied and the instruction which controls output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders designed to handle two's complement numbers in the TMC208K or unsigned magnitude numbers in the TMC28KU. The output registers hold the product as two 8-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the multipliers to be used on a bus, or allow the MSP and LSP to be multiplexed over the same 8-bit output lines.

Signal Definitions

Power

V_{DD}, GND — The TMC208K and TMC28KU operate from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

X_{7-0},Y_{7-0} — The TMC208K has two 8-bit two's complement data inputs labeled X and Y. The TMC28KU has two 8-bit unsigned magnitude data inputs labeled X and Y. The Most Significant Bits (MSBs), X_7 and Y_7, carry the sign information for the two's complement notation in the TMC208K. The remaining bits are X_{6-0} and Y_{6-0} with X_0 and Y_0 the LSBs. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown in Figures 1 through 4.

Data Outputs

P_{15-0} — The TMC208K has a 16-bit two's complement output which is the product of the two input X and Y values. The TMC28KU has a 16-bit unsigned magnitude output which is the product of the two input X and Y values. This output is divided into two 8-bit output words, the MSP and LSP. The MSB of both the MSP and the LSP is the sign bit in the TMC208K. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown in Figures 1 through 4. Note that since +1 cannot be exactly represented in fractional two's complement notation, some provision for handling the case (−1) x (−1) must be made. The TMC208K outputs a −1 in this case. As a result, external error handling provisions may be required.

Clocks

CLK X, CLK Y, CLK P — The TMC208K and TMC28KU have three clock lines, one for each input register (CLK X and CLK Y) and one for the product register (CLK P). Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. In the TMC208K, the RND input is registered and clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks. In the TMC28KU, the RND input is registered and clocked in on the rising edge of CLK X.

Controls

TRIM, TRIL — TRIM and TRIL are the three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when LOW. TRIM and TRIL are not registered.

RND — When RND (Round) is HIGH, a one is added to the MSB of the LSP. A one will be added to the P_6 bit in the 208K or to the P_7 bit in the 28KU. Note that rounding always occurs in the positive direction. In some applications this may introduce a systematic bias. The RND input is registered and used when a rounded 8-bit product is desired.

Package Interconnections

Signal Type	Signal Name	Function	B5, N5 Package
Power	V_{DD}	Supply Voltage	30
	GND	Ground	32
Data Inputs	X_{7-0}	X Input Word	22-15
	Y_{7-0}	Y Input Word	35-33, 31, 29-26
Data Outputs	P_{15-8}	MSP Output	36-40, 1-3
	P_{7-0}	LSP Output	7-14
Clocks	CLK X	X Register Clock	23
	CLK Y	Y Register Clock	24
	CLK P	Product Register Clock	4
Controls	TRIM	MSP Three-State	5
	TRIL	LSP Three-State	6
	RND	Round	25

Figure 1. Fractional Two's Complement Notation (TMC208K)

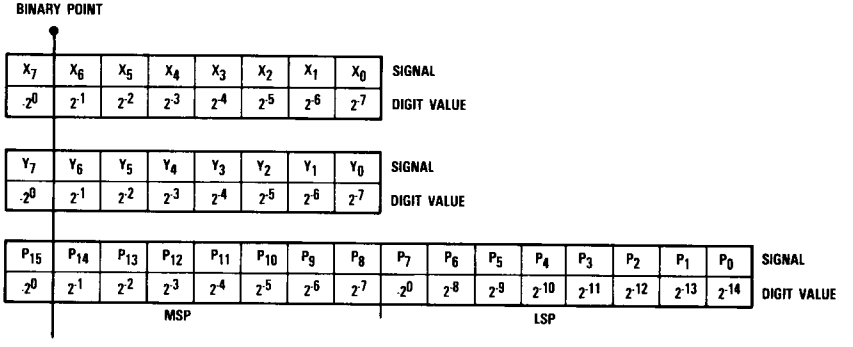


Figure 2. Integer Two's Complement Notation (TMC208K)

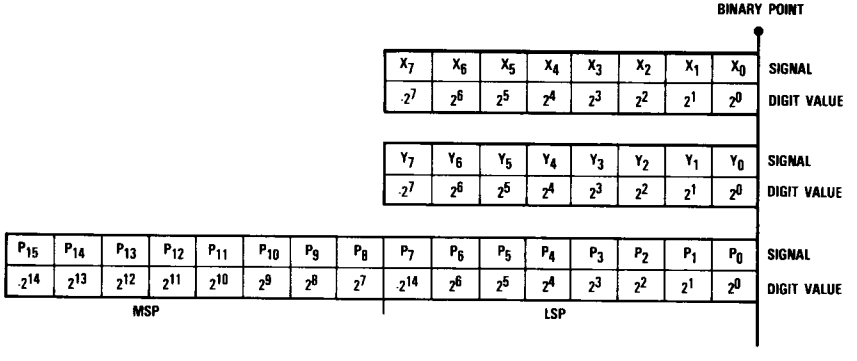


Figure 3. Fractional Unsigned Magnitude Notation (TMC28KU)

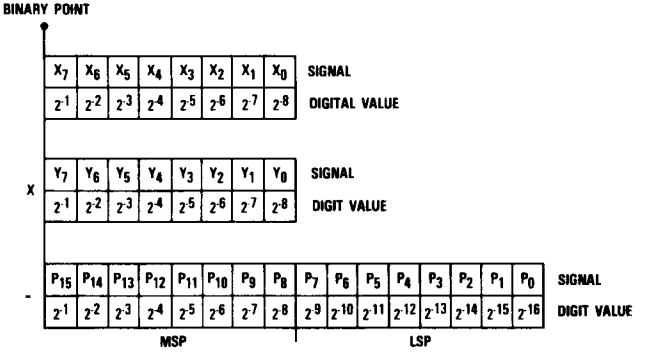


Figure 4. Integer Unsigned Magnitude Notation (TMC28KU)

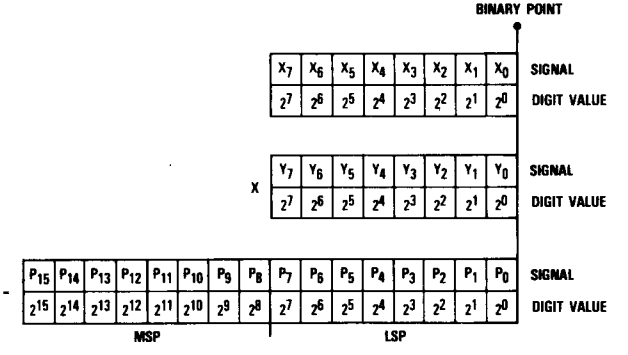


Figure 5. Timing Diagram

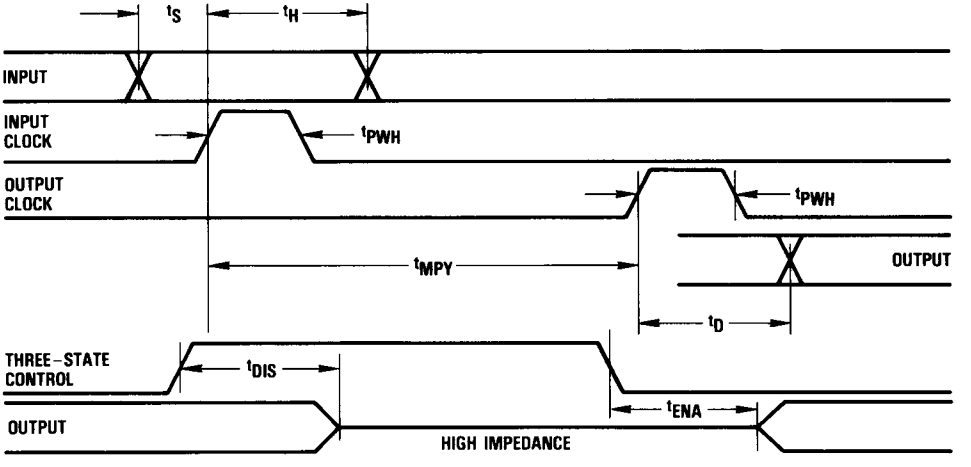


Figure 6. Equivalent Input Circuit

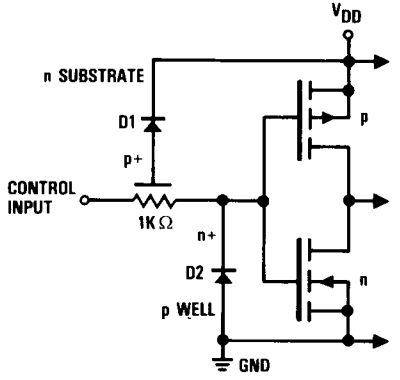


Figure 7. Equivalent Output Circuit

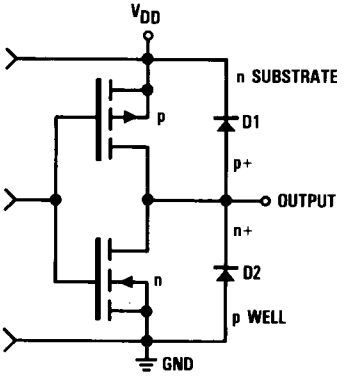
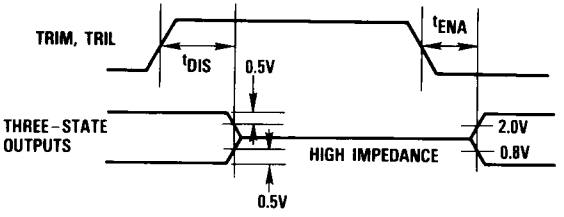


Figure 8. Threshold Levels For Three-State Measurements



Application Discussion

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, the TMC208K and TMC28KU do not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer or fractional notation. If integer notation is used, the LSBs of the multiplier, multiplicand and product all have the same value. If fractional notation is used, the MSBs of the multiplier, multiplicand and product all have the same value.

DC characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, TRIM, TRIL = 5V, f = 10MHz		50		50	mA
		V_{DD} = Max, TRIM, TRIL = 5V, f = 22MHz		100		100	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MPY}	Multiply Time	V_{DD} = Min					
		TMC208K, TMC28KU		65		70	ns
		TMC208K-1, TMC28KU-1		45		50	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15		15		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		ns
t_S	Input Setup Time	TMC208K, TMC28KU	25		30		ns
		TMC208K-1, TMC28KU-1	20		25		ns
t_H	Input Hold Time		0		0		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		25		30	ns
t_{ENA}	Three-State Output Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		20		25	ns
t_{DIS}	Three-State Output Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		20		25	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage[2]	−0.5 to (V_{DD} + 0.5)V
Forced current[3,4]	−1.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC208KB5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	208KB5C
TMC208KB5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	208KB5C1
TMC208KB5V	EXT – T_C = –55°C to 125°C	MIL-STD-883	40 Pin CERDIP	208KB5V
TMC208KB5V1	EXT – T_C = –55°C to 125°C	MIL-STD-883	40 Pin CERDIP	208KB5V1
TMC208KN5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	208KN5C
TMC208KN5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	208KN5C1
TMC28KUB5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	28KUB5C
TMC28KUB5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	28KUB5C1
TMC28KUB5V	EXT – T_C = –55°C to 125°C	MIL-STD-833	40 Pin CERDIP	28KUB5V
TMC28KUB5V1	EXT – T_C = –55°C to 125°C	MIL-STD-883	40 Pin CERDIP	28KUB5V1
TMC28KUN5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	28KUN5C
TMC28KUN5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	28KUN5C1