TDC1005

Serial Shift Register

Dual 64-Bit

The TRW TDC1005 is a dual 64-bit positive-edge-triggered serial shift register which operates at 25MHz. This device is cascadable in the number of words and the word size.

Complementary TTL outputs Q and $\overline{Q}$ are provided. The two data inputs in each shift register, D0 and D1, are controlled by a data select input, DS. This provides on-chip recirculate gating when the true output is hard-wired to one of the inputs.

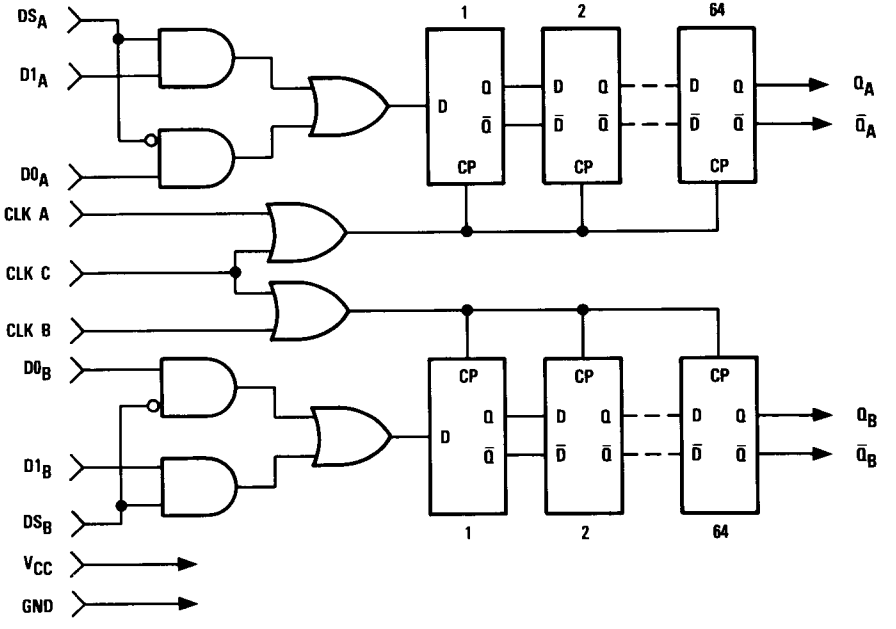
Features

- 25MHz Guaranteed Clock Frequency
- Fully TTL Compatible
- True and Complementary Outputs
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 16 Pin CERDIP
- Horizontal And Vertical Cascadability

Applications

- High-Speed Data Acquisition
- First-In First-Out Data Buffers
- Coefficient Storage For FIR Filters
- Digital Delay Lines
- Local Storage Registers

Functional Block Diagram



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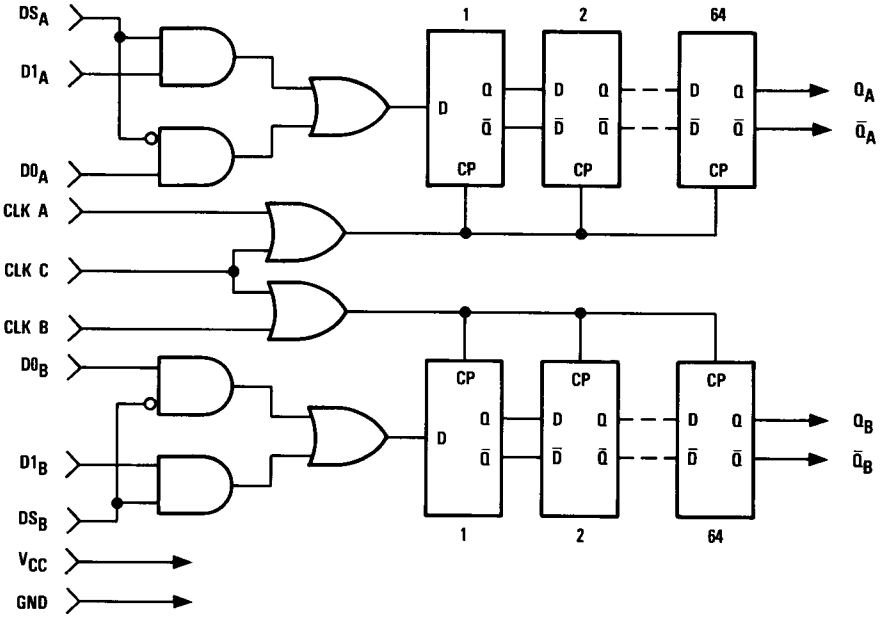
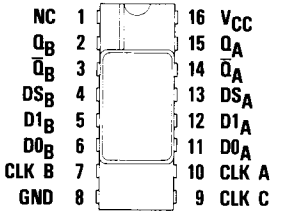
Functional Block Diagram



Pin Assignments



16 Pin CERDIP – B9 Package

Functional Description

General Information

The TDC1005 is a positive-edge-triggered dual 64-bit serial shift register. One of two data inputs (D0 and D1) is selected by the Data Select control (DS). Complementary outputs Q and $\overline{Q}$ are available.

Power

The TDC1005 operates from a single +5 Volt power supply.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 16
GND	Ground	0.0V	Pin 8

Data Inputs

The TDC1005 has two data inputs per block, ($D0_A$ and $D0_B$, $D1_A$ and $D1_B$).

Name	Function	Value	J9 Package
$D0_A$	Data Input 0, Block A	TTL	Pin 11
$D1_A$	Data Input 1, Block A	TTL	Pin 12
$D0_B$	Data Input 0, Block B	TTL	Pin 6
$D1_B$	Data Input 1, Block B	TTL	Pin 5

Data Select

Two data select controls, one for Block A (DS_A) and one for Block B (DS_B), are provided to select between inputs 0 and 1. The 0 input is selected when DS is LOW; the 1 input is selected when DS is HIGH.

Name	Function	Value	J9 Package
DS_A	Block A Data Select	TTL	Pin 13
DS_B	Block B Data Select	TTL	Pin 4

K

Data Outputs

Complementary outputs Q and $\overline{Q}$ are provided for the TDC1005.

Name	Function	Value	J9 Package
QA	Data Output Block A	TTL	Pin 15
$\overline{QA}$	Data Output (Inv.) Block A	TTL	Pin 14
QB	Data Output Block B	TTL	Pin 2
$\overline{QB}$	Data Output (Inv.) Block B	TTL	Pin 3

Clocks

The TDC1005 has three clock inputs (CLK A, CLK B, CLK C) which are combined to provide the clock signals for the two blocks. Block A is clocked by the logical OR of CLK A and CLK C. Block B is clocked by the logical OR of CLK B and CLK C. This allows the two blocks to be clocked either independently or simultaneously.

Name	Function	Value	J9 Package
CLK A	Clock A	TTL	Pin 10
CLK B	Clock B	TTL	Pin 7
CLK C	Clock C	TTL	Pin 9

No Connects

Pin 1 on the TDC1005 is not connected internally. This pin may be left unconnected.

Name	Function	Value	J9 Package
NC	No connection	Open	Pin 1

Figure 1. Timing Diagram

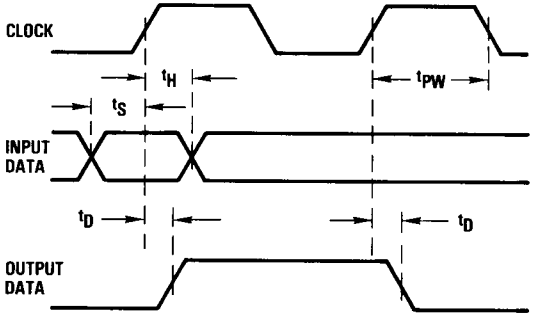


Figure 2. Input/Output Schematics

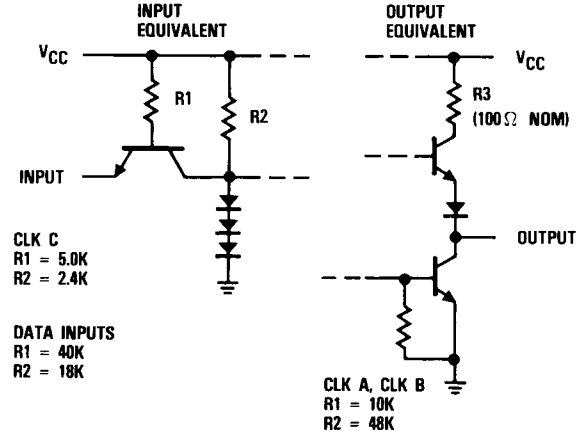
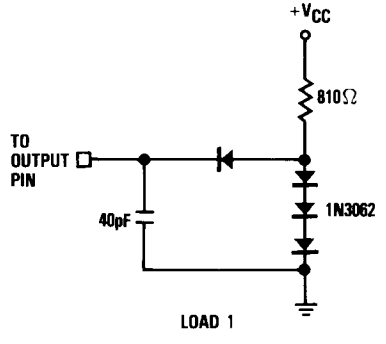


Figure 3. Test Load for Delay Measurement (Typical)



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	0 to +5.5V
Output	
Applied voltage (measured to GND)	0 to +5.5V [2]
Applied current, externally forced	−1.0 to 6.0ma [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	18			18			ns
t_S	Input Register Setup Time	7			7			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max		105		120	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{IL}	Input Current, Logic LOW [1]	V_{CC} = Max, V_{IL} = 0.4V		−0.5		−0.8	mA/Load
I_{IH}	Input Current, Logic HIGH [1]	V_{CC} = Max, V_{IH} = 2.4V		20		50	μA/Load

Note: 1. CLK C: Eight equivalent loads
CLK A, CLK B: Four equivalent loads

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Clock Frequency	See Figure 3	25		24		MHz
t_D	Output Delay	See Figure 3		35		35	ns

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1005B9C	STD − T_A = 0°C to 70°C	Commercial	16 Pin CERDIP	1005B9C
TDC1005B9A	EXT − T_C = −55°C to 125°C	High Reliability	16 Pin CERDIP	1005B9A