TDC1034

Digital-to-Analog Converter
4-Bit, 200MHz

The TRW TDC1034 is a 4-bit D/A converter, designed for 200MHz operation and is capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Three special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1034 is built with TRW's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays insure low glitch energy. The TDC1034 offers high performance, low power consumption, and video compatibility in an 18 pin CERDIP package.

Features

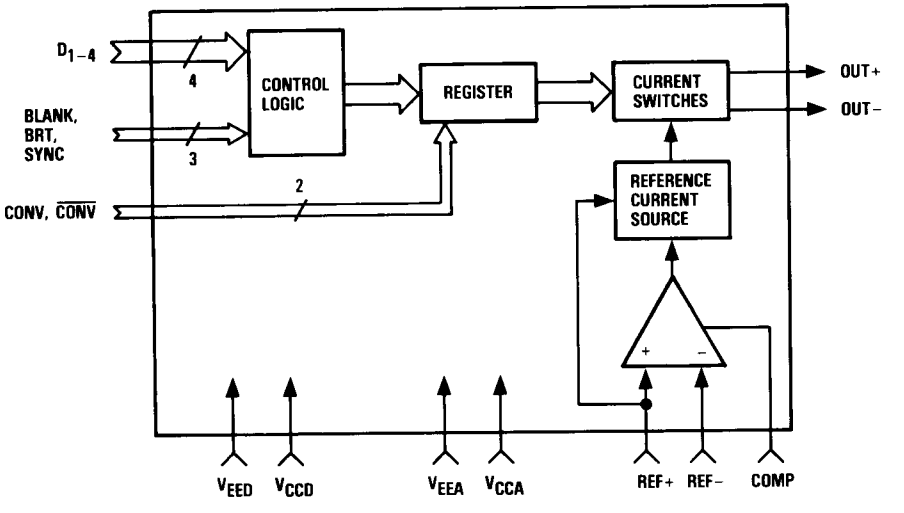
- "Graphics-Ready"
- 200MHz Conversion Rate
- 1/8 LSB Linearity
- Power Supply Noise Rejection >50dB
- Registered Data And Video Controls
- Differential Current Outputs
- Video Controls: SYNC, BLANK, BRIghT
- Low Glitch Energy
- ECL Compatible, Can Be Used In TTL Systems
- Low Power Dissipation
- Available In An 18 Pin CERDIP Package
- Single −5.2V Power Supply

B

Applications

- CAD/CAM Workstations
- RGB Graphics
- Raster Scan Displays
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

Functional Block Diagram



TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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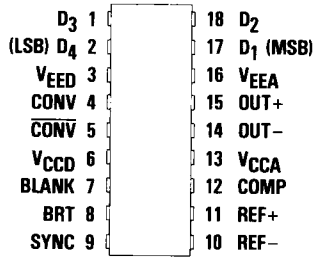
Pin Assignments



18 Pin CERDIP – B8 Package

Functional Description

General Information

The TDC1034 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. Each rising edge of the CONVert clock (CONV) latches data and control values into an internal D-type register. The registered values are then converted into an analog output by switched current sinks.

The TDC1034 uses a segmented circuit design scheme in which the input data is decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen output levels.

Special control inputs, SYNC, BLANK and BRighT (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1034 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is $-5.2V$, these may ultimately be connected to the same power source, but high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in *Figure 7*. The return for I_{EED}, the current drawn from the V_{EED} supply, is V_{CCD}. The return for I_{EEA} is V_{CCA}. All V_{EE} and V_{CC} pins MUST be connected.

Although the TDC1034 is specified for a nominal supply of $-5.2V$, operation from a $+5.0V$ supply is possible provided that the relative polarities of all voltages are correctly maintained. For additional information concerning the use of ECL D/A converters in a $+5V$ system, refer to *TRW Application Note TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment."*

Reference

The TDC1034 has two reference inputs: REF+ and REF–, which are noninverting and inverting inputs to an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see *Figure 4*).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full-scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in *Figure 7*.

The reference current flows into the REF+ input, while REF– is typically connected to a negative reference voltage through a resistor chosen to minimize input offset current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1034's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen when dynamic modulation of the reference is required.

Controls

The TDC1034 has three special video control inputs: SYNC, BLANK and BRighT (BRT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

Controls (cont.)

The video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. These inputs, like data, must be valid for a setup time of t_S before, and a hold time of t_H after the rising edge of CONV in order to be registered.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in *Table 1*. Internal logic governs the interaction of these controls to simplify their use in video applications. BLANK and SYNC override the data inputs. SYNC overrides all other inputs, and produces full-scale output. The BRT control creates a "whiter than white" level by adding 10% of the full-scale value to the present output level, and is especially useful in graphics display for highlighting cursors, warning messages, or menus. For non-video applications, these controls may be left unconnected.

Data Inputs

Data inputs to the TDC1034 are standard single-ended ECL compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

Valid data must be present at the input a setup time t_S before, and a hold time t_H after the rising edge of CONV.

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1034. Within the constraints shown in *Figure 2*, the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$. CONV may be driven single-ended by connecting $\overline{\text{CONV}}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected.

Analog Outputs

The two analog outputs of the TDC1034 are high impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving dual 75 Ohm loads to standard video levels. The output voltage is the product of the output current and effective load impedance, and is usually between 0V and −1.07V in the standard configuration (see *Figure 5*). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

B

Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	16
	V_{EED}	Digital Supply Voltage	−5.2V	3
	V_{CCA}	Analog Supply Voltage	0.0V	13
	V_{CCD}	Digital Supply Voltage	0.0V	6
Reference	REF−	Reference Current− Input	Op-Amp Virtual Ground	10
	REF+	Reference Current+ Input	Op-Amp Virtual Ground	11
	COMP	COMPensation Input	C_C	12
Controls	BLANK	Video BLANK Input	ECL	7
	BRT	Video BRighT Input	ECL	8
	SYNC	Video SYNC Input	ECL	9
Data Inputs	D_1	Data Bit 1 (MSB)	ECL	17
	D_2		ECL	18
	D_3		ECL	1
	D_4	Data Bit 4 (LSB)	ECL	2
Convert	CONV	CONVert Clock Input	ECL	4
	$\overline{CONV}$	CONVert Clock Input, Complement	ECL	5
Analog Outputs	OUT−	Output Current−	See Text	14
	OUT+	Output Current+	See Text	15

Figure 1. Timing Diagram

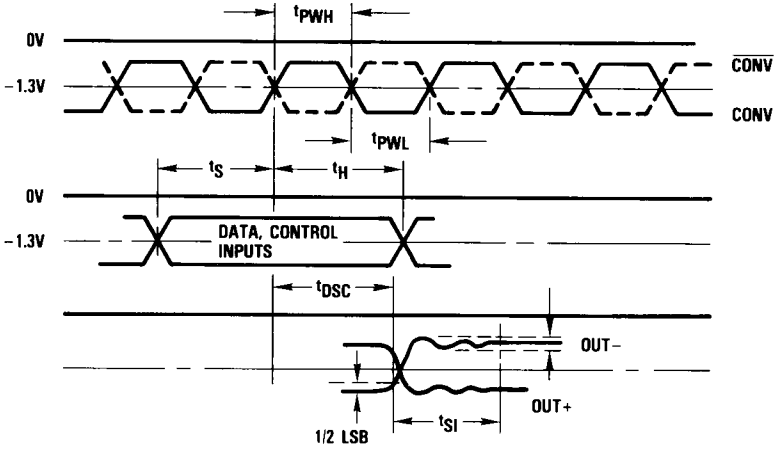


Figure 2. CONV, $\overline{CONV}$ Switching Levels

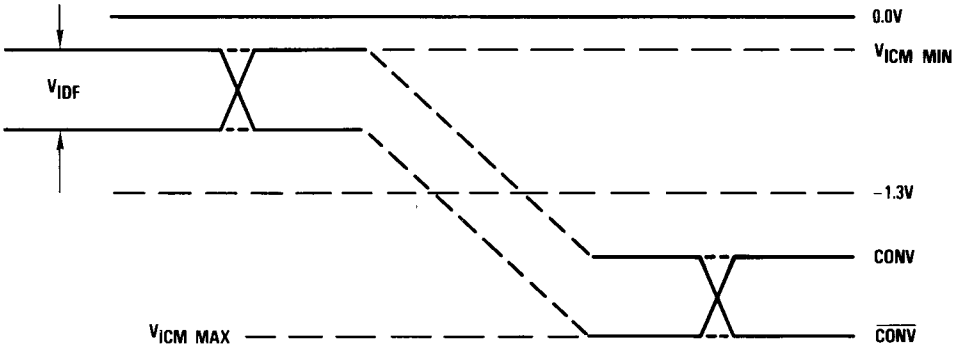


Figure 3. Equivalent Input Circuit

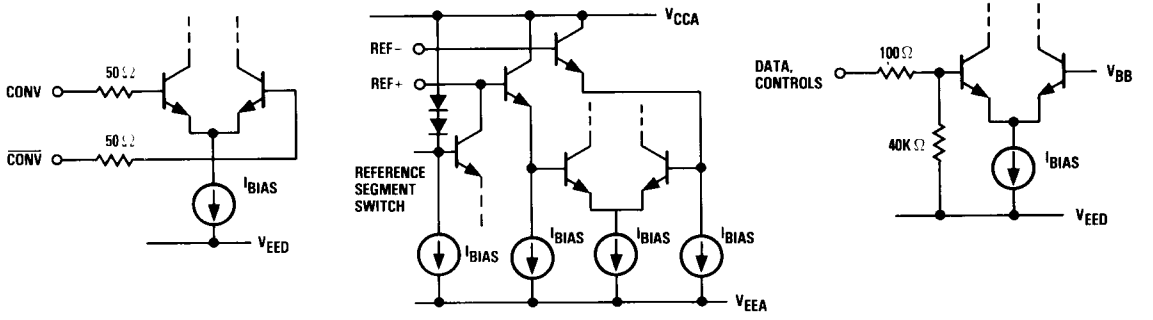


Figure 4. Equivalent Output Circuit

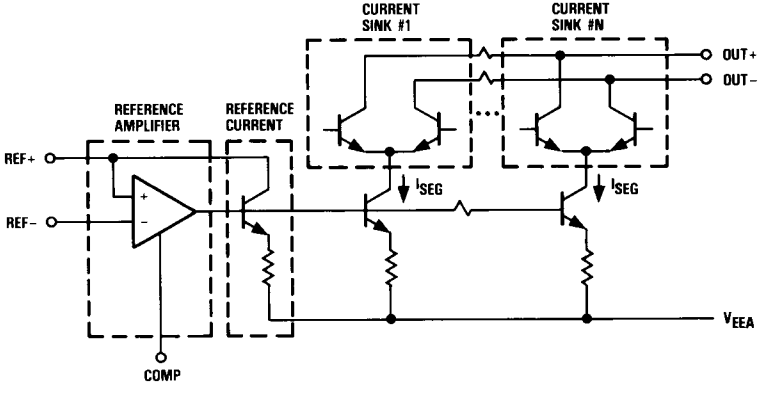
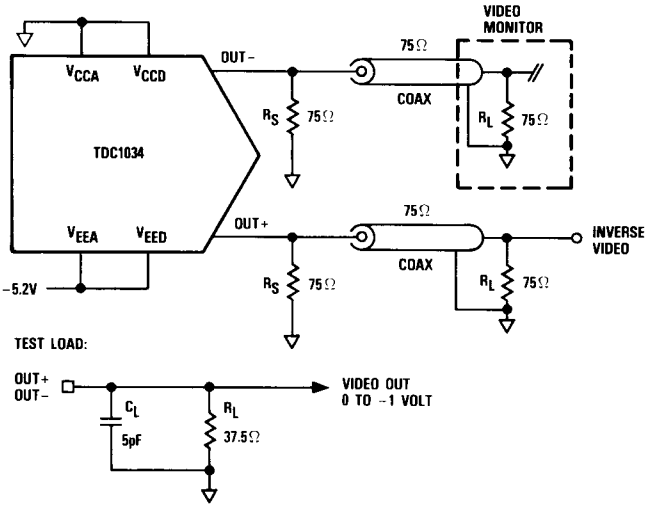


Figure 5. Standard Load Configuration



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to V_{CCD})	-7.0 to 0.5V
V_{EEA} (measured to V_{CCA})	-7.0 to 0.5V
V_{EEA} (measured to V_{EED})	-0.5 to 0.5V
V_{CCA} (measured to V_{CCD})	-0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to V_{CCD})	V_{EED} to 0.5V
Reference input, applied voltage (measured to V_{CCA})[2]	
REF+	V_{EEA} to 0.5V
REF-	V_{EEA} to 0.5V
Reference input, applied current, externally forced[3,4]	
REF+	6.0mA
REF-	0.5mA

Output

Analog output, applied voltage (measured to V_{CCA})	
OUT+	-2.0 to +2.0V
OUT-	-2.0 to +2.0V
Analog output, applied current, externally forced[3,4]	
OUT+	50mA
OUT-	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	-60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	-60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to V_{CCD})	-4.75	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{CCA})	-4.75	-5.2	-5.5	V
$V_{CCA}-V_{CCD}$	Supply Voltage Differential	-0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	-0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)	-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)	0.3		1.2	V
t_{PWL}	CONV Pulse Width, LOW	4			ns
t_{PWH}	CONV Pulse Width, HIGH	4			ns
t_S	Setup Time, Data and Controls	4.0			ns
t_H	Hold Time, Data and Controls	0			ns
V_{IL}	Input Voltage, Logic LOW			-1.49	V
V_{IH}	Input Voltage, Logic HIGH	-1.045			V
I_{REF}	Reference Current Video standard output levels[1]	1.10	1.17	1.24	mA
	6-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor	1000	2700		pF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after intitial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	V_{EEA} = V_{EED} = Max, static[1]			
		T_A = 0°C to 70°C		-145	mA
		T_A = 70°C		-130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF-			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output		-1.2	+1.5	V
V_{OCN}	Compliance Voltage, - Output		-1.2	+1.5	V
R_O	Equivalent Output Resistance		50		K
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = Nom, SYNC = BLANK = 0, BRT = 1	30		mA
I_{ON}	Max Current, - Output	V_{EEA} = Nom, SYNC = 1	30		mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = Max, V_I = -1.49V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = Max, V_I = -1.045V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = Max, $-2.5 < V_I < -0.5$		50	μA

Note:
1. Worst case over all data and control states.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = Min	200		MSPS
t_{DSC}	Clock to Output Delay	V_{EEA}, V_{EED} = Min		8	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = Min, 3.2%		5	ns
t_{RI}	Rise Time, Current	10% to 90% of Gray Scale		2.0	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = Nom		0.8	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Nom		0.8	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = Max, SYNC = BLANK = 0, BRT = 1		10	μA
EG	Absolute Gain Error	V_{EEA}, V_{EED} = Min		6	% of Gray Scale
TC_G	Gain Error Tempco	I_{REF} = Nom		0.01	% of Gray Scale/°C
BWR	Reference Bandwidth, -3dB	C_C = Min, V_{REF} = 1mV p-p	1		MHz
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = Nom[1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = Nom[2]		46	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Nom		120	μA/V
G_C	Peak Glitch Charge[3,4]			800	fCoulomb
G_I	Peak Glitch Current			1.2	mA
G_E	Peak Glitch "Energy" (Area)[4]			30	pV-Sec
FT_C	Feedthrough Clock[5]	Data = Constant BW = 250MHz		-36	dB
		BW = 50MHz		-50	dB
FT_D	Feedthrough Data[5]	CONV = Constant BW = 250MHz		-42	dB
		BW = 50MHz		-50	dB

Notes:

1. 20KHz, 0.75V p-p ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, 0.75V p-p ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps x nanoseconds.
4. 37.5 Ω load. Because glitches tend to be symmetric, average glitch energy approaches zero.
5. dB relative to full gray scale.

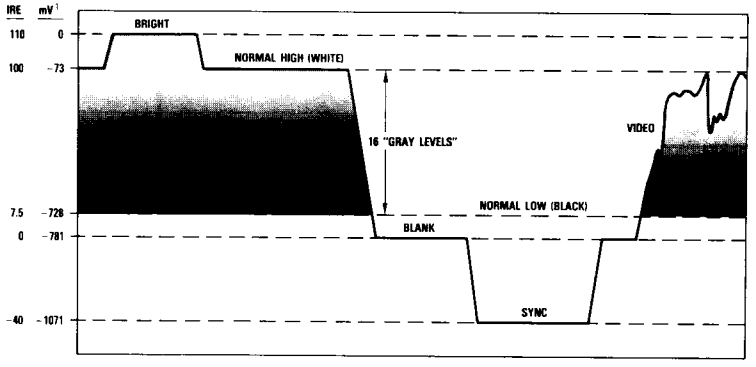
Table 1 Video Control Truth Table

Sync	Blank	Bright	Data Input	Out− (mA)[1]	Out− (V)[2]	Out− (IRE)[3]	Description[4]
1	X	X	X	28.57	−1.071	−40	Sync Level
0	1	X	X	20.83	−0.781	0	Blank Level
0	0	0	0000	19.40	−0.728	7.5	Normal Low Level
0	0	0	1111	1.95	−0.073	100	Normal High Level
0	0	1	0000	17.44	−0.654	7.5	Enhanced Low Level
0	0	1	1111	0.00	0.00	110	Enhanced High Level

Notes:

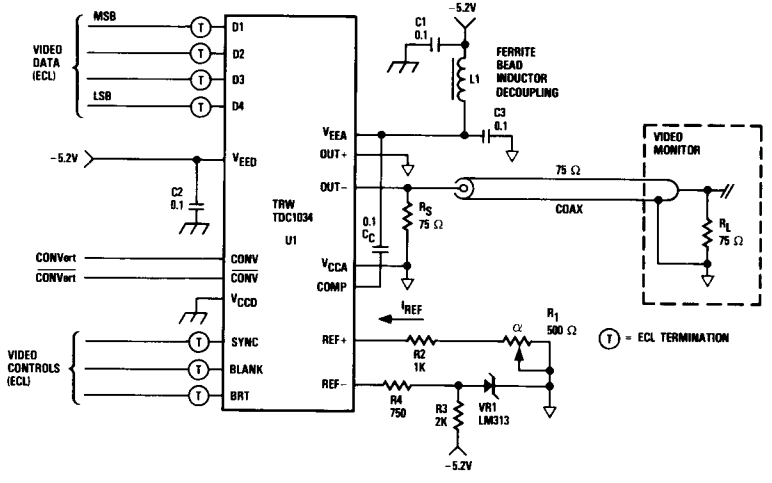
1. Out+ is complementary to Out−. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms to V_{CCA}). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS−343−A tolerance on all control values is assumed.

Figure 6. Video Output Waveform for Out− and Standard Load Configuration



Note: 1. Output voltage is measured with standard load connected between Out− and V_{CCA}.

Figure 7. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1034B8C	STD–T_A=0°C to 70°C	Commercial	18 Pin CERDIP	1034B8C

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