Digital FIR Filter

Building Block, 10MHz

The TDC1028 is a video-speed, TTL compatible bit-slice building block for Finite Impulse Response (FIR) digital filters and multi-bit digital correlators. It is used independently in the coefficient and signal data word dimensions as a bit-slice processor. Word lengths can be multiples of four bits. Two's complement or unsigned magnitude operation is independently selectable for both coefficients and signal data words.

The TDC1028 provides eight delay stages, eight multipliers, and eight adders in a single integrated circuit. Eight coefficient storage registers are also provided for ease in programming filter characteristics and to make correlation possible. One coefficient may be changed every clock cycle. The delay registers and the adder pipeline registers have been merged for efficiency.

Features

- 10MHz Throughput Rate
- Eight Coefficients
- Cascadable (To > 36 Taps) Without External Components
- 4-Bit Coefficient And Signal Data Words
- Independently Expandable Coefficient And Signal Word Length
- Independently Selectable Format For Coefficients And Signal Data Words (Two's Complement Or Unsigned Magnitude)
- Available In A 48 Pin Hermetic Ceramic DIP Package
- Radiation Hard Bipolar Process
- Single +5V Power Supply
- TTL Compatible

Applications

- Digital Video Filters
- Matched Filters
- Pulse Compression
- Multi-Bit Correlation
- Waveform Synthesis
- Adaptive Filters

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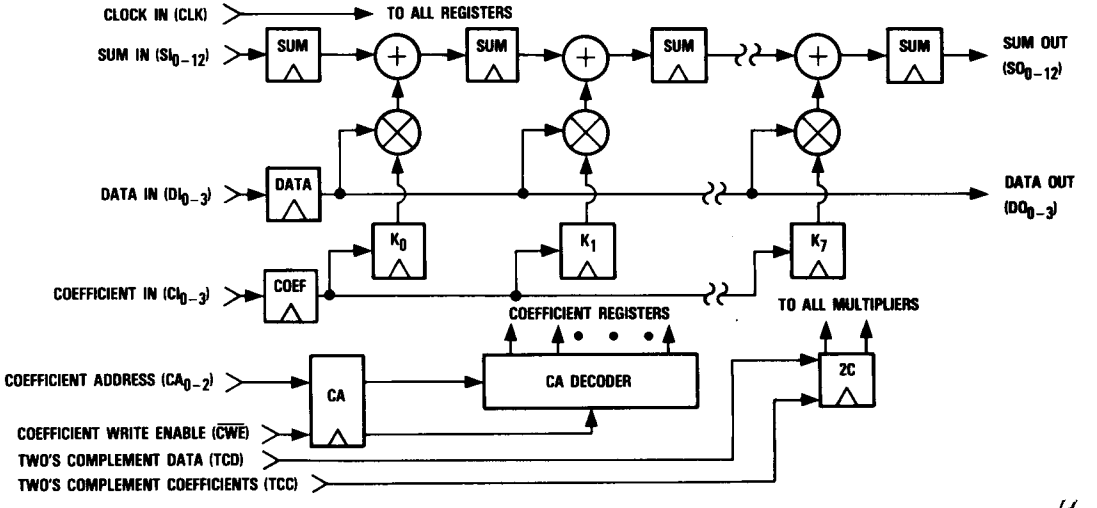
Functional Block Diagram



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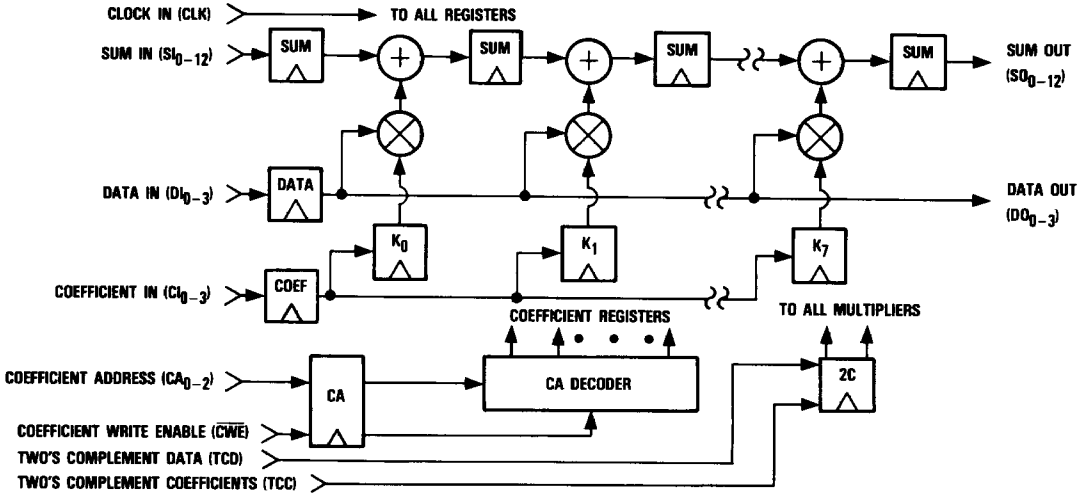
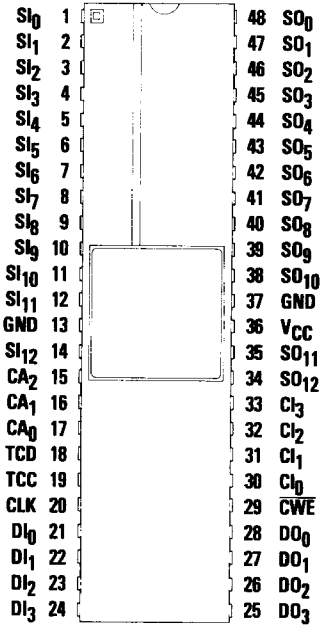
40G00817 Rev. E–11/90
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments



48 Lead DIP - J4 Package

Functional Description

General Information

The TDC1028 has four internal functions: delay, multiplication, addition, and coefficient storage. These functions are connected to form a building block for finite impulse response filters or correlators. Cascading inputs are provided to allow the construction of filters or correlators of arbitrary length. The basic word size for coefficients and data is four bits. The order of the operations has been changed from the canonical form to permit the merging of delay and pipelining registers (see Figure 1).

Power

The TDC1028 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J4 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 36
GND	Ground	0.0V	Pins 13,37

Inputs

The TDC1028 has three types of inputs: signal data, coefficients, and sum (cascading) inputs.

Name	Function	Value	J4 Package
DI_3	Signal Data Input MSB	TTL	Pin 24
DI_2		TTL	Pin 23
DI_1		TTL	Pin 22
DI_0	Signal Data Input LSB	TTL	Pin 21
CI_3	Coefficient Input MSB	TTL	Pin 33
CI_2		TTL	Pin 32
CI_1		TTL	Pin 31
CI_0	Coefficient Input LSB	TTL	Pin 30
SI_{12}	Cascading Sum Input MSB	TTL	Pin 14
SI_{11}		TTL	Pin 12
SI_{10}		TTL	Pin 11
SI_9		TTL	Pin 10
SI_8		TTL	Pin 9
SI_7		TTL	Pin 8
SI_6		TTL	Pin 7
SI_5		TTL	Pin 6
SI_4		TTL	Pin 5
SI_3		TTL	Pin 4
SI_2		TTL	Pin 3
SI_1		TTL	Pin 2
SI_0	Cascading Sum Input LSB	TTL	Pin 1

Data Outputs

The TDC1028 has two outputs: a sum output and a data output. The data output is used to connect one TDC1028 to the next (cascading) for greater filter or correlation length. The sum output is used both for cascading and signal output.

Name	Function	Value	J4 Package
SO_{12}	Sum Output MSB	TTL	Pin 34
SO_{11}		TTL	Pin 35
SO_{10}		TTL	Pin 38
SO_9		TTL	Pin 39
SO_8		TTL	Pin 40
SO_7		TTL	Pin 41
SO_6		TTL	Pin 42
SO_5		TTL	Pin 43
SO_4		TTL	Pin 44
SO_3		TTL	Pin 45
SO_2		TTL	Pin 46
SO_1		TTL	Pin 47
SO_0	Sum Output LSB	TTL	Pin 48
DO_3	Data Output MSB	TTL	Pin 25
DO_2		TTL	Pin 26
DO_1		TTL	Pin 27
DO_0	Data Output LSB	TTL	Pin 28

Clocks

The TDC1028 operates synchronously from a single master clock, which can be clocked at up to 10MHz. All internal circuitry is static; there is no minimum clock frequency required. The rising edge of CLK latches the Coefficient Input (CI_{3-0}), the Coefficient Address (CA_{2-0}), and the Coefficient Write Enable control ($\overline{CWE}$). If $\overline{CWE}$ is LOW, a new coefficient will be loaded into the selected coefficient register at the next rising edge of CLK, as shown in Figure 4.

Name	Function	Value	J4 Package
CLK	Clock	TTL	Pin 20

Controls

The TDC1028 has six control inputs. TCC and TCD control the interpretation of the data and coefficients as two's complement or unsigned magnitude numbers. These inputs provide two's complement operation for the respective input when a logic HIGH is applied, and unsigned magnitude operation when a logic LOW is applied. One active LOW input ($\overline{CWE}$) controls the writing of a coefficient, and three inputs (CA_{2-0}) control the selection of which coefficient is to be written.

Name	Function	Value	J4 Package
TCC	Two's Complement Coefficients	TTL	Pin 19
TCD	Two's Complement Data	TTL	Pin 18
$\overline{CWE}$	Coefficient Write Enable	TTL	Pin 29
CA_2	Coefficient Address MSB	TTL	Pin 15
CA_1		TTL	Pin 16
CA_0	Coefficient Address LSB	TTL	Pin 17

Figure 1.

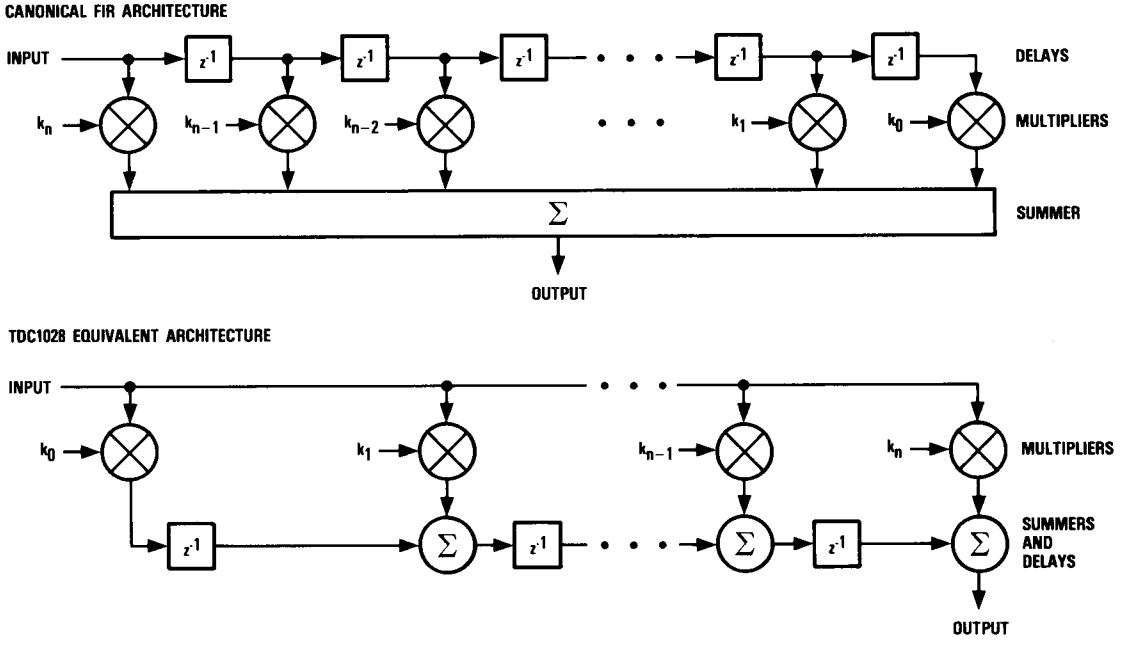


Figure 2.

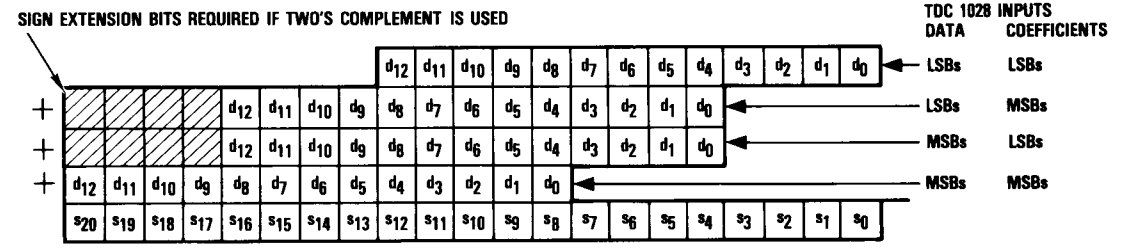


Figure 3.

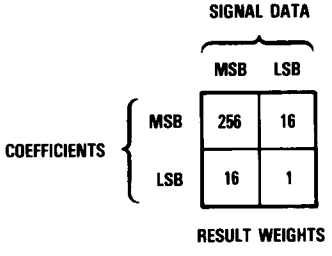


Figure 4.

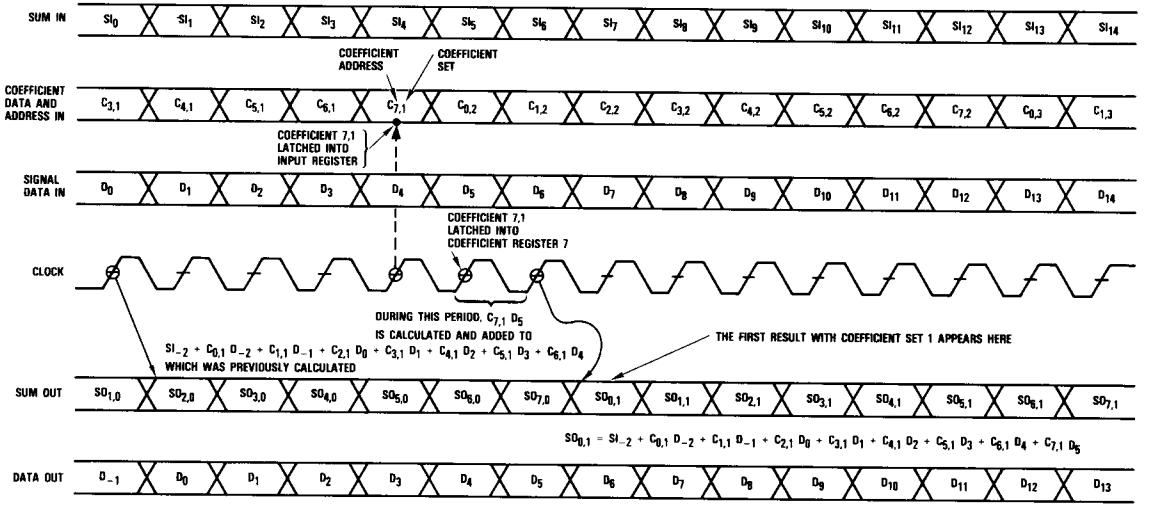


Figure 5.

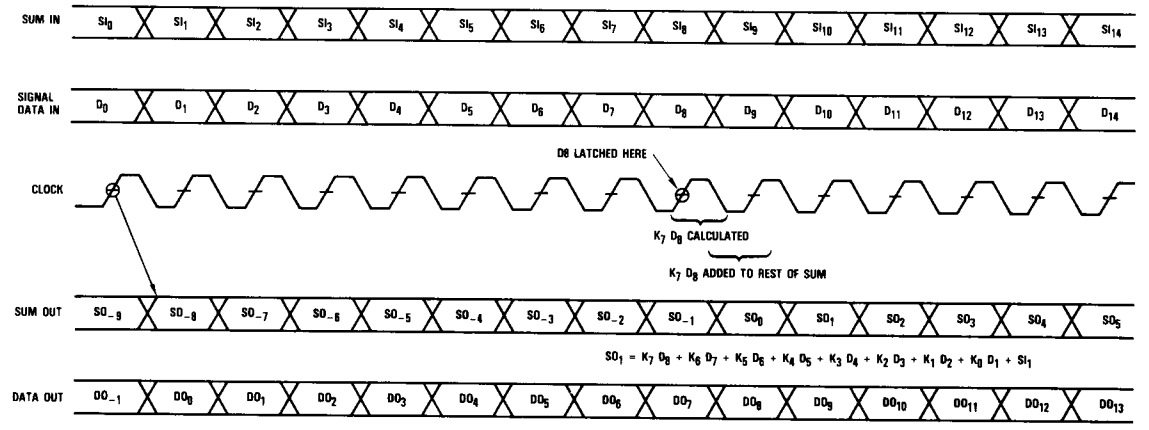


Figure 6. Equivalent Input Circuit

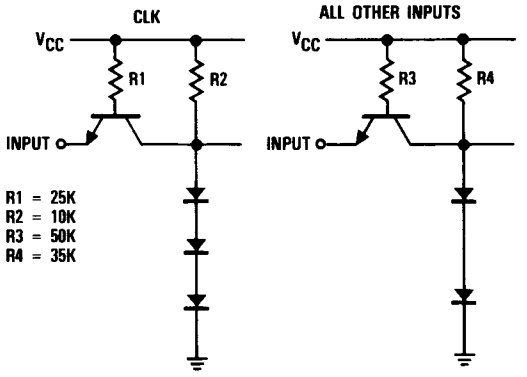


Figure 7. Equivalent Output Circuit

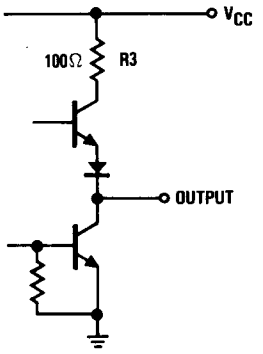
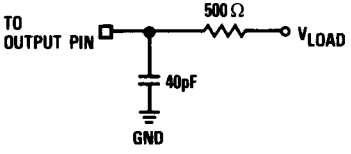


Figure 8. Test Load



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	41			65			ns
t_{PWH}	Clock Pulse Width, HIGH	55			65			ns
t_{CY}	Clock Cycle Time	100			135			ns
t_S	Input Setup Time							
	Data In, Sum In	15			15			ns
	Coefficient In, Coefficient Address In	25			25			ns
	Coefficient Write Enable	30			30			ns
t_H	Input Hold Time (All inputs)	5			5			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max, Static					
		T_A = 0°C to 70°C		700			mA
		T_A = 70°C		550			mA
		T_C = −55°C to 125°C				900	mA
		T_C = 125°C				500	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V					
		Data Inputs		−0.4		−0.4	mA
		Clock Input		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V					
		Data Inputs		75		75	μA
		Clock Input		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

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Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{CC} = Min		100		135	ns
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		30		35	ns

Note:

1. All transitions are measured at a 1.5V level.

Application Notes

More than one TDC1028 may be connected together to form filters of greater length, greater signal data resolution, and/or greater coefficient resolution.

The simplest form of expansion is length. Each TDC1028 has a data and a sum input, and a data and a sum output. To make a filter of greater length, connect the data and sum outputs to the data and sum inputs of the next device, as shown in Figures 2 and 3. This procedure is used for each section of a filter built with higher resolution for signal data and coefficients. Note that the sum inputs of the first device in a series (the one to which signal data is directly applied) must be supplied with a "zero" input (that is, all sum input pins must be grounded). This form of expansion is also used in combination with increased resolution, and is directly applicable to those cases.

Two options are available for increased resolution. The first method uses external adders and pipeline registers, the second uses the internal adders and pipeline registers of the TDC1028. Block diagrams of these methods are shown in Figures 9 and 10. The second method significantly increases latency; the output experiences a significant delay with respect to that of an ideal but causal Finite Impulse Response filter.

This section discusses the increasing of signal data and coefficient resolution when both signal data and coefficients are given in two's complement notation. For additional information, refer to TRW LSI Products Application Note TP-22.

The basic approach is to divide the word that requires greater resolution into two or more parts of four bits each. A separate section will be needed for every four bits or fraction thereof. Usually, both signal data words and coefficients will be divided. Next, a filter section is assigned to each possible combination of non-overlapping 4-bit groups of signal data with 4-bit groups of coefficients. (A filter section is assigned for each element in the cross-product of the signal data and coefficient data word spaces.) This process is shown in Figure 3, which illustrates division into 4-bit segments, used with both options for increasing resolution.

The choice is made between the adder option and the no-adder option. If the adder option is chosen, a pipelined adder must be designed using MSI components. A complete 16-tap filter using 8-bit signal data words and 8-bit coefficients is shown in Figure 9. Care must be taken to assure that the outputs of each of the sections are properly weighted. Note that the Two's Complement Data (TCD) pin should be active only in the sections which have the MSD of the data word as the input. Likewise, the Two's Complement Coefficient (TCC) pin should be active only on the sections which have the MSD of the coefficient word as the input.

However, another approach is possible. The TDC1028 has internal adders which are not used in the above configuration. Those are the adders in the first device in each section. By introducing suitable delays, these adders can be used to increase resolution without using external adders. A sample circuit, a complete 16-tap filter using 8-bit signal data words and 8-bit coefficients, is shown in Figure 10. Notice that this introduces an eighteen sample delay in the signal path. The necessary 8-bit wide by 9 or 18 stage long shift registers are provided by TRW's TDC1011.

Figure 9.

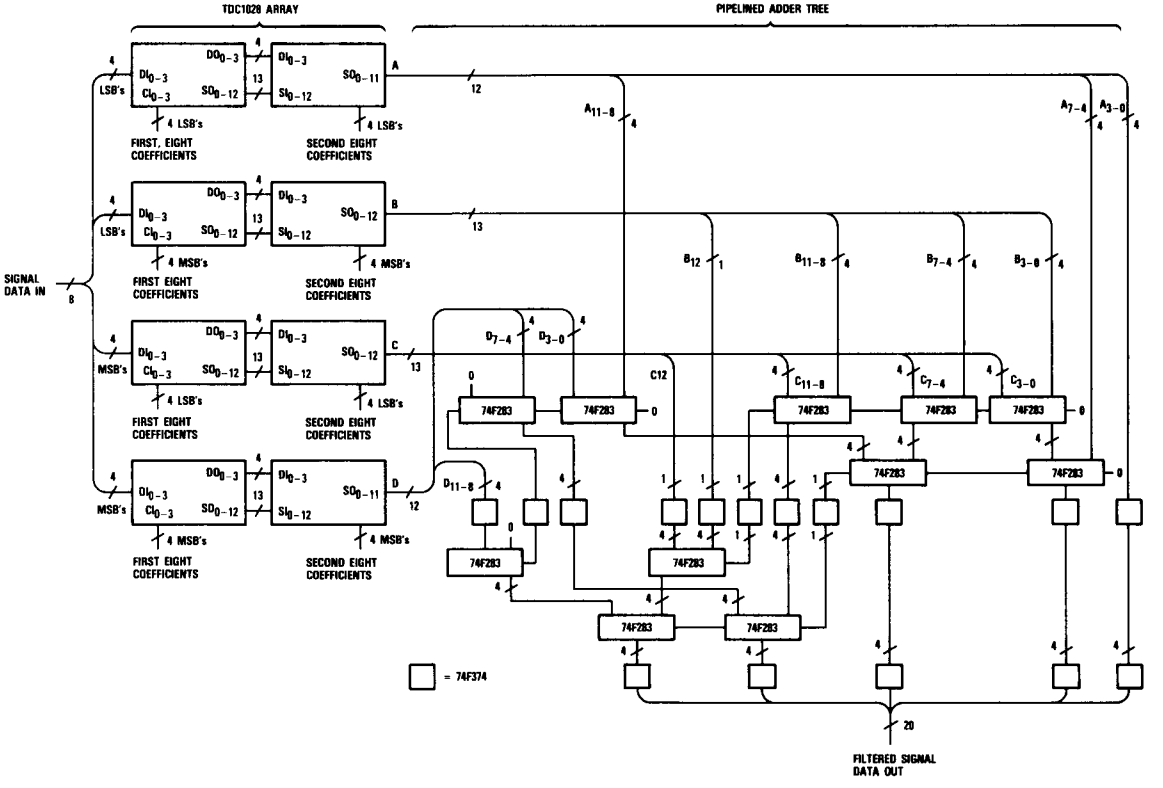
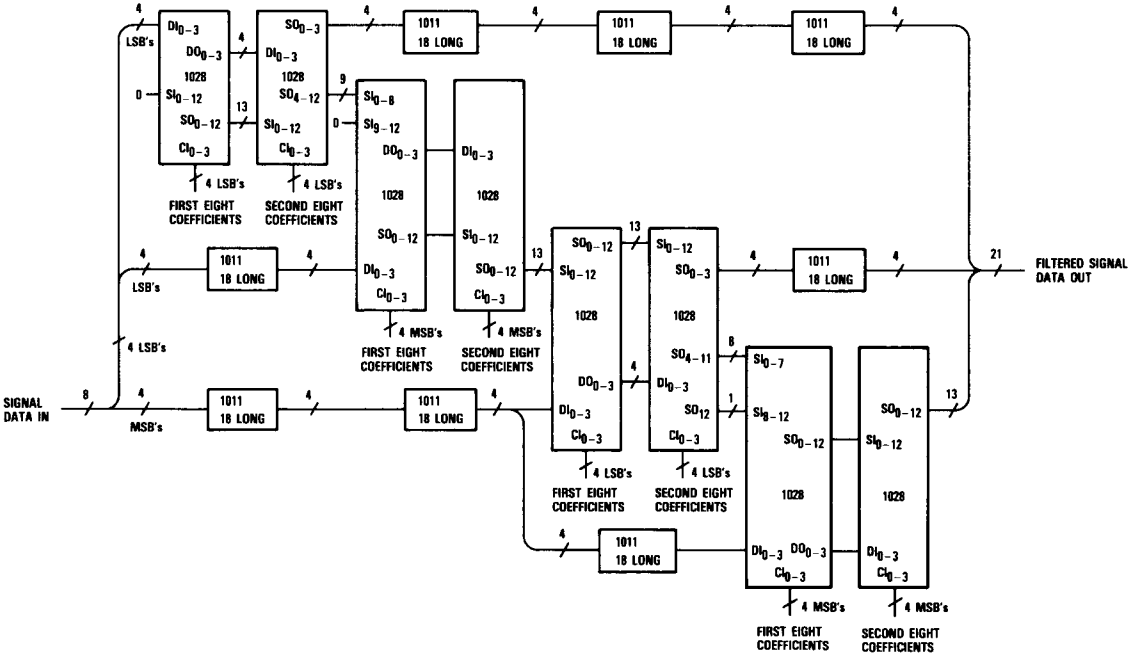

TDC1028 ARRAY
PIPELINED ADDER TREE
SIGNAL DATA IN
LSB's
MSB's
FIRST, EIGHT COEFFICIENTS
SECOND EIGHT COEFFICIENTS
74F283
74F374
FILTERED SIGNAL DATA OUT

Figure 10.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1028J4C	STD – T_A = 0°C to 70°C	Commercial	48 Pin Hermetic Ceramic DIP	1028J4C
TDC1028J4A	EXT – T_C = –55°C to 125°C	High Reliability	48 Pin Hermetic Ceramic DIP	1028J4A