

## 4K-bit TTL bipolar PROM (512 x 8)

82S141

## FEATURES

- Address access time: 90ns max
- Input loading: -150 $\mu$ A max
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: 3-State
- Unprogrammed outputs are Low level

- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

## APPLICATIONS

- Prototyping/volume production
- Sequential controllers

## DESCRIPTION

The 82S141 is field programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S141 includes on-chip decoding and four chip enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in based organizations.

## ORDERING INFORMATION

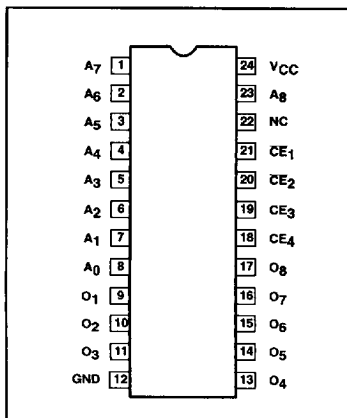
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-pin Ceramic DIP (600mil-wide)	82S141/BJA	GDIP1-T24
24-pin Ceramic Flat Pack	82S141/BKA	GDFP2-F24

\* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

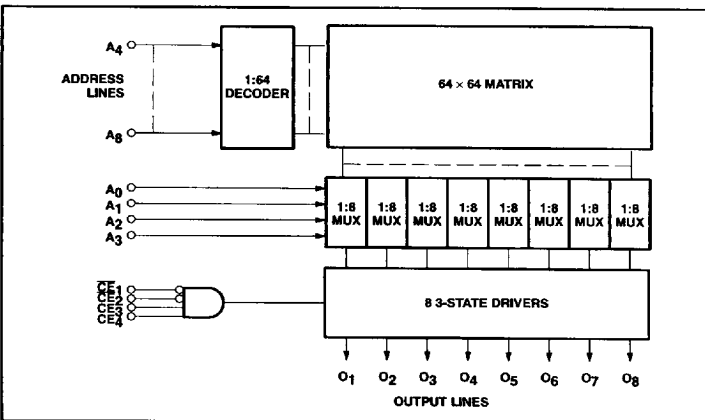
## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	+7	V <sub>DC</sub>
V <sub>I</sub>	Input voltage	+5.5	V <sub>DC</sub>
V <sub>O</sub>	Output voltage Off-State	+5.5	V <sub>DC</sub>
T <sub>A</sub>	Operating temperature range	-55 to +125	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

## PIN CONFIGURATION



## BLOCK DIAGRAM



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## DC ELECTRICAL CHARACTERISTICS

 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1, 2</sup>	LIMITS			UNIT
			Min	Typ <sup>5</sup>	Max	
<b>Input voltage</b>						
$V_{IL}$	Low	$V_{CC} = 4.5\text{V}$ , $I_I = -18\text{mA}$	2.0	-0.8	0.8	V
$V_{IH}$	High					V
$V_{IK}$	Clamp					V
<b>Output voltage</b>						
$V_{OL}$	Low	$V_{CC} = 4.5\text{V}$ , $\overline{CE}_{1,2} = \text{Low}$ , $CE_{3,4} = \text{High}$ $I_O = 9.6\text{mA}$ $I_O = -2\text{mA}$	2.4		0.5	V
$V_{OH}$	High					V
<b>Input current</b>						
$I_{IL}$	Low	$V_{CC} = 5.5\text{V}$ $V_I = 0.45\text{V}$ $V_I = 5.5\text{V}$			-150	$\mu\text{A}$
$I_{IH}$	High					$\mu\text{A}$
<b>Output current</b>						
$I_{OZ}$	Hi-Z state	$V_{CC} = 5.5\text{V}$ $\overline{CE}_{1,2} = \text{High}$ , $CE_{3,4} = \text{Low}$ , $V_O = 5.5\text{V}$ $\overline{CE}_{1,2} = \text{High}$ , $CE_{3,4} = \text{Low}$ , $V_O = 0.4\text{V}$			+40 -40	$\mu\text{A}$ $\mu\text{A}$
$I_{OS}$	Short circuit <sup>3</sup>					$\overline{CE}_{1,2} = \text{Low}$ , $CE_{3,4} = \text{High}$ , $V_O = 0\text{V}$ $V_{CC} = 5.5\text{V}$ , High Stored
<b>Supply current</b>						
$I_{CC}$		$\overline{CE}_{1,2} = \text{High}$ , $CE_{3,4} = \text{Low}$ $V_{CC} = 5.5\text{V}$			125 185	mA
<b>Capacitance<sup>6</sup></b>						
$C_{IN}$	Input	$V_{CC} = 5.0\text{V}$ , $\overline{CE}_{1,2} = \text{High}$ $V_I = 2.0\text{V}$ $V_O = 2.0\text{V}$			5 8	pF
$C_{OUT}$	Output					pF

## AC ELECTRICAL CHARACTERISTICS

 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ 

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ <sup>5</sup>	Max	
$t_{AA}$	Access time <sup>4</sup>	Output	Address	50	90	ns	
$t_{CE}$		Output	Chip enable	20	50	ns	
$t_{CD}$	Disable time	Output	Chip disable	20	50	ns	

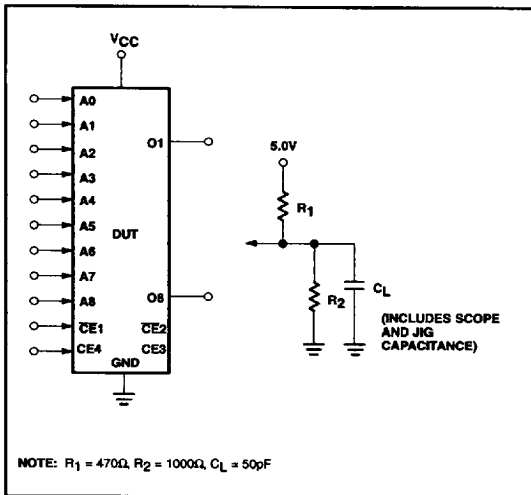
## NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1  $\mu\text{s}$ .
5. Typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = +25^{\circ}\text{C}$ .
6. Guaranteed, but not tested.

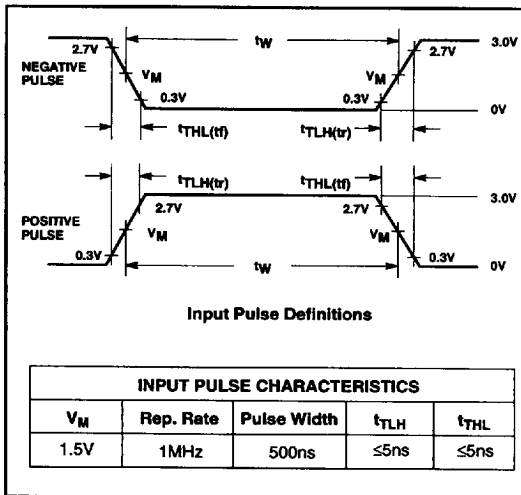
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## TEST LOAD CIRCUITS



## VOLTAGE WAVEFORMS



## TIMING DIAGRAMS

