

DTL Circuits

General Description

The National Semiconductor family of DTL is a complete line of compatible monolithic integrated circuits designed to operate at medium speed with medium power dissipation and high fan-out. The DTL family is available in 14-pin epoxy B or ceramic dual-in-line packages for operation over the 0°C to +75°C temperature range.

The DTL line is composed of a variety of NAND gates that allow complete design flexibility. The gates are available with either 6k pull-up resistors for low power dissipation, or 2k pull-up resistors for increased speed. The gate outputs can be wired together to achieve the wired-OR function.

The NAND gates are complemented with the DM932 and DM957 buffers which provide higher fan-out; the DM944 and DM958 power gates which have an open collector, and the DM933 extender which allows increased fan-in for both buffers and DM930 and DM961 gates.

The flip-flops in this family are of the direct coupled master-slave type, with direct clear and direct set lines. The dual flip-flops include ones with either common or separate clocks.

The DM945 and DM948 are R-S flip-flops which can be externally cross coupled to perform in the JK mode. They are of the master-slave type with output buffers to provide isolation from the output load. These flip-flops feature both asynchronous set and clear lines. The DM945 has a 6k pull-up resistor and the DM948 has a 2k pull-up resistor.

The DM9093 and DM9094 are dual JK flip-flops of the DM945 and DM948 variety respectively. Both flip-flops have separate clocks and no asynchronous clear lines.

The DM9097 and DM9099 are dual JK flip-flops of the DM948 and DM945 variety respectively. Both flip-flops have common clocks and both asynchronous set and clear lines.

The DM930 series is directly compatible with the TTL devices manufactured by National and can be used in conjunction with them in those portions of a system where speed is not the main consideration.

Features

- **NAND Gates**
 - DM930, DM961 - dual four input gates with expanders
 - DM935, DM936, DM937 - hex inverters
 - DM946, DM949 - quad two input gates
 - DM962, DM963 - triple three input gates
 - DM1800, DM1801 - dual five input gates
- **Buffers/Extenders**
 - DM932 - dual four input buffer with expander
 - DM933 - dual four input extender
 - DM944 - dual four input power gate with expander
 - DM957 - quad two input buffer
 - DM958 - quad two input power gate
- **Flip-Flops**
 - DM945, DM948 - RS flip-flops
 - DM9093, DM9094, DM9097, DM9099 - dual JK flip-flops

Truth Tables

SYNCHRONOUS TRUTH TABLE

t _n				t _n + 1
S1 Pin 3	S2 Pin 4	C1 Pin 12	C2 Pin 11	Q Pin 6
L	X	L	X	Q _n
L	X	X	L	Q _n
X	L	L	X	Q _n
X	L	X	L	Q _n
L	X	H	H	L
X	L	H	H	L
H	H	L	X	H
H	H	X	L	H
H	H	H	H	*

* - Indeterminate State
X - Don't Care

ASYNCHRONOUS TRUTH TABLE

S _D Pin 10	C _D Pin 5	Q Pin 6	Q̄ Pin 9
H	H	NC	NC
L	H	H	L
H	L	L	H
L	L	H	H

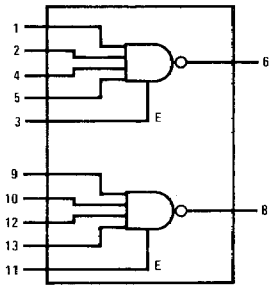
JK TRUTH TABLE

t _n			t _n + 1
S1 Pin 3	C1 Pin 12	Q Pin 6	Q
L	L	Q _n	Q _n
H	L	L	H
L	H	L	L
H	H	H	Q̄ _n

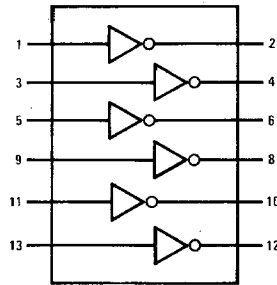
(Connect S2 to Q̄, C2 to Q) Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs, and are independent of all other inputs.



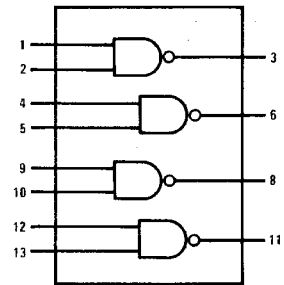
Connection and Logic Diagrams



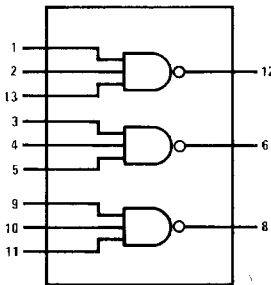
930(J, (N)); 932(J, (N));
944(J, (N)); 961(J, (N));
1800(J, (N)); 1801(J, (N))



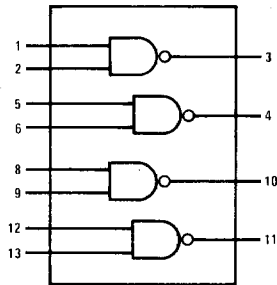
935(J, (N)); 936(J, (N));
937(J, (N))



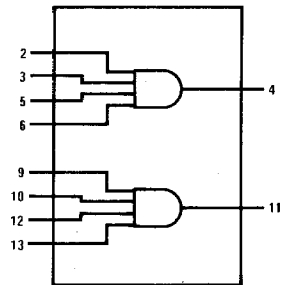
946(J, (N)); 949(J, (N))



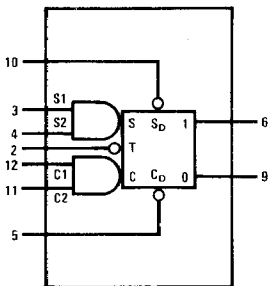
962(J, (N)); 963(J, (N))



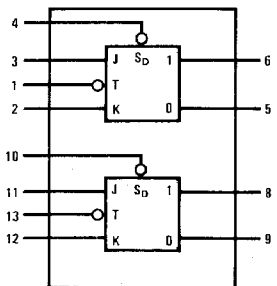
957(J, (N)); 958(J, (N))



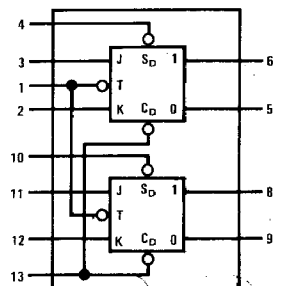
933(J, (N))



945(J, (N)); 948(J, (N))



9093(J, (N)); 9094(J, (N))



9097(J, (N)); 9099(J, (N))

Electrical Characteristics ($V_{CC} = 5.0V$)

PARAMETER		CONDITIONS		DM930, DM935, DM936, DM937, DM946 DM949, DM961, DM962, DM963, DM1800, DM1801						UNITS
				0°C		25°C		75°C		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{CEX}	Output Leakage Current	$V_i = 0, V_o = 5V$	2k Gates			100			μA	
			6k Gates			100				
V_{OH}	High Level Output Voltage(1)	$V_{iL} = \text{Max}, I_{oH} = \text{Max}$		2.6		2.6		2.5	V	
V_{OL}	Low Level Output Voltage	$V_i = V_{iH}, I_{oL} = \text{Max}$			0.45		0.45	0.50	V	
I_{iH}	High Level Input Current (1)	$V_i = V_R$			5		5	10	μA	
I_{iL}	Low Level Input Current	$V_i = V_F$			-1.40		-1.40	-1.33	mA	
I_{OS}	Short Circuit Output Current	$V_i = 0$	2k Gates			-1.85	-3.90		mA	
			6k Gates		1.30	-0.61	-1.30	-1.25		
I_{CC1}	Supply Current	$V_{CC} = 5V, V_i = V_R$	2k Gates				5.9		mA	
			6k Gates				4			
I_{CC2}	Supply Current	$V_{CC} = 8V, V_i = 0$					4		mA	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 30 \text{ pF}, R_L = 3.9 \text{ k}\Omega$	2k Gates			15	60		ns	
			6k Gates			25	80			
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L = 50 \text{ pF}, R_L = 400\Omega$	2k Gates			10	30		ns	
			6k Gates			10	30			

Notes

(1) Applies to all gates except DM935.

Test Conditions

GATES

TEMP.	V_{iH} VOLTS	V_{iL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	(6k) I_{oL} (mA)	(2k) I_{oL} (mA)	(6k) I_{oH} (mA)	(2k) I_{oH} (mA)
0°C	2.0	1.2	4.0	0.45	-	12.0	11.0	-0.12	-0.5
+25°C	1.9	1.1	4.0	0.45	5.0	12.0	11.0	-0.12	-0.5
+75°C	1.8	0.95	4.0	0.50	-	11.4	10.4	-0.12	-0.5

Electrical Characteristics ($V_{CC} = 5.0V$)

PARAMETER		CONDITIONS		DM932, DM933, DM944, DM957, DM958						UNITS
				0°C		25°C		75°C		
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$I_{IL} = I_{FD}$	933	0.75	0.90	0.68	0.82	0.60	0.75	V
I_{CEX}	Output Leakage Current	$V_I = 0, V_O = 5V$	932, 957				100			μA
			944, 958		25		100		200	
V_{OH}	High Level Output Voltage	$V_I = V_{IL}, I_{OH} = \text{Max}$	932, 957	2.6		2.6		2.5		V
V_{OL}	Low Level Output Voltage	$V_I = V_{IH}, I_{OL} = \text{Max}$	All Except 933		0.45		0.45		0.50	V
I_{IH}	High Level Input Current	$V_I = V_R$	933		5		5		10	μA
			Others		5		5		10	
I_{IL}	Low Level Input Current	$V_I = V_F$	All Except 933		-1.40		-1.40		-1.33	mA
I_{OS}	Short Circuit Output Current	$V_I = 0$	932, 957		-16		-16		-14	mA
I_{CC1}	Supply Current	$V_{CC} = 5V, V_I = V_R$	932				30.0			mA
			944				22.5			
			957				60.0			
			958				4.5			
I_{CC2}	Supply Current	$V_{CC} = 8V, V_I = 0$	All Except 933				4		mA	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 500 \text{ pF}, R_L = 510\Omega$	932, 957			25	80			ns
		$C_L = 20 \text{ pF}, R_L = 510\Omega$	944, 958			15	50			
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L = 500 \text{ pF}, R_L = 150\Omega$	932, 957			15	40			ns
		$C_L = 100 \text{ pF}, R_L = 150\Omega$	944, 958			10	35			

Test Conditions

BUFFERS/EXTENDERS

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	I_{FD} mA	932 957	944 958	932 957
							I_{OL} (mA)	I_{OL} (mA)	I_{OH} (mA)
0°C	2.0	1.2	4.0	0.45	-	-2	36	40	-2.0
+25°C	1.9	1.1	4.0	0.45	5.0	-2	36	40	-2.5
+75°C	1.8	0.95	4.0	0.50	-	-2	34	36	-3.0

Electrical Characteristics ($V_{CC} = 5.0V$)

PARAMETER	CONDITIONS	DM945, DM948, DM9093, DM9094 DM9097, DM9099						UNITS		
		0°C		25°C		75°C				
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{CEX}	Output Leakage Current	$V_i = 0, V_O = 5V$		945, 948		100		μA		
V_{OH}	High Level Output Voltage	$V_i = V_{IL}$ $I_{OH} = \text{Max}$	Data	945, 948	2.6	2.6	2.5	V		
			Set, Reset	945, 948	2.6	2.6	2.6			
			All	9093, 9094 9097, 9099	2.6	2.6	2.5			
V_{OL}	Low Level Output Voltage	$V_i = V_{IH}, I_{OL} = \text{Max}$		All	0.45	0.45	0.50	V		
I_{IH}	High Level Input Current	$V_i = V_R$	Data	945, 948	5.0	5.0	10.0	μA		
			Set, Reset	945, 948	5.0	5.0	10.0			
			Clock	945, 948	30	30	40			
				9093, 9094 9097, 9099	20	20	30			
			Clear	9097, 9099	40	40	60			
			All Except Clocks, and Direct Clear on 9097, 9099	9093, 9094 9097, 9099	10	10	20			
I_{IL}	Low Level Input Current	$V_i = V_F$	Data	All	0.95	-0.95	-0.90	mA		
			Set, Reset	945, 948	2.8	-2.8	-2.67			
			Direct Set	9093, 9094 9097, 9099	-2.8	2.8	2.67			
			Clock	945	-2.8	-2.8	-2.66			
				948, 9093 9094	-2.8	2.8	2.67			
			Clock, Direct Clear	9097, 9099	-5.6	5.6	5.34			
I_{OS}	Short Circuit Output Current	$V_i = 0$	2k	1.77	4.2	-1.77	4.2	-1.60	-4.0	mA
			6k	0.59	1.41	-0.59	-1.41	-0.55	-1.38	
I_{CC1}	Supply Current	$V_{CC} = 5V$ (Inputs Open)	945				14			mA
			948				17			
			9093, 9099				28			
			9094, 9097				34			
I_{CC2}	Supply Current	$V_{CC} = 8V, V_i = 0$	945				18			mA
			948				23			
			9093, 9099				36			
			9094, 9097				45			
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 30 \text{ pF}, R_L = 2 \text{ k}\Omega$	2k			25	75			ns
			6k			25	100			
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L = 50 \text{ pF}, R_L = 330\Omega$				15	55			ns

Test Conditions

FLIP-FLOPS

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	945 9093	948 9094	945 9093	948 9094	945 9093	948 9094
						9099	9097	9099	9097	9099	9099
0°C	2.0	1.2	4.0	0.45	-	1.15	1.30	16.8	15.4	-0.12	-0.5
+25°C	1.9	1.1	4.0	0.45	5.0	0.95	1.15	16.8	15.4	-0.12	-0.5
+75°C	1.8	0.95	4.0	0.50	-	0.65	0.85	16.0	14.6	-0.12	-0.5

