National Semiconductor

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100364
Low Power 16-Input Multiplexer

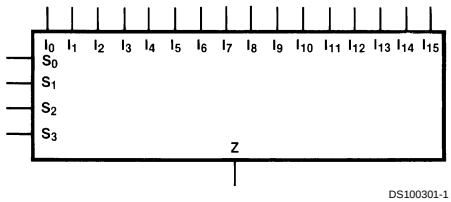
General Description

The 100364 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0–S_3). Their decoding is shown in the truth table. Output data polarity is the same as the seleted input data. All inputs have 50 kΩ pulldown resistors.

Features

- 35% power reduction of the 100164
- 2000V ESD protection
- Pin/function compatible with 100164
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Standard Microcircuit Drawing (SMD) 5962-9459201

Logic Symbol

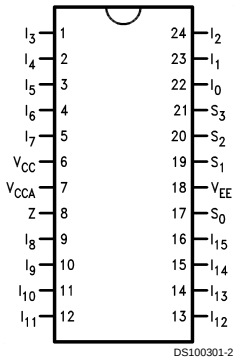


DS100301-1

Pin Names	Description
I_0–I_{15}	Data Inputs
S_0–S_3	Select Inputs
Z	Data Output

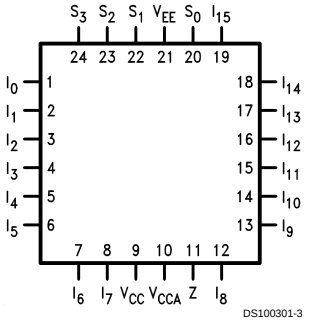
Connection Diagrams

24-Pin DIP



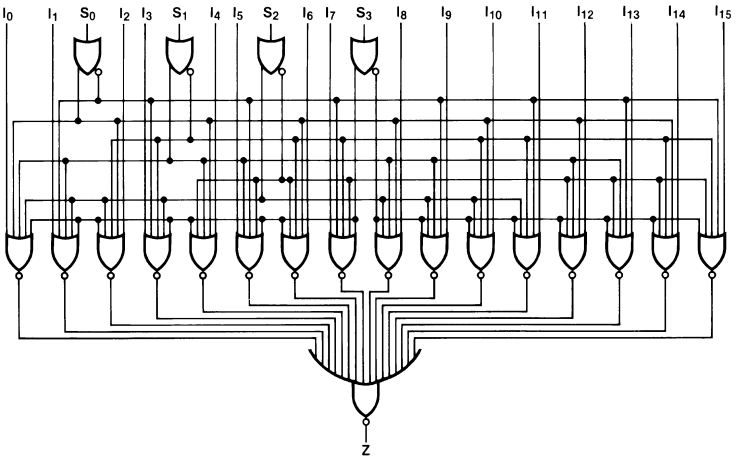
DS100301-2

24-Pin Quad Cerpak



DS100301-3

Logic Diagram



DS100301-5

Truth Table

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
Pin Potential to	
Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current	
(DC Output HIGH)	−50 mA
ESD (Note 2)	≥ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for All Inputs		(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs		(Notes 3, 4, 5, 6)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 3, 4, 5)
I_{IH}	Input HIGH Current		300	µA	0˚C to +125˚C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		(Notes 3, 4, 5)
			450	µA	−55˚C			
I_{EE}	Power Supply Current	−95	−35	mA	−55˚C to +125˚C	Inputs Open		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups, 1, 2, 3, 7 and 8.

Note 5: Sampled tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7 and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.50	2.60	0.60	2.40	0.60	2.80	ns	*Figures 1, 2*	(Notes 7, 8, 9)
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.70	3.30	0.90	3.10	1.00	3.50	ns		
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	0.50	2.90	0.70	2.60	0.60	3.00	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.20	0.20	1.20	0.20	1.20	ns		(Note 10)

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C temp., Subgroups A10 and A11.

Note 10: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Test Circuit

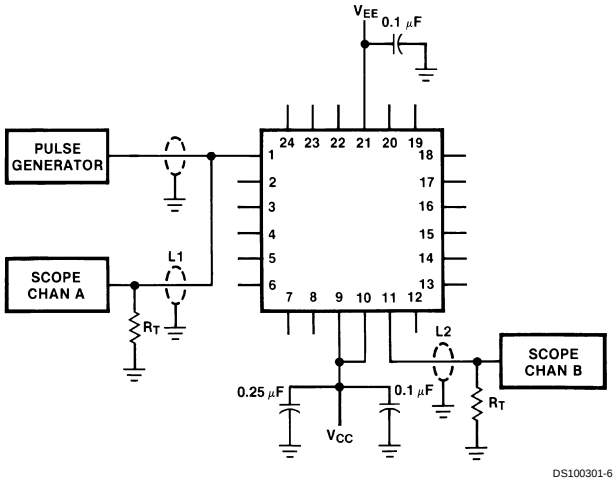
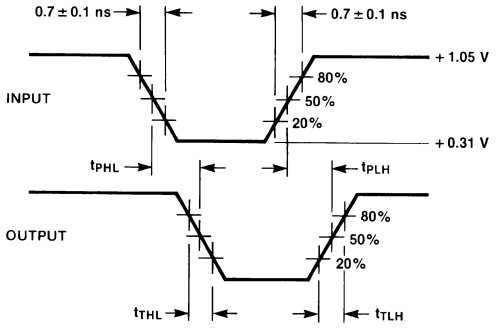


FIGURE 1. AC Test Circuit

Switching Waveforms



Note 11: V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

Note 12: L1 and L2 = Equal length 50Ω impedance lines

Note 13: R_T = 50Ω terminator internal to scope

Note 14: Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

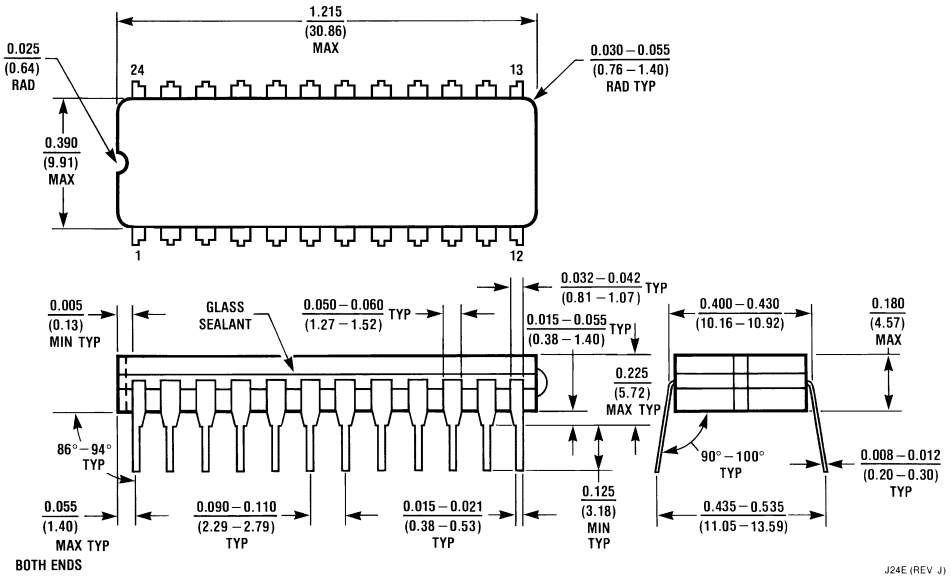
Note 15: All unused outputs are loaded with 50Ω to GND

Note 16: C_L = Fixture and stray capacitance ≤ 3 pF

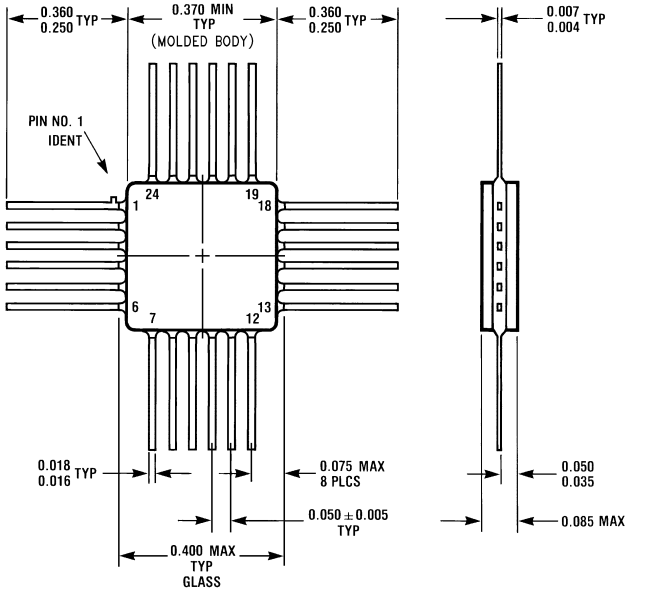
Note 17: Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B

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