



Quad Exclusive OR Gate

**ELECTRICALLY TESTED PER:
5962-8755801**

The 10H513 is a Quad Exclusive OR Gate with an enable common to all gates. The outputs may be wire-ORed together to perform a 4-bit comparison function ($A = B$). The enable is active LOW.

- 250 mW Max/Pkg (No Load)
- $t_{pd} = 2.5$ ns typ
- $t_r, t_f = 2.0$ ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	5	2	GND
AOUT	2	6	3	51 Ω to VTT
BOUT	3	7	4	51 Ω to VTT
A1N	4	8	5	GND
A2N	5	9	7	OPEN
B1N	6	10	8	GND
B2N	7	11	9	OPEN
VEE	8	12	10	VEE
Enable	9	13	12	OPEN
C1N	10	14	13	GND
C2N	11	15	14	OPEN
D1N	12	16	15	GND
D2N	13	1	17	OPEN
COUT	14	2	18	51 Ω to VTT
DOUT	15	3	19	51 Ω to VTT
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

VTT = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

Input		\bar{E}	Output
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
\emptyset	\emptyset	H	L

\emptyset = Don't Care

Military 10H513

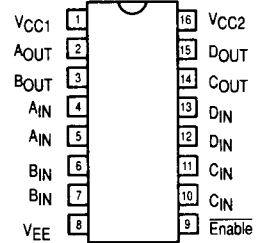


AVAILABLE AS

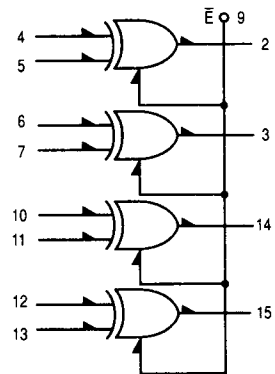
- 1) JAN: N/A
 - 2) SMD: 5962-8755801
 - 3) 883: 10H513/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

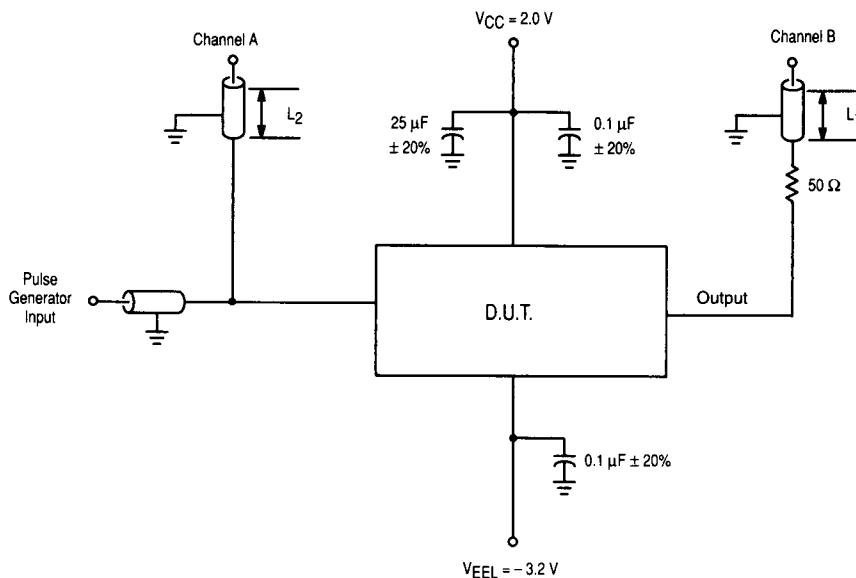
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



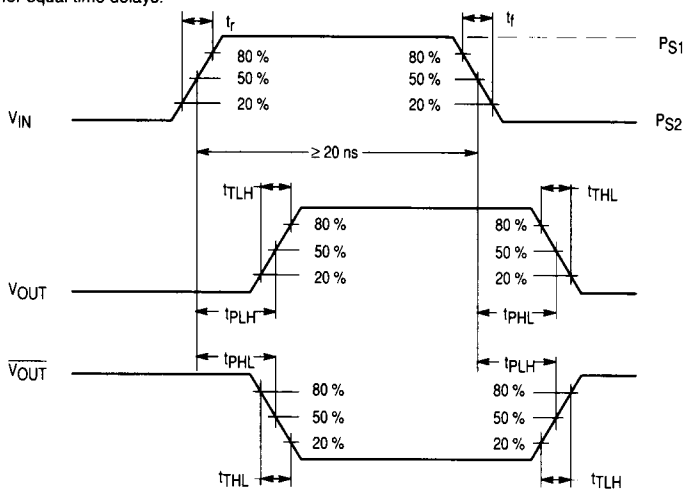
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NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. 2:1 divider may be used.
5. $L_1 = L_2$: Matched for equal time delays.



NOTES

1. $P_{IN} \geq 20$ ns.
2. $f_{IN} = 1.0$ MHz.
3. $t_r = t_f = 1.0$ ns ± 0.1 ns

Figure 1. Switching Test Circuit and Waveforms

10H513 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	PS1	PS2	V _{IL2}	V _{IH2}	V _{CC}	VEE1	VEE2	
T _A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.46	-4.94	
T _A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.46	-4.94	
T _A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.46	-4.94	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to -2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3			V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	VEE1	VEE2	V _{CC}	P. U. T.		
V _{OH}	High Output Voltage	Min	Max	Min	Max	Min	Max	V	4-7 11, 13				8			1, 16	2, 3, 14, 15	
V _{OL}	Low Output Voltage	Min	Max	Min	Max	Min	Max	V					8			1, 16	2, 3, 14, 15	
V _{OHA}	High Output Voltage	Min	Max	Min	Max	Min	Max	V	4-7 10-13		4-7 10-13	4-7 10-13		8		1, 16	2, 3, 14, 15	
V _{OLA}	Low Output Voltage	Min	Max	Min	Max	Min	Max	V	4-7 10-13		4-7 10-13	4-7 10-13		8		1, 16	2, 3, 14, 15	
I _{EE}	Power Supply Current							mA					8			1, 16	8	
I _{IH1}	Input Current High		320		510		510	μA	4, 6 10, 12				8			1, 16	4, 6, 10, 12	
I _{IH2}	Input Current High		270		430		430	μA	5, 7 11, 13				8			1, 16	5, 7, 11, 3	
I _{IH3}	Input Current High		740		1100		1100	μA	9				8			1, 16	9	
I _{IL}	Input Current Low	0.5		0.3		0.5		μA					8	4-7 9-11 13, 14		1, 16	4-7, 9-13	

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Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	PS ₁	PS ₂	V _{IL2}	V _{IH2}	V _{CC}	VEEL
T _A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-2.94
T _A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-2.94
T _A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+25° C		+125° C		-55° C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9 Min	Subgroup 9 Max	Subgroup 10 Min	Subgroup 10 Max	Subgroup 11 Min	Subgroup 11 Max		V _{IN}	V _{OUT}	V _{CC}	VEEL	PS ₁	PS ₂	P.U.T.	
t _{TLH}	Rise Time	0.6	1.9	0.6	2.0	0.5	1.8	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15	
t _{THL}	Fall Time	0.6	1.9	0.6	2.0	0.5	1.8	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15	
t _{PLH} Data	Propagation Delay Low to High (A or B to Out)	0.4	1.8	0.5	1.9	0.4	1.7	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15	
t _{pHL} Data	Propagation Delay High to Low (A or B to Out)	0.4	1.8	0.5	1.9	0.4	1.7	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15	
t _{pLH} Enable	Propagation Delay Low to High (Enable to Out)	0.5	2.4	0.6	2.5	0.5	2.3	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15	
t _{pHL} Enable	Propagation Delay High to Low (Enable to Out)	0.5	2.4	0.6	2.5	0.5	2.3	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15	