



CYPRESS SEMICONDUCTOR

T-46-13-29

CY7C268

CY7C269

8192 x 8 Registered Diagnostic PROM

Features

- CMOS for optimum speed/power
- High speed
 - 15-ns max set-up
 - 12-ns clock to output
- Low power
 - 660 mW (commercial)
 - 770 mW (military)
- On-chip edge-triggered registers
 - Ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register
 - For serial observability and controllability of the output register
- EPROM technology
 - 100% programmable
 - Reprogrammable (7C269W)
- 5V ±10% V_{CC}, commercial and military
- Capable of withstanding >2001V static discharge
- Slim 300-mil, 28-pin plastic or hermetic DIP (7C269)

Functional Description

The CY7C268 and the CY7C269 are 8192 x 8 registered diagnostic PROMs. They are both organized as 8,192 words by 8 bits wide, and they have both a pipeline output register and an onboard diagnostic shift register. Both devices feature a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM, and may be programmed to any desired value.

The CY7C268 has 32 pins and features full diagnostic capabilities while the CY7C269 provides limited diagnostics and is available in a space-efficient 28-pin package. This allows the designers to optimize designs for either board-area efficiency with the CY7C269, or combine the CY7C268 with other diagnostic products using the standard interface.

CY7C268

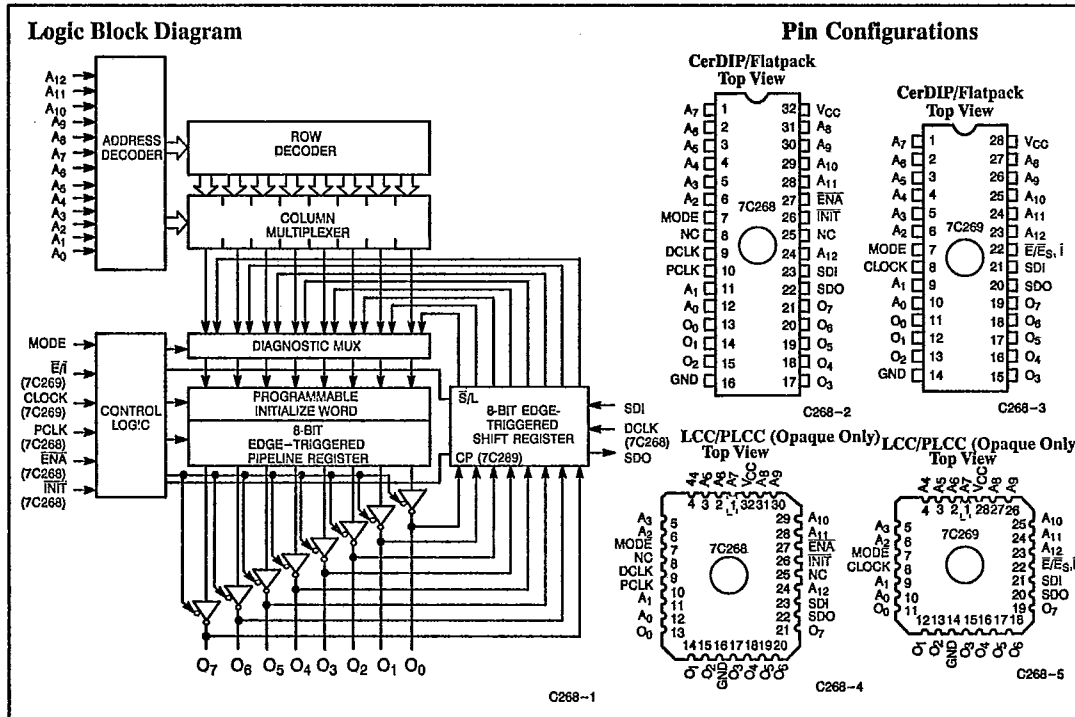
The CY7C268 provides 13 address signals (A₀ through A₁₂), 8 data out signals (O₀ through O₇), ENA (enable), PCLK (pipeline clock) and INIT (initialize) for control.

The full standard feature diagnostics of the CY7C268 utilize the SDI and SDO (shift in and shift out), MODE, and DCLK signals. These signals allow serial data to be shifted into and out of the diagnostic shift register at the same time the pipeline register is used for normal operation. The MODE signal is used to control the transfer of the information in the diagnostic register to the pipeline register, or the data on the output bus into the diagnostic register. The data on the output bus may be provided from the pipeline register or from an external source.

When the MODE signal is LOW, the PROM operates in a normal pipeline mode. The contents of the addressed memory location are loaded into the pipeline register on the rising edge of PCLK. The outputs are enabled with the ENA signal either synchronously or asynchronously, depending on how the device is configured when programmed. If programmed for asynchronous enable, ENA LOW enables the outputs. If configured for synchronous enable, ENA LOW will enable the outputs synchronously with PCLK during the rising edge of PCLK. ENA



PROMS





Functional Description (continued)

HIGH will synchronously disable the outputs during the rising edge of PCLK. The asynchronous initialize signal, INIT, transfers the initialize byte into the pipeline register on a HIGH to LOW transition. INIT LOW disables PCLK and must transition back to a HIGH in order to enable PCLK. DCLK shifts data into SDI and out of SDO on each rising edge.

When MODE is HIGH, the rising edge of the PCLK signal loads the pipeline register with the contents of the diagnostic register. Similarly, DCLK, in this mode, loads the diagnostic register with the information on the data output pins. The information loaded will be either the contents of the pipeline register if the outputs are enabled, or data on the bus if the outputs are disabled (in a high-impedance state).

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The CY7C269 is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, it has 13 address signals (A₀ through A₁₂), 8 data out signals (O₀ through O₇), E/I (Enable or Initialize), and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SDI (shift in) and SDO (shift out). Normal pipelined operation and diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the 7C269 is programmed to perform either the Enable or the Initialize function. If the E/I pin is

used for a INIT (asynchronous initialize) function, the outputs are permanently enabled and the initialize word is loaded into the pipeline register on a HIGH to LOW transition of the INIT signal. The INIT LOW disables CLOCK and must return high to re-enable CLOCK. If the E/I pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation. This enable function then operates exactly the same as the 7C268.

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The E/I signal becomes a secondary mode signal designating whether to shift the diagnostic shift register or to load either the diagnostic register or the pipeline register. If E/I is HIGH, CLOCK performs the function of DCLK, shifting SDI into the least-significant location of the diagnostic register and all bits one location toward the most-significant location on each rising edge. The contents of the most-significant location in the diagnostic register are available on the SDO pin.

If the E/I signal is LOW, SDI becomes a direction signal, transferring the contents of the diagnostic register into the pipeline register when SDI is LOW. When SDI is HIGH, the contents of the output pins are transferred into the diagnostic register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the outputs are enabled, the contents of the pipeline register are transferred into the diagnostic register. If the outputs are disabled, an external source of data may be loaded into the diagnostic register. In this condition, the SDO signal is internally driven to be the same as the SDI signal, thus propagating the "direction of transfer information" to the next device in the string.

Selection Guide

		7C269-15	7C269-18	7C269-25
Maximum Set-Up Time (ns)		15	18	25
Maximum Clock to Output (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		140	140

		7C268-40 7C269-40	7C268-50 7C269-50	7C268-60 7C269-60
Maximum Set-Up Time (ns)		40	50	60
Maximum Clock to Output (ns)		20	25	25
Maximum Operating Current (mA)	Commercial	100	80	80
	Military		120	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature - 65°C to +150°C
- Ambient Temperature with Power Applied - 55°C to +125°C
- Supply Voltage to Ground Potential - 0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State - 0.5V to +7.0V
- DC Input Voltage - 3.0V to +7.0V
- DC Program Voltage 13.0V
- UV Exposure 7258 Wsec/cm²

- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[1]	- 40°C to +85°C	5V ± 10%
Military ^[2]	- 55°C to +125°C	5V ± 10%



Electrical Characteristics Over the Operating Range^{3, 4}

Parameters	Description	Test Conditions	7C269-15		7C269-18		7C269-25		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	Com'l	0.4		0.4		0.4	V
		V _{CC} = Min., I _{OL} = 6.0 mA	Mil	0.4		0.4		0.4	
V _{IH}	Input HIGH Voltage		2.0		2.0		2.0		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _{IN} ≤ V _{CC}	- 10	+10	- 10	+10	- 10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	- 40	+40	- 40	+40	- 40	+40	μA
I _{OS} ⁵	Output Short Circuit Current			90		90		90	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	120		120		120	mA
			Mil			140		140	
V _{PP}	Programming Supply Voltage		12	13	12	13	12	13	V
I _{PP}	Programming Supply Current			50		50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4		0.4	V



Parameters	Description	Test Conditions	7C268-40 7C269-40		7C268-50 7C269-50		7C268-60 7C269-60		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA	Com'l	0.4		0.4		0.4	V
		V _{CC} = Min., I _{OL} = 8.0 mA	Mil	0.4		0.4		0.4	
V _{IH}	Input HIGH Voltage		2.0		2.0		2.0		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _{IN} ≤ V _{CC}	- 10	+10	- 10	+10	- 10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	- 40	+40	- 40	+40	- 40	+40	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = GND		90		90		90	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	100		80		80	mA
			Mil			120		100	
V _{PP}	Programming Supply Voltage		12	13	12	13	12	13	V
I _{PP}	Programming Supply Current			50		50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4		0.4	V

- Notes:
- Contact a Cypress representative for industrial temperature range specifications.
 - T_A is the "instant on" case temperature.
 - See the last page of this specification for Group A subgroup testing information.
 - See Introduction to CMOS PROMs in this Data Book for general information on testing.
 - For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.



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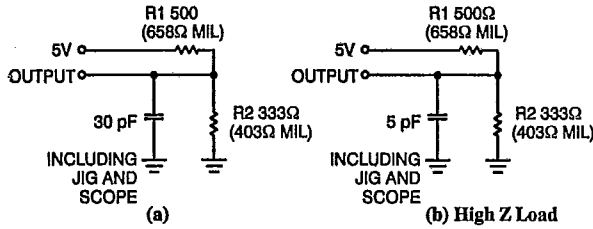
Capacitance^[4, 6]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	10	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

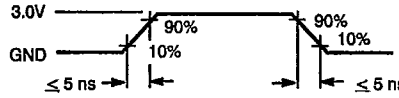
AC Test Loads and Waveforms

Test Load for -15 through -25 speeds



C268-6

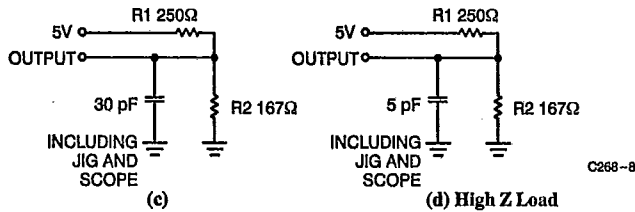
C268-7



Equivalent to: THEVENIN EQUIVALENT

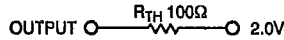


Test Load for -40 through -60 speeds



C268-8

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[3,4]

Parameters	Description	7C269-15		7C269-18		7C269-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{AS}	Address Set-Up to Clock	15		18		25		ns
t _{HA}	Address Hold from Clock	0		0		0		ns
t _{CO}	Clock to Output Valid		12		15		20	ns
t _{PW}	Clock Pulse Width	12		15		15		ns
t _{SES}	E _S Set-Up to Clock (Sync Enable Only)	12		15		15		ns
t _{HES}	E _S Hold from Clock	5		5		5		ns
t _{DI}	INIT to Out Valid		15		18		25	ns
t _{RI}	INIT Recovery to Clock	12		15		20		ns
t _{PWI}	INIT Pulse Width	12		18		25		ns
t _{COS}	Output Valid from Clock (Sync. Mode)		12		15		20	ns
t _{HZS}	Output Inactive from Clock (Sync. Mode)		12		15		20	ns
t _{DOE}	Output Valid from E _{LOW} (Asynch. Mode)		12		15		20	ns
t _{HZE}	Output Inactive from E _{HIGH} (Asynch. Mode)		12		15		20	ns



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Switching Characteristics Over the Operating Range^[3,4] (continued)

Parameters	Description	7C268-40 7C269-40		7C268-50 7C269-50		7C268-60 7C269-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{AS}	Address Set-Up to Clock	40		50		60		ns
t _{HA}	Address Hold from Clock	0		0		0		ns
t _{CO}	Clock to Output Valid		20		25		25	ns
t _{PW}	Clock Pulse Width	15		20		20		ns
t _{SES}	\bar{E}_S Set-Up to Clock (Sync Enable Only)	15		15		15		ns
t _{HES}	\bar{E}_S Hold from Clock	5		5		5		ns
t _{DI}	\bar{INIT} to Output Valid		25		35		35	ns
t _{RI}	\bar{INIT} Recovery to Clock	20		25		25		ns
t _{PWI}	\bar{INIT} Pulse Width	25		35		35		ns
t _{COS}	Output Valid from Clock (Sync. Mode)		20		25		25	ns
t _{HZS}	Output Inactive from Clock (Sync. Mode)		20		25		25	ns
t _{DOE}	Output Valid from \bar{E} LOW (Asynch. Mode)		20		25		25	ns
t _{HZE}	Output Inactive from \bar{E} HIGH (Asynch. Mode)		20		25		25	ns



Diagnostic Mode Switching Characteristics Over the Operating Range^[3,4]

Parameters	Description	7C269-15		7C269-18		7C269-25		7C268-40,50,60 7C269-40,50,60		Units	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{SSDI}	Set-Up SDI to Clock	Com'l	20		25		25		30	ns	
		Mil			25		30		35		
t _{HSDI}	SDI Hold from Clock	Com'l	0		0		0		0	ns	
		Mil			0		0		0		
t _{DSDO}	SDO Delay from Clock	Com'l		20		25		25		30	ns
		Mil				25		30		40	
t _{DCL}	Minimum Clock LOW	Com'l	20		25		25		25	ns	
		Mil			25		25		25		
t _{DCH}	Minimum Clock HIGH	Com'l	20		25		25		25	ns	
		Mil			25		25		25		
t _{SM}	Set-Up to Mode Change	Com'l	20		25		25		25	ns	
		Mil			25		30		30		
t _{HM}	Hold from Mode Change (7C269)	Com'l	0		0		0		0	ns	
		Mil			0		0		0		
t _{MS}	Mode to SDO	Com'l		20		25		25		25	ns
		Mil				25		30		30	
t _{SS}	SDI to SDO	Com'l		30		35		40		40	ns
		Mil				35		40		45	
t _{SO}	Data Set-Up to DCLK	Com'l	20		25		25		25	ns	
		Mil			25		30		30		
t _{HO}	Data Hold from DCLK	Com'l	10		10		10		10	ns	
		Mil			13		13		15		

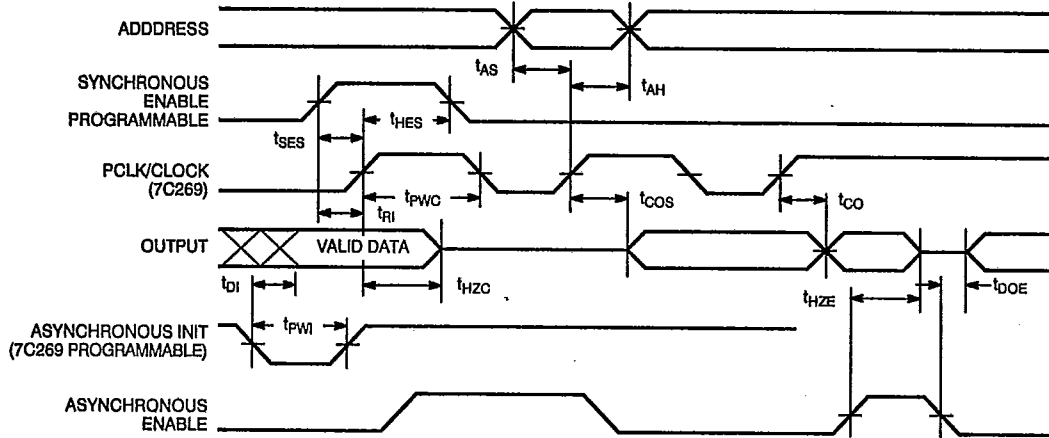


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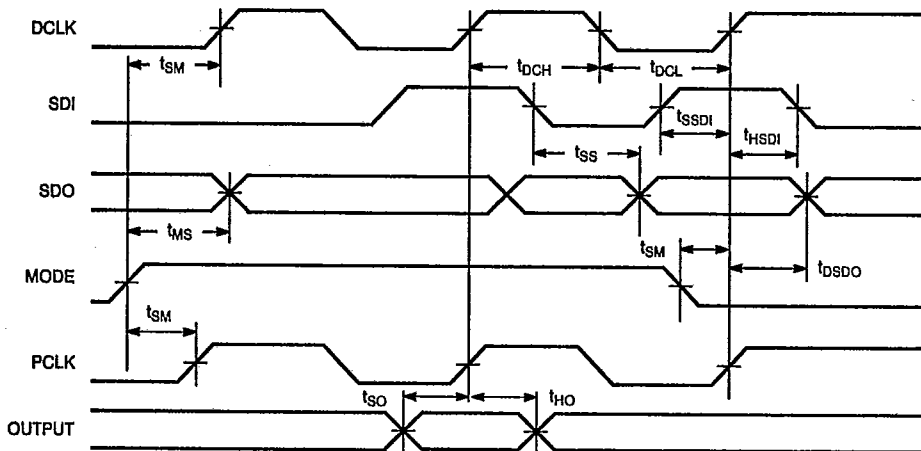
Switching Waveforms^[3,4]

Pipeline Operation (Mode = 0)



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Diagnostic Waveform for the 7C268



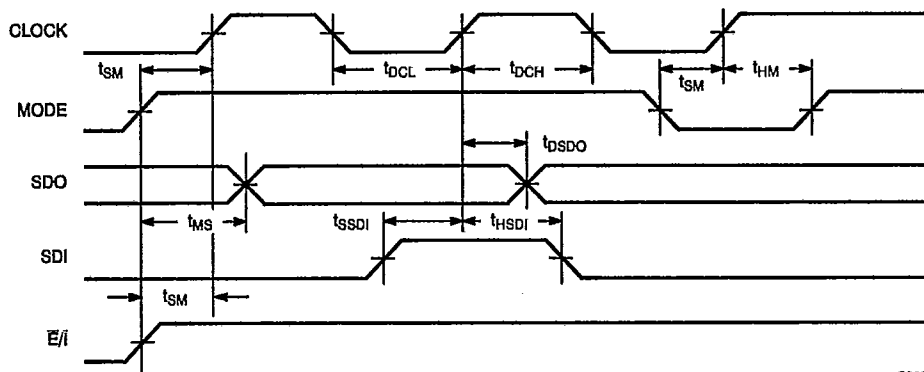
C268-9



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Switching Waveforms^[3,4] (continued)

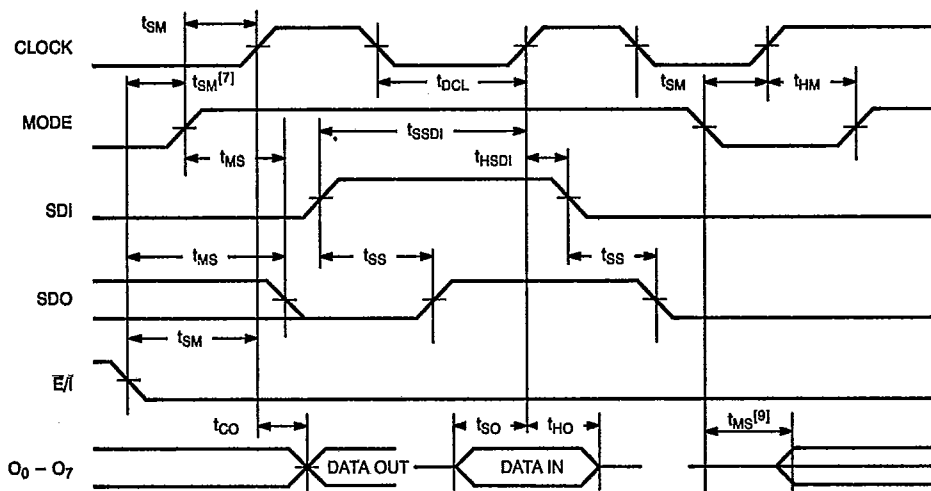
Diagnostic Application for the 7C269 (Shifting the Shadow Register^[8])



C268-12



Diagnostic Application for the 7C269 (Parallel Data Transfer)



C268-11

- Notes:
- 7. Asynchronous enable mode only.
 - 8. Diagnostic register = shadow register = shift register.
 - 9. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H → L) then the output impedance change delay is t_{MS} .



Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
8191	1FFF	Data
8192	2000	Init Byte
8193	2001	Control Byte

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Control Byte

- 00 Asynchronous output enable (default condition)
- 01 Synchronous output enable
- 02 Asynchronous initialize (CY7C269 only)

Table 1. CY7C268 Mode Selection

Mode	Pin Function ⁽¹⁰⁾								
	Read or Output Disable	A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
	Other	A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Load SR to PR		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Load Output to SR		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Shift SR		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Asynchronous Enable Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Synchronous Enable Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Asynchronous Initialization Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Memory		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Verify		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Inhibit		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Synchronous Enable		V _{IHP}	V _{IHP}	A ₁₀ - A ₇	V _{IHP}	V _{PP}	A ₄ - A ₃	V _{IHP}	V _{PP}
Program Initial Byte		X	V _{ILP}	A ₁₀ - A ₇	V _{IHP}	V _{PP}	A ₄ - A ₃	V _{ILP}	V _{PP}

Mode	Pin Function ⁽¹⁰⁾								
	Read or Output Disable	A ₀	MODE	DCLK	PCLK	SDI	SDO	\bar{E} , \bar{E}_S , I	O ₇ - O ₀
	Other	A ₀	PGM	DCLK	PCLK	NA	\bar{V}_{FY}	V _{PP}	D ₇ - D ₀
Read		A ₀	V _{IL}	X	V _{IL} /V _{IH}	X	SDO	V _{IL}	O ₇ - O ₀
Load SR to PR		A ₀	V _{IH}	V _{IL}	V _{IL} /V _{IH}	X	SDI	X	O ₇ - O ₀
Load Output to SR		A ₀	V _{IH}	V _{IH} /V _{IH}	V _{IL}	V _{IL}	SDI	V _{IH}	O ₇ - O ₀
Shift SR		A ₀	V _{IH}	V _{IL} /V _{IH}	V _{IL}	D _{IN}	SDO	X	O ₇ - O ₀
Asynchronous Enable Read		A ₀	V _{IL}	V _{IL}	X	V _{IL}	SDO	V _{IL}	O ₇ - O ₀
Synchronous Enable Read		A ₀	V _{IL}	V _{IL}	V _{IL} /V _{IH}	V _{IL}	SDO	V _{IL}	O ₇ - O ₀
Asynchronous Initialization Read		A ₀	V _{IL}	V _{IL}	X	V _{IL}	SDO	V _{IL}	O ₇ - O ₀
Program Memory		A ₀	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Verify		A ₀	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{PP}	O ₇ - O ₀
Program Inhibit		A ₀	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	High Z
Program Synchronous Enable		V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Initial Byte		V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ - D ₀



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Table 2. CY7C269 Mode Selection

Mode	Pin Function ⁽¹⁰⁾								
	Read or Output Disable	A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
	Other	A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Load SR to PR		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Load Output to SR		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Shift SR		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Asynchronous Enable Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Synchronous Enable Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Asynchronous Initialization Read		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Memory		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Verify		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Inhibit		A ₁₂	A ₁₁	A ₁₀ - A ₇	A ₆	A ₅	A ₄ - A ₃	A ₂	A ₁
Program Synchronous Enable		V _{IHP}	V _{IHP}	A ₁₀ - A ₇	V _{IHP}	V _{PP}	A ₄ - A ₃	V _{IHP}	V _{PP}
Program Initialize		V _{ILP}	V _{IHP}	A ₁₀ - A ₇	V _{IHP}	V _{PP}	A ₄ - A ₃	V _{ILP}	V _{PP}
Program Initial Byte		A ₁₂	V _{ILP}	A ₁₀ - A ₇	V _{IHP}	V _{PP}	A ₄ - A ₃	V _{ILP}	V _{PP}

PROMS

Mode	Pin Function ⁽¹⁰⁾							
	Read or Output Disable	A ₀	MODE	CLK	SDI	SDO	\bar{E}, \bar{I}	O ₇ - O ₀
	Other	A ₀	PGM	CLK	NA	$\bar{V}FY$	V _{PP}	D ₇ - D ₀
Read		A ₀	V _{IL}	V _{IL} /V _{IH}	X	High Z	V _{IL}	O ₇ - O ₀
Load SR to PR		A ₀	V _{IH}	V _{IL} /V _{IH}	V _{IL}	SDI	V _{IL}	O ₇ - O ₀
Load Output to SR		A ₀	V _{IH}	V _{IL} /V _{IH}	V _{IH}	SDI	V _{IL}	O ₇ - O ₀
Shift SR		A ₀	V _{IH}	V _{IL} /V _{IH}	D _{IN}	SDO	V _{IH}	O ₇ - O ₀
Asynchronous Enable Read		A ₀	V _{IL}	V _{IL}	X	High Z	V _{IL}	O ₇ - O ₀
Synchronous Enable Read		A ₀	V _{IL}	V _{IL} /V _{IH}	X	High Z	V _{IL}	O ₇ - O ₀
Asynchronous Initialization Read		A ₀	V _{IL}	V _{IL}	X	High Z	V _{IL}	O ₇ - O ₀
Program Memory		A ₀	V _{ILP}	V _{ILP}	X	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Verify		A ₀	V _{IHP}	V _{ILP}	X	V _{ILP}	V _{PP}	O ₇ - O ₀
Program Inhibit		A ₀	V _{IHP}	V _{ILP}	X	V _{IHP}	V _{PP}	High Z
Program Synchronous Enable		V _{ILP}	V _{ILP}	V _{ILP}	X	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Initialize		V _{ILP}	V _{ILP}	V _{ILP}	X	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Initial Byte		V _{IHP}	V _{ILP}	V _{ILP}	X	V _{IHP}	V _{PP}	D ₇ - D ₀

Note:
10. X = "don't care" but not to exceed V_{CC} ±5%.

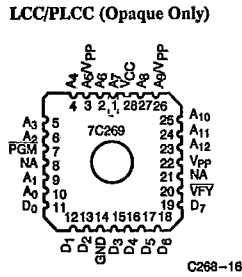
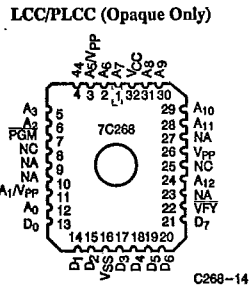
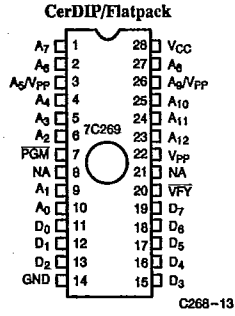
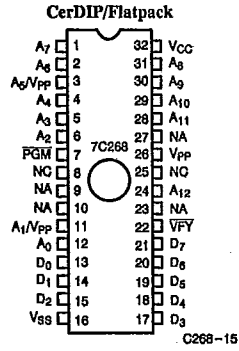
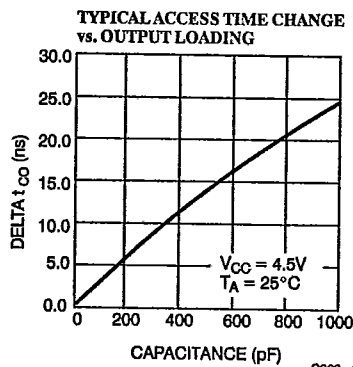
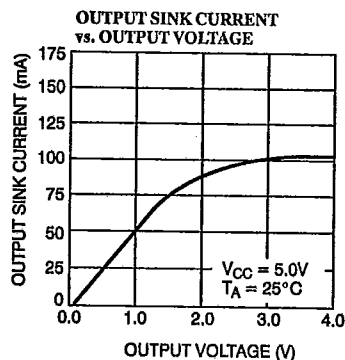
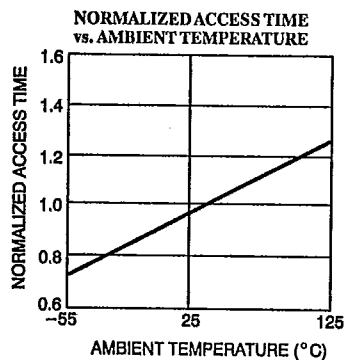
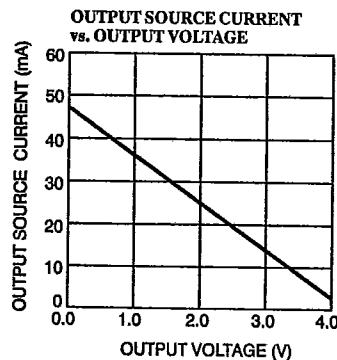
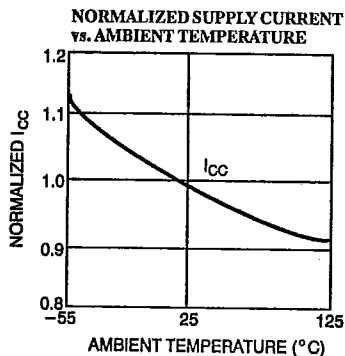
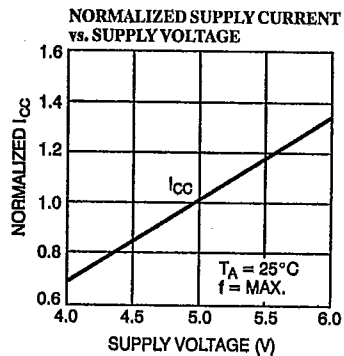


Figure 1. Programming Pinouts



Typical DC and AC Characteristics



C268-17



T-46-13-29

Ordering Information^[1]

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Type	Operating Range
40	100	CY7C268-40DC	D20	Commercial
		CY7C268-40WC	W20	
50	80	CY7C268-50DC	D20	Commercial
		CY7C268-50WC	W20	
	120	CY7C268-50DMB	D20	Military
		CY7C268-50LMB	L55	
		CY7C268-50QMB	Q55	
60	80	CY7C268-60DC	D20	Commercial
		CY7C268-60WC	W20	
	100	CY7C268-60DMB	D20	Military
		CY7C268-60LMB	L55	
		CY7C268-60QMB	Q55	
		CY7C268-60WMB	W20	

Notes:

11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Type	Operating Range
15	120	CY7C269-15DC	D22	Commercial
		CY7C269-15PC	P21	
		CY7C269-15WC	W22	
18	120	CY7C269-18DC	D22	Commercial
		CY7C269-18PC	P21	
		CY7C269-18WC	W22	
	140	CY7C269-18DMB	D22	Military
		CY7C269-18LMB	L64	
		CY7C269-18QMB	Q64	
25	140	CY7C269-25DC	D22	Commercial
		CY7C269-25LC	L64	
		CY7C269-25PC	P21	
		CY7C269-25QC	Q64	
		CY7C269-25WC	W22	
		CY7C269-25DMB	D22	
	CY7C269-25LMB	L64		
	CY7C269-25QMB	Q64		
	CY7C269-25WMB	W22		
	40	100	CY7C269-40DC	D22
CY7C269-40PC			P21	
CY7C269-40WC			W22	
50	80	CY7C269-50DC	D22	Commercial
		CY7C269-50PC	P21	
		CY7C269-50WC	W22	
	120	CY7C269-50DMB	D22	Military
		CY7C269-50LMB	L64	
		CY7C269-50QMB	Q64	
60	80	CY7C269-60DC	D22	Commercial
		CY7C269-60PC	P21	
		CY7C269-60WC	W22	
	100	CY7C269-60DMB	D22	Military
		CY7C269-60LMB	L64	
		CY7C269-60QMB	Q64	
		C7C269Y-60WMB	W22	



CY7C268
CY7C269

MILITARY SPECIFICATIONS
Group A Subgroup Testing

T-46-13-29

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3



PROMS

Switching Characteristics

Parameters	Subgroups
t _{AS}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11
t _{PW}	7, 8, 9, 10, 11
t _{SES}	7, 8, 9, 10, 11
t _{HES}	7, 8, 9, 10, 11
t _{COS}	7, 8, 9, 10, 11

Diagnostic Mode Switching Characteristics

Parameters	Subgroups
t _{SSDI}	7, 8, 9, 10, 11
t _{HSDI}	7, 8, 9, 10, 11
t _{SDSO}	7, 8, 9, 10, 11
t _{DCL}	7, 8, 9, 10, 11
t _{DCH}	7, 8, 9, 10, 11
t _{HM} ^[12]	7, 8, 9, 10, 11
t _{MS}	7, 8, 9, 10, 11
t _{SS}	7, 8, 9, 10, 11

Notes:

12. 7C269 only.

Document #: 38-00069-C