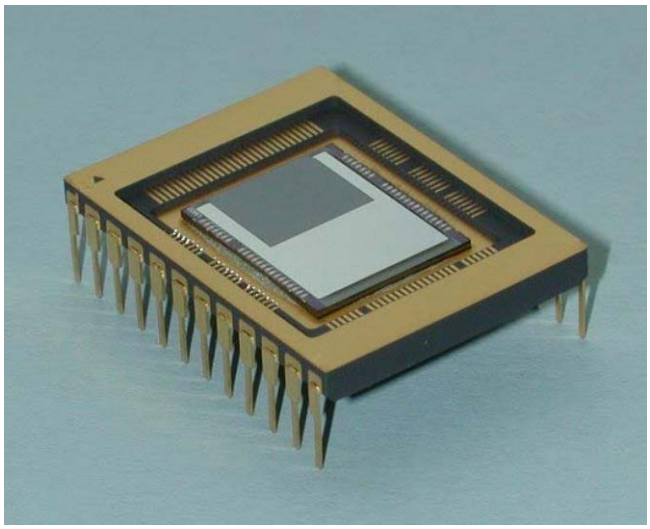
CCD67 NIMO Back Illuminated High Performance CCD Sensor

FEATURES

- 256 by 256 pixel format
- 26 µm square pixels
- Back Illuminated format for high quantum efficiency
- Frame transfer operation
- Low noise, high responsivity output amplifier
- Gated dump drain on output register
- 100% active area



INTRODUCTION

This version of the CCD67 family of CCD sensors is a frame transfer imaging device with a single serial output register.

There are two low noise amplifiers in the readout register, one at each end. Charge can be made to transfer through either or both of the amplifiers by making the appropriate RØ1 connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

The register is designed to accommodate 3 image pixels of charge.

The CCD67 is pin compatible with the CCD57 and the centre of the image area of the CCD67 is coincident with that of the CCD57.

Other variants of the CCD67 available are front illuminated format and inverted mode. Designers are advised to contact e2v technologies should they be considering the use of CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE

Pixel readout frequency	45 kHz
Output amplifier responsivity	1.5 µV/e^-
Peak signal	600 ke^-/pixel
Spectral range	200–1060 nm
Readout noise @ 18 kHz	4 e^- rms

GENERAL DATA

Format

Image area	268 (H) x 264 (V)
Active pixels	256 (H) x 256 (V)
Pixel size	26 x 26 µm
Number of output amplifiers	2
Number of underscan (serial) pixels	6 (each end)

Package

Package size	30.0 x 22.6 mm
Number of pins	32
Inter-pin spacing	2.54 mm
Window material	Removable glass
Package type	Ceramic DIL array

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PERFORMANCE

		Min	Typical	Max	Units	Note
Peak charge storage			600,000		e^-/pixel	1
Dynamic range			150,000:1			4
Dark signal at 293 K (equivalent at 243 K)			85,000 (550)	170,000 (1100)	e^-/pixel/s	2, 3, 8
Charge transfer efficiency	Parallel		>99.999	-	%	5
	Serial		>99.999	-	%	
Output amplifier responsivity		1.0	1.5	2.0	µV/e^-	3
Readout noise at 243K (18 kHz)			4	6	rms e^-/pixel	3, 6
Readout frequency			45	5000	KHz	7
Dark signal non-uniformity at 293 K (std. deviation)			8500	17000	e^-/pixel/s	3, 8

NOTES

1. Signal level at which resolution begins to degrade. The typical values are those expected from design.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K may be estimated from:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

   where Q □d0□ is the dark signal at 293 K.
3. Test carried out at e2v technologies on all sensors at 243 K.
4. Dynamic range is the ratio of full-well capacity to readout noise. Not measured.
5. CCD characterisation made using charge generated by X-ray photons of known energy. Not measured.
6. Measured at a pixel readout frequency of 18 KHz using a dual-slope integrator technique (i.e. correlated double sampling). All other tests measured at 45 KHz.
7. Readout above 5 MHz can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured at 243K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 8 times the specified maximum dark signal generation rate The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

Column defects A column which contains at least 9 white or 9 black defects.

GRADE	0	1	2
Column defects;			
black	0	2	8
white	0	0	1
Black spots	10	20	40
Traps >200 e^-	1	2	5
White spots	10	20	30

Grade 5 Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

SPECTRAL RESPONSE AT 243 K

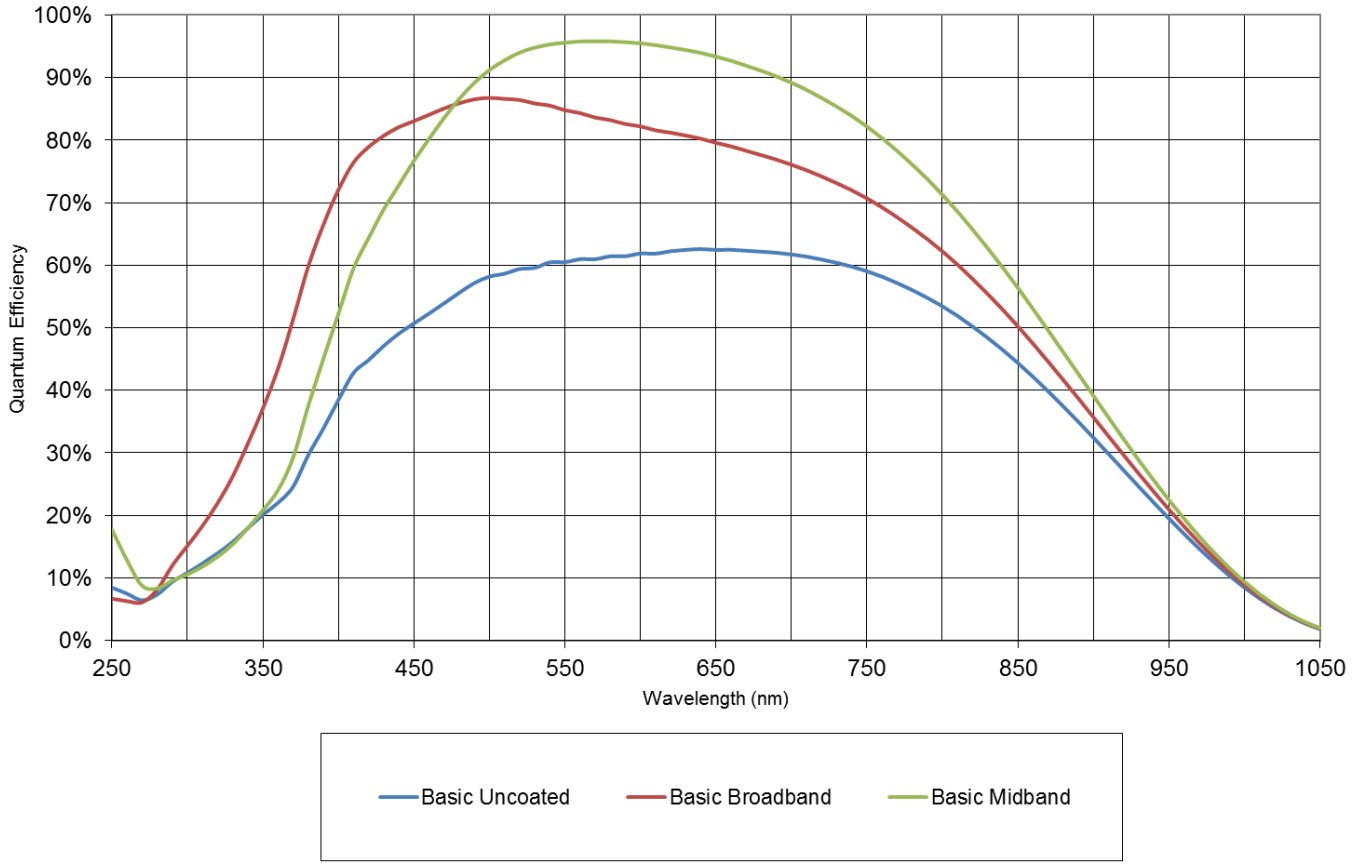
Standard Silicon

Wavelength (nm)	Minimum Response (QE) (see note 9)			Maximum Response Non-uniformity (1σ)	
	Basic Process Mid-band Coated	Basic Process Broadband Coated	Basic Process Uncoated		
300	-	-	-	-	%
350	15	25	10	5	%
400	40	55	25	3	%
500	85	75	55	3	%
650	85	75	50	3	%
900	30	30	30	5	%

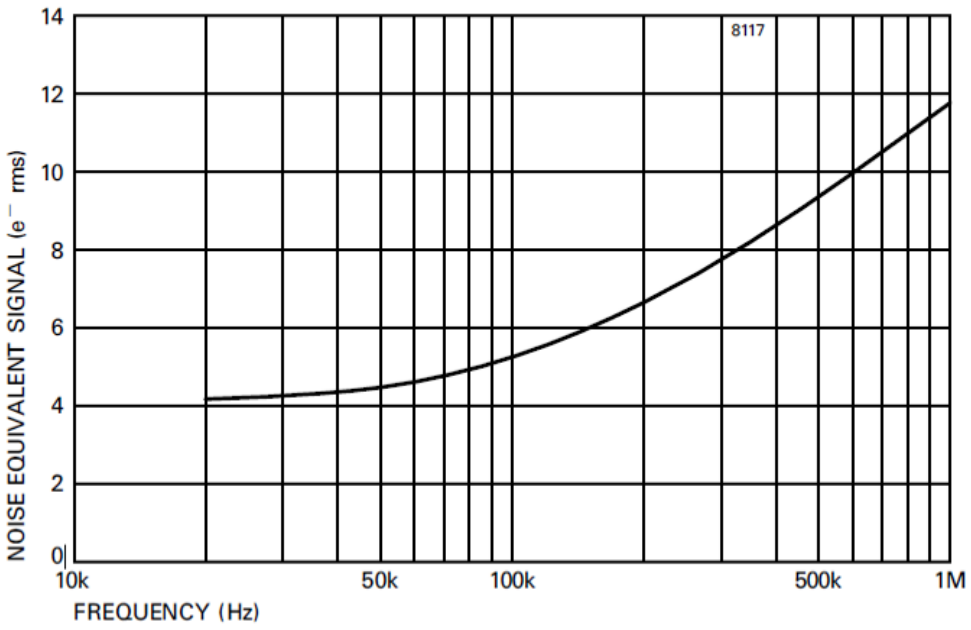
Notes

9. The uncoated process, that may be suitable for soft X-ray and EUV applications, would be supplied without the storeshield.

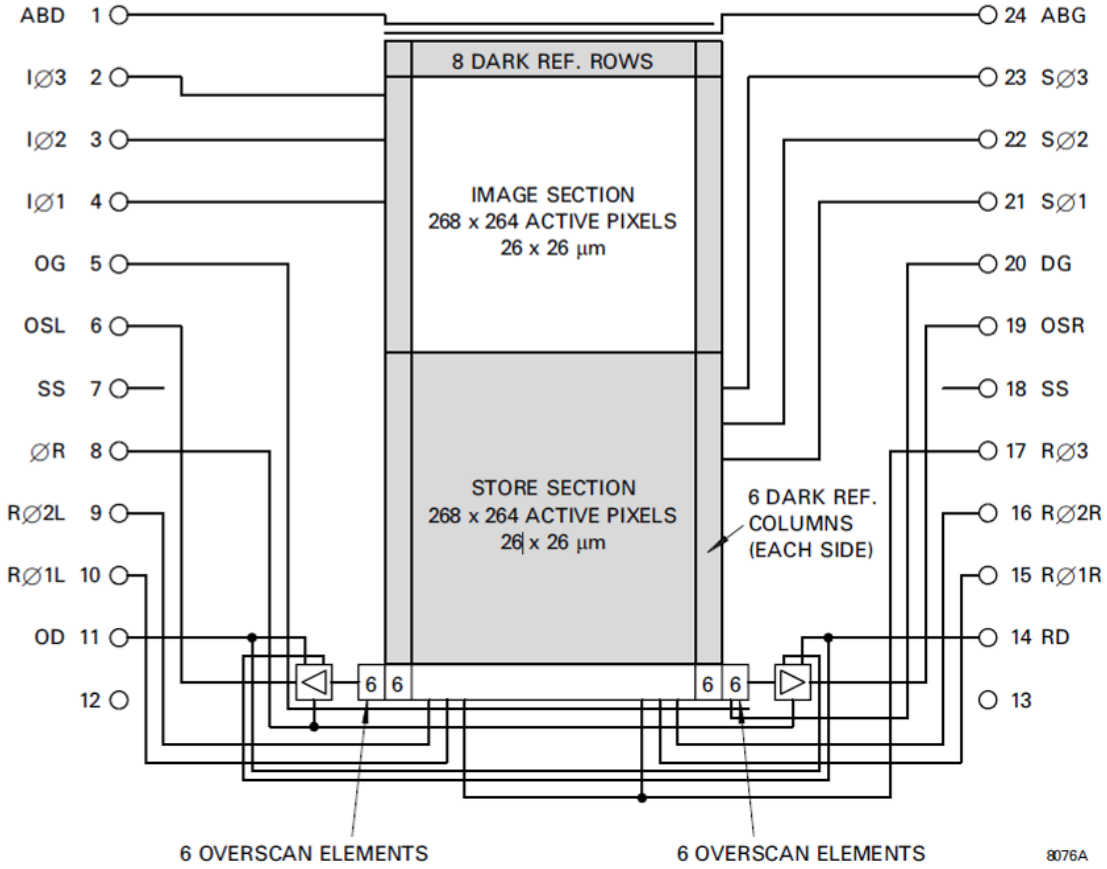
TYPICAL SPECTRAL RESPONSE (At –30 °C)



TYPICAL OUTPUT CIRCUIT NOISE (If Measured using clamp and sample)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

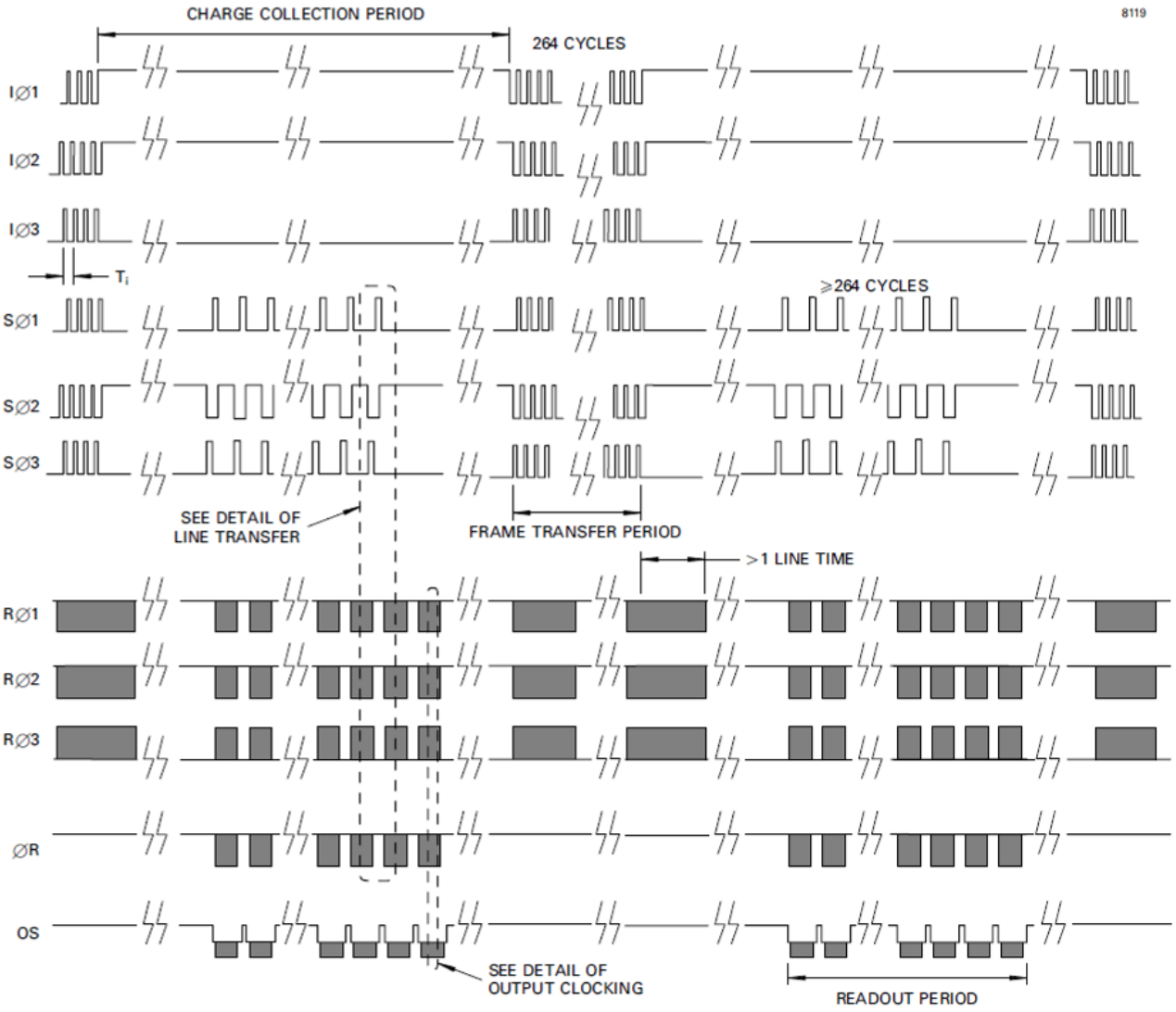
PIN	REF	DESCRIPTION	CLOCK LOW Typical	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
				Min	Typical	Max	
1	ABD	Anti-blooming drain (see note 10)	n/a		V_{OD}		−0.3 to +32 V
2	I∅3	Image area clock, phase 3	0	8	12	15	±20 V
3	I∅2	Image area clock, phase 2	0	8	12	15	±20 V
4	I∅1	Image area clock, phase 1	0	8	12	15	±20 V
5	OG	Output gate	n/a	1	3	5	±20 V
6	OSL	Output transistor source (left)	n/a		see note 11		−0.3 to +25 V
7	SS	Substrate	n/a	0	0	10	-
8	∅R	Reset pulse	0	8	12	15	±20 V
9	R∅2L	Register clock phase 2 (left)	1	8	11	15	±20 V
10	R∅1L	Register clock phase 1 (left)	1	8	11	15	±20 V
11	OD	Output drain	n/a	27	29	31	−0.3 to +32 V
12	-	No connection	n/a		-		-
13	-	No connection	n/a		-		-
14	RD	Reset drain	n/a	15	17	19	−0.3 to +25 V
15	R∅1R	Register clock phase 1 (right)	1	8	11	15	±20 V
16	R∅2R	Register clock phase 2 (right)	1	8	11	15	±20 V
17	R∅3	Register clock phase 3	1	8	11	15	±20 V
18	SS	Substrate	n/a	0	0	10	-
19	OSR	Output transistor source (right)	n/a		see note 11		−0.3 to +25 V
20	DG	Dump gate (see note 12)	0	10	12	14	±20 V
21	S∅1	Storage area clock, phase 1	0	8	12	15	±20 V
22	S∅2	Storage area clock, phase 2	0	8	12	15	±20 V
23	S∅3	Storage area clock, phase 3	0	8	12	15	±20 V
24	ABG	Anti-blooming gate (see note 10)	n/a	0	3	5	±20 V

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance. Refer to the specific device test data if possible.

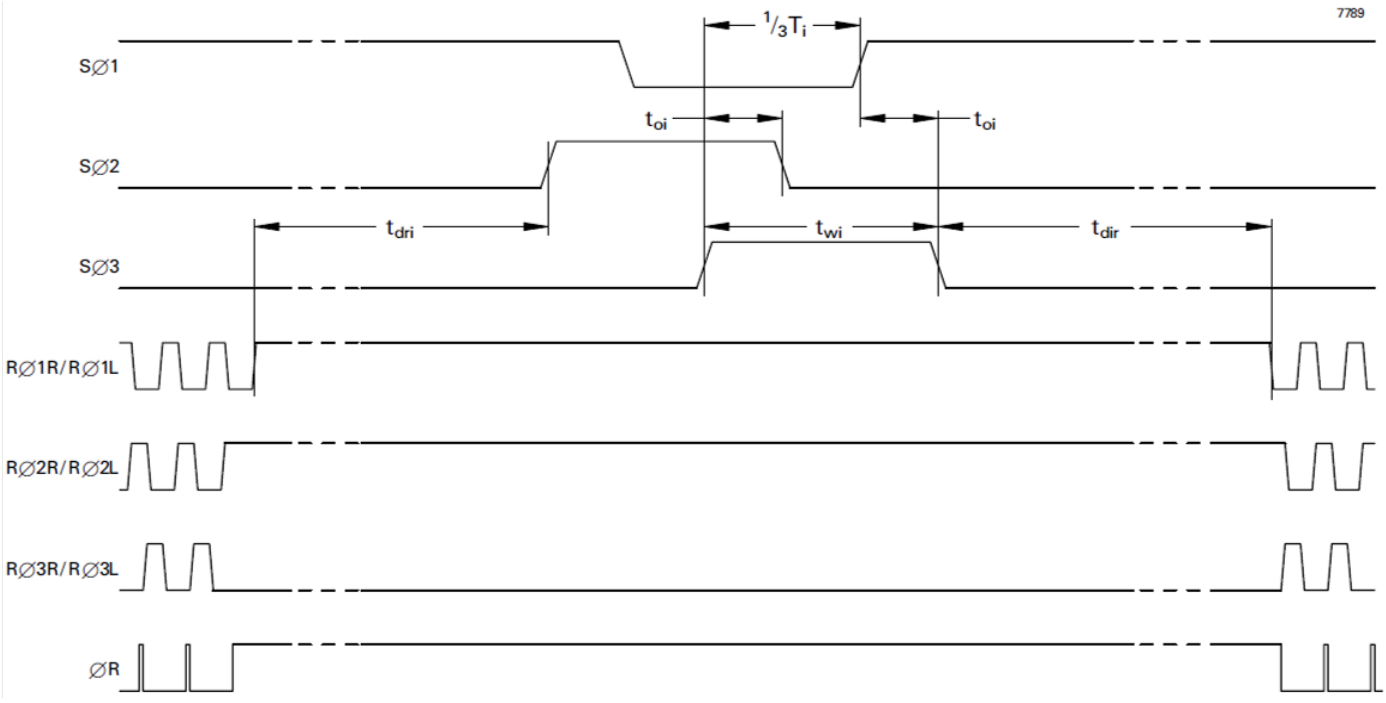
NOTES

10. Although anti-blooming is not incorporated, bias is still necessary.
11. Not critical; OS = 3 to 5 V below OD typically. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
12. This gate is normally low. It should be pulsed high for charge dump.

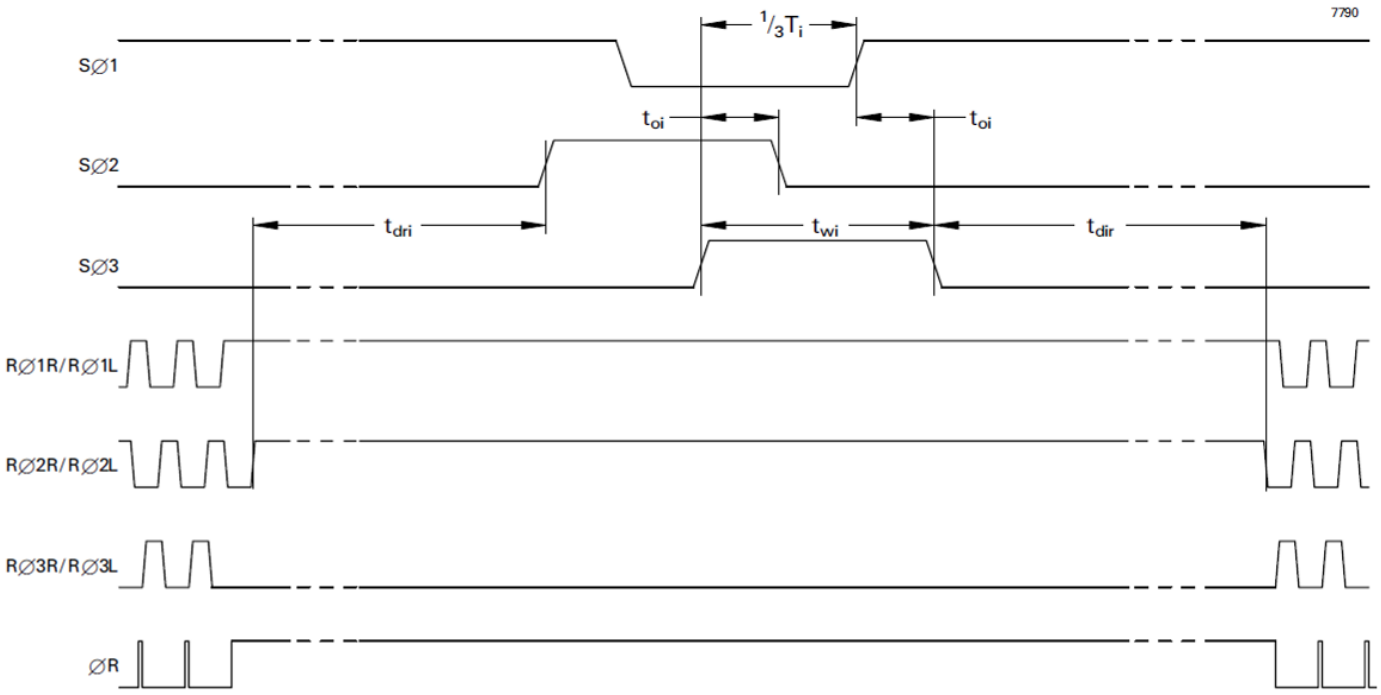
FRAME TRANSFER TIMING DIAGRAM



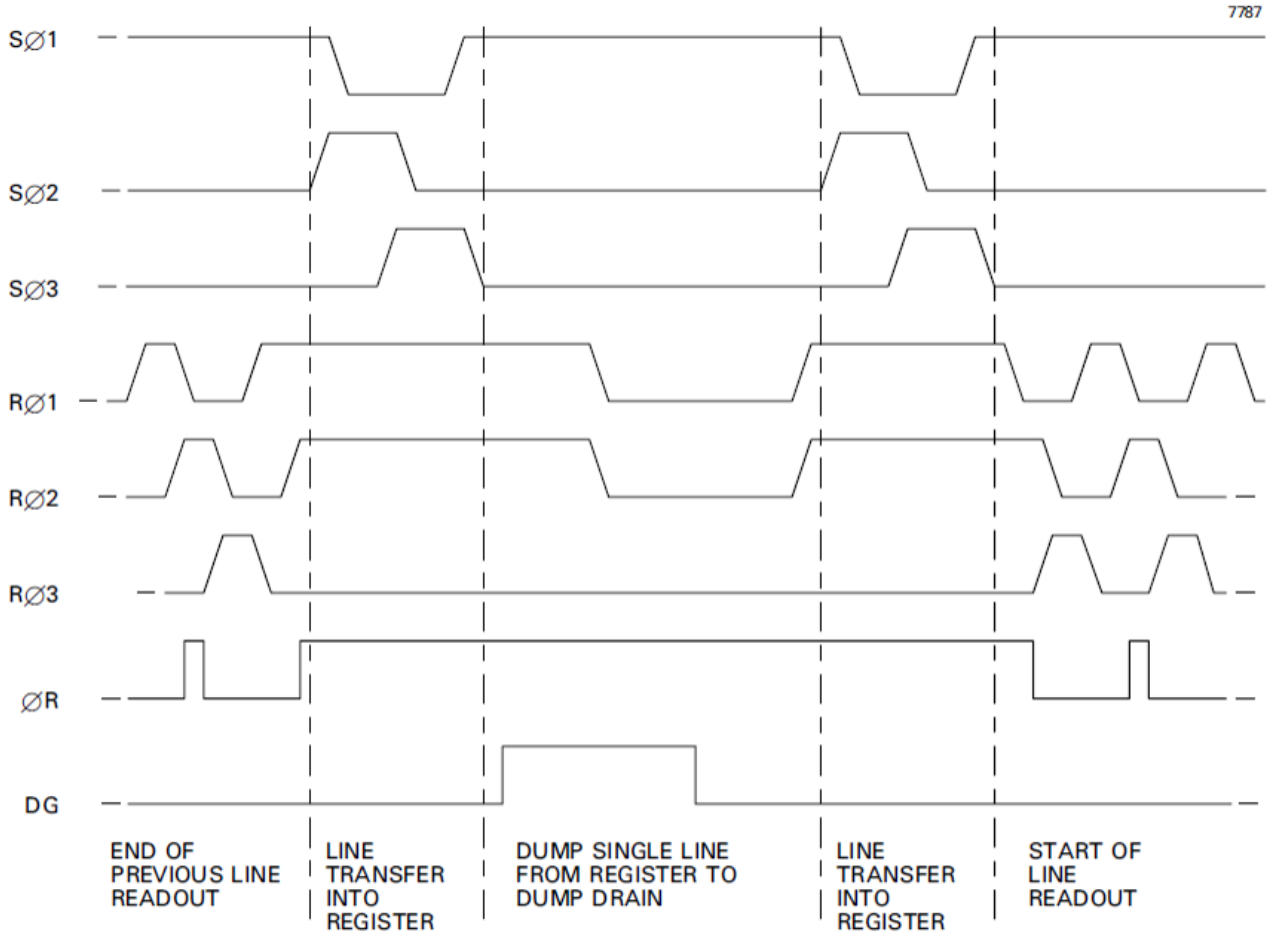
DETAIL OF LINE TRANSFER (For output from the right-hand amplifier)



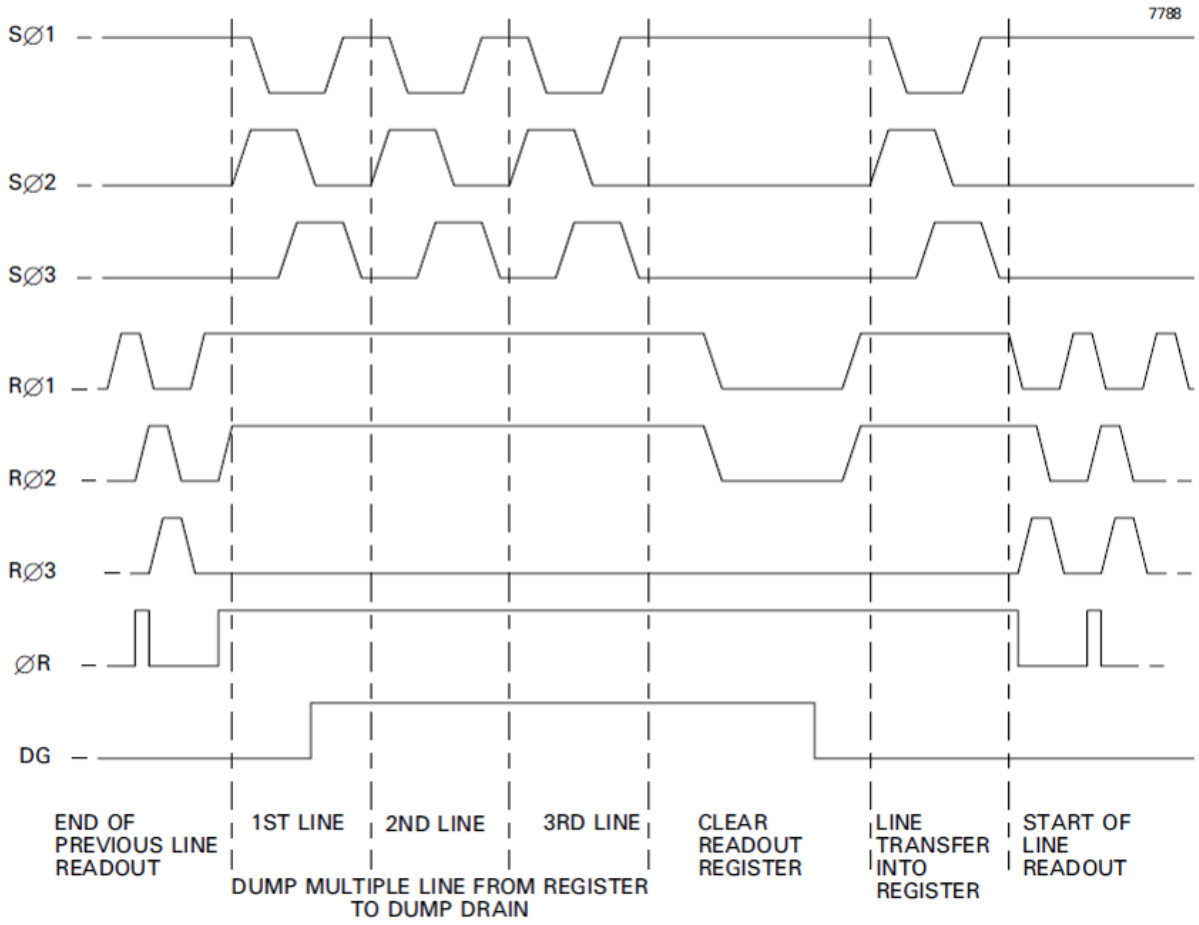
DETAIL OF LINE TRANSFER (For output from the left-hand amplifier)



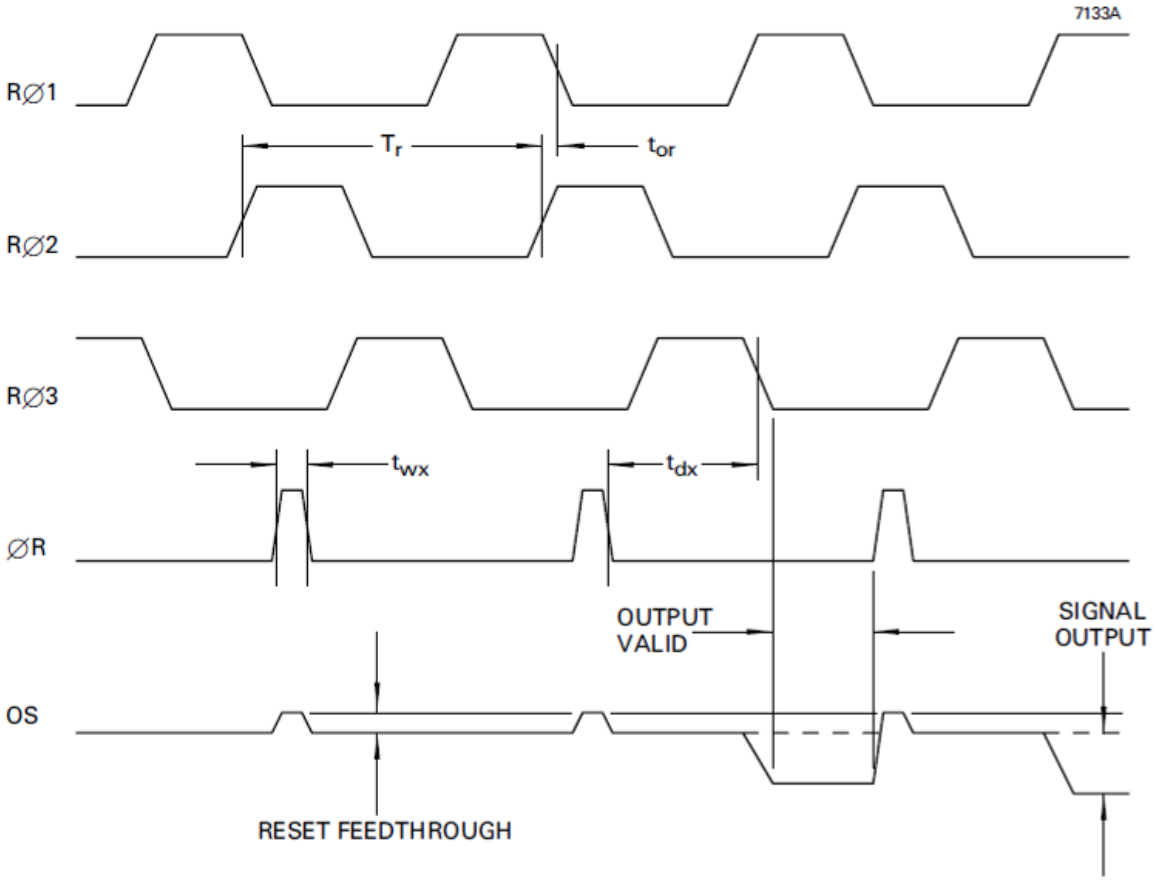
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



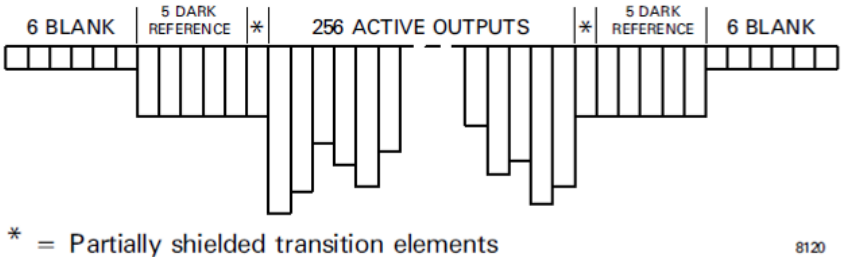
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING (Output from right-hand amplifier)



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

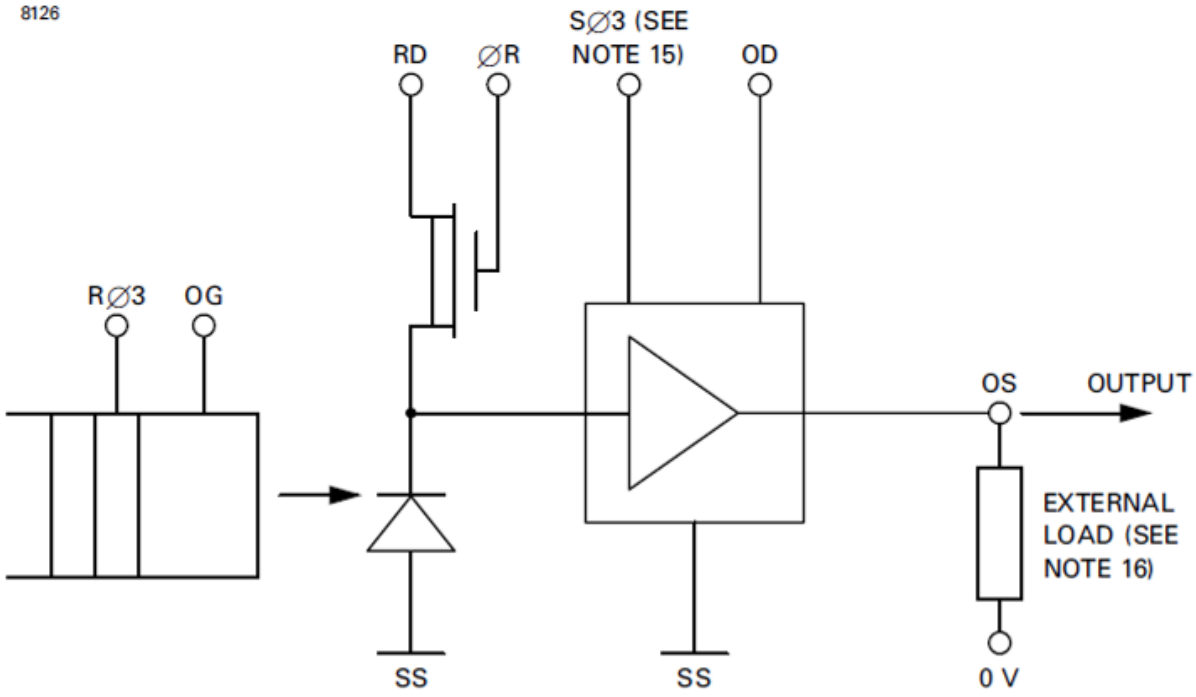
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	0.5	1	see note 13	µs
t_{wi}	Image clock pulse width	0.25	0.5	see note 13	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.03	0.1	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	0.1	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi})/2$	0.1	$0.2T_i$	µs
t_{dir}	Delay time, S∅ stop to R∅ start	1	2	see note 13	µs
t_{dri}	Delay time, R∅ stop to S∅ start	1	1	see note 13	µs
T_r	Output register clock cycle period	125	500	see note 13	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2\ t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

13. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

14. To minimise dark current, two of the IØ clocks should be held low during integration. IØ timing requirements are identical to SØ (as shown above).

OUTPUT CIRCUIT (Right-hand amplifier)



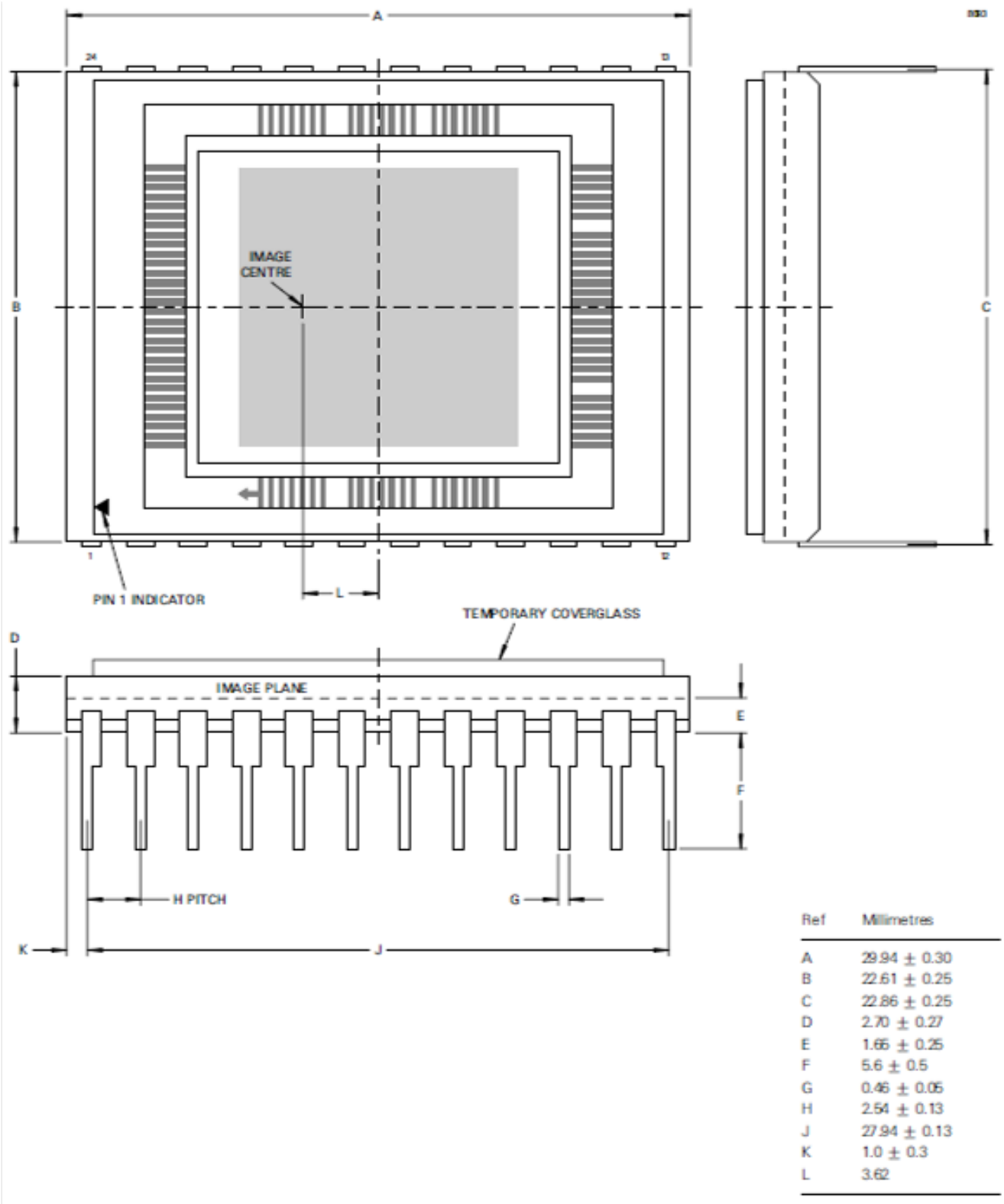
NOTES

15. The amplifier has a DC restoration circuit which is internally activated whenever S∅3 is high.

16. External load not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

OUTLINES (All dimensions in millimetres; dimensions without limits are nominal)

Standard Ceramic Package



Ref	Millimetres
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3
L	3.62

ORDERING INFORMATION

Options include:

- Temporary quartz window
- Temporary glass window
- Fibre-optic coupling
- UV coating
- X-ray phosphor coating

For further information on the performance of these and other options, contact e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating	153	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling .....5 K/min