

### FEATURES

- 256 x 256 Pixel Image Area.
- 26  $\mu\text{m}$  Square Pixels.
- Low Noise, High Responsivity Output Amplifier.
- 100% Active Area.
- Gated Dump Drain on Output Register.

### INTRODUCTION

This version of the CCD67 family of CCD Sensors is a frame transfer imaging device with a single serial output register.

There are two low noise amplifiers in the readout register, one at each end. Charge can be made to transfer through either or both of the amplifiers by making the appropriate  $R\bar{O}$  connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

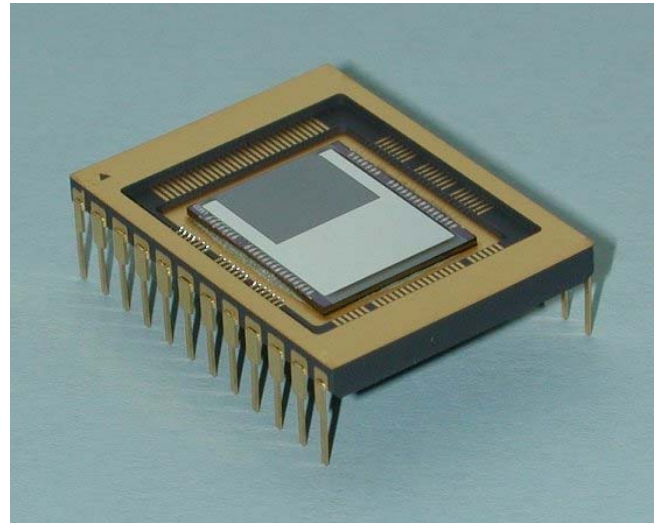
The register is designed to accommodate 3 image pixels of charge.

The CCD67 is pin compatible with the CCD57 and the centre of the image area of the CCD67 is coincident with that of the CCD57.

Other variants of the CCD67 are available for applications with differing requirements. Designers are advised to contact e2v technologies should they be considering the use of CCD sensors in abnormal environments or if they require customised packaging.

### TYPICAL PERFORMANCE

Maximum readout frequency . . . . .	5	MHz
Output responsivity . . . . .	1.5	$\mu\text{V}/\text{e}^-$
Peak signal . . . . .	450	$\text{ke}^-/\text{pixel}$
Spectral range . . . . .	400 - 1100	nm
Readout noise (1 MHz) . . . . .	12	$\text{e}^- \text{ rms}$



### GENERAL DATA

#### Format

Image area pixels . . . . .	268 (H) x 264 (V)
Active area pixels . . . . .	256 (H) x 256 (V)
Storage area pixels . . . . .	268 (H) x 264 (V)
Pixel size . . . . .	26 x 26 $\mu\text{m}$
Number of output amplifiers . . . . .	2
Number of underscan (serial) pixels . . . . .	6 (each end)

#### Package

Package size . . . . .	30.0 x 22.6 mm
Number of pins . . . . .	32
Inter-pin spacing . . . . .	2.54 mm
Window material . . . . .	temporary coverglass or 3 mm fibre-optic
Package type . . . . .	ceramic DIL array

## PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	300k	450k	-	e <sup>-</sup> /pixel
Peak output voltage (no binning)	-	0.9	-	V
Dark signal (see note 2)	-	200	500	e <sup>-</sup> /pixel/s
Dynamic range (see note 3)	-	112 500:1	-	
Charge transfer efficiency (see note 4):				
parallel	-	99.9999	-	%
serial	-	99.9993	-	%
Output amplifier responsivity	1.0	1.5	2.0	μV/e <sup>-</sup>
Readout noise at 233 K (20 kHz) (see note 5)	-	4.0	6.0	rms e <sup>-</sup>
Maximum readout frequency (see note 6)	-	-	5	MHz
Maximum vertical transfer frequency	-	-	2	MHz
Photo response non-uniformity (see note 7) (std. deviation)	-	3	5	% of mean
Dark signal non-uniformity (293 K) (see note 8)	-	50	150	e <sup>-</sup> /pixel/s

## NOTES

- Signal level at which resolution begins to degrade.
- Measured between 233 and 253 K and V<sub>SS</sub> +9.0 V. Dark signal at any temperature T (kelvin) may be estimated from:  

$$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$
 where Q<sub>d0</sub> is the dark signal at T = 293 K (20 °C).
- Dynamic range is the ratio of full-well capacity to readout noise measured at 233 K and 20 kHz readout speed.
- CCD characterisation measurements made using charge generated by X-ray photons of known energy.
- Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period.
- Readout at speeds in excess of 5 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
- This is not quoted for the fibre-optic variant as it is affected by the fibre-optic.
- Measured between 253 and 293 K, excluding white defects.

## BLEMISH SPECIFICATION

- Traps** Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e<sup>-</sup> at 233 K.
- Slipped columns** Are counted if they have an amplitude greater than 200 e<sup>-</sup>.
- Black spots** Are counted when they have a signal level of less than 90% of the local mean at a signal level of approximately half full-well.

**White spots** Are counted when they have a generation rate 10 times the specified maximum dark signal generation rate (measured between 253 and 293 K). The amplitude of white spots will vary in the same manner as dark current, i.e.:

$$Q_d/Q_{d0} = 122T^3 e^{-6400/T}$$

**White column** A column which contains at least 9 white defects.

**Black column** A column which contains at least 9 black defects.

GRADE	0	1	2
Column defects:			
black or slipped	0	1	4
white	0	0	0
Black spots	5	10	20
Traps > 200 e <sup>-</sup>	1	2	5
White spots	5	10	15

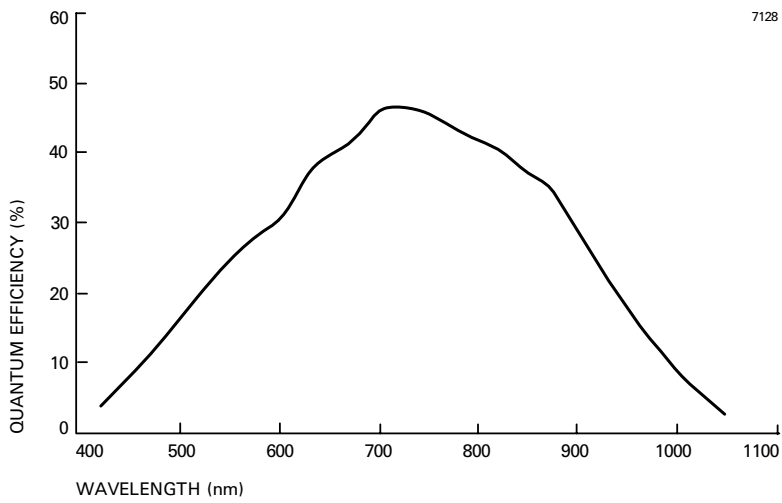
**Grade 5** Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters.

Minimum separation between adjacent black columns . . . . . 50 pixels

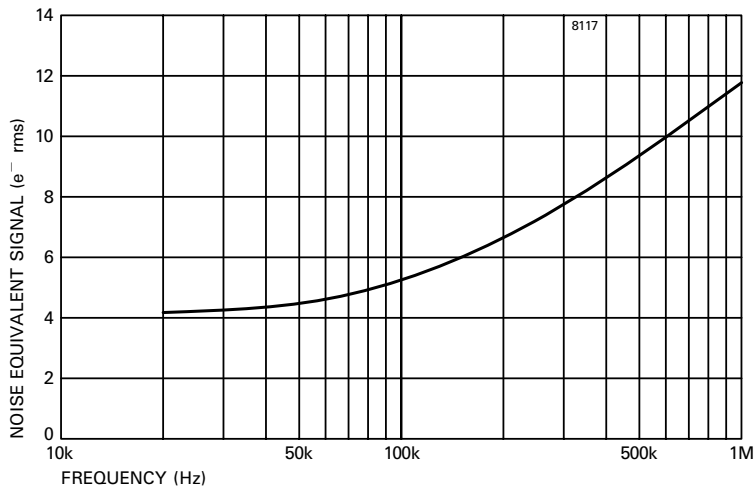
**Note** The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

## TYPICAL SPECTRAL RESPONSE

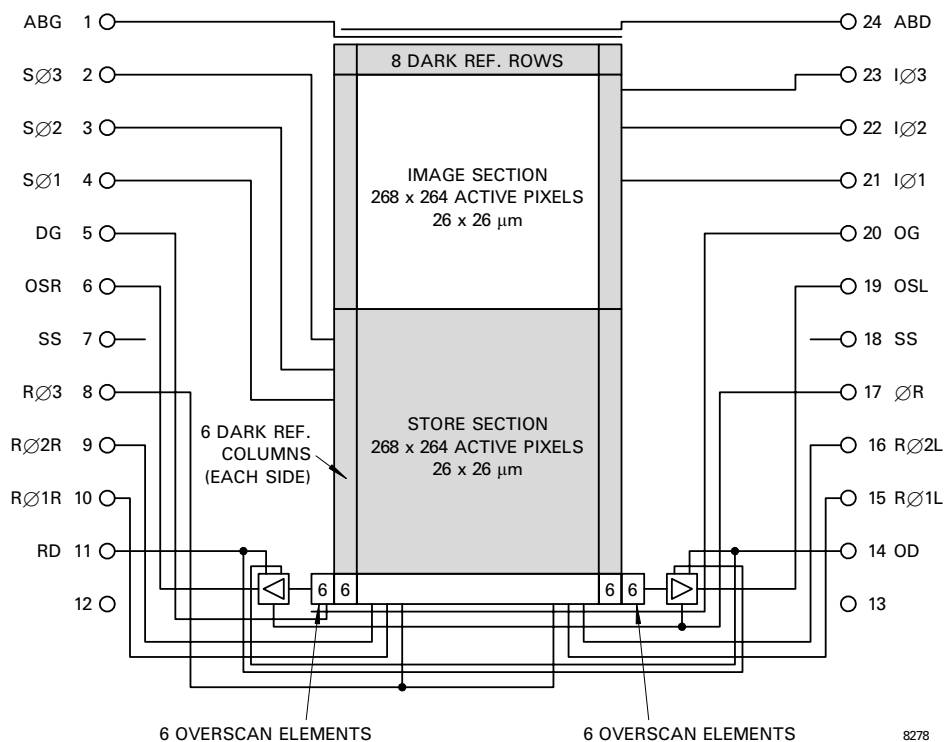
This graph is for a non-windowed or fibre-optic coupled device. A small deviation from the curve can be expected as a result of the coupling.



## TYPICAL OUTPUT NOISE



# DEVICE SCHEMATIC



8278

## CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

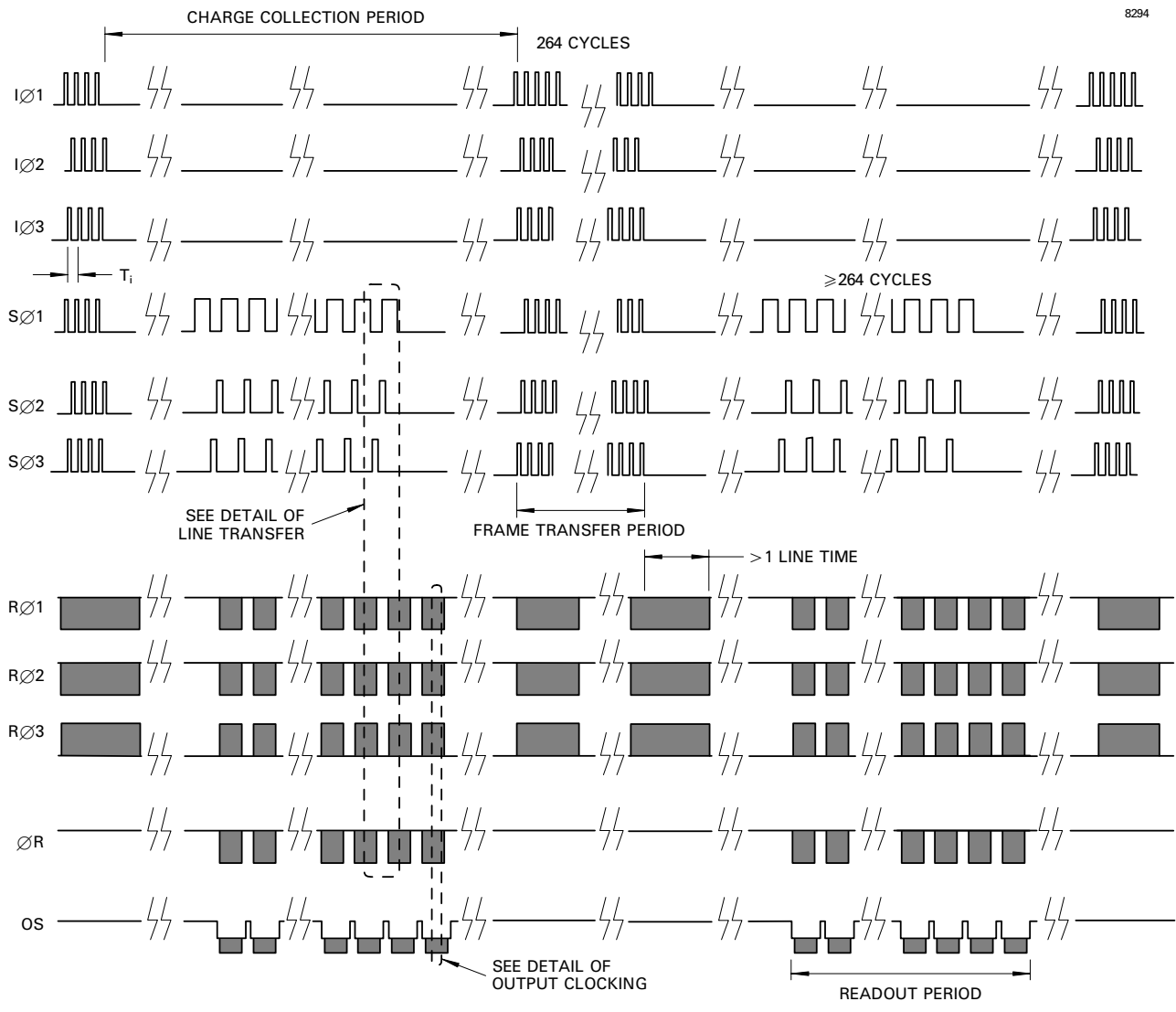
PIN	REF	DESCRIPTION	CLOCK LOW (V typ.)	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS w.r.t. V <sub>SS</sub>
				Min	Typical	Max	
1	ABG	Anti-blooming gate (see note 9)	n/a	0	3	5	±20 V
2	SØ3	Storage clock, phase 3	0	8	12	15	±20 V
3	SØ2	Storage clock, phase 2	0	8	12	15	±20 V
4	SØ1	Storage clock, phase 1	0	8	12	15	±20 V
5	DG	Dump gate (see note 10)	0	10	12	14	±20 V
6	OSR	Output transistor source (right amplifier)	n/a	see note 11			−0.3 to +25 V
7	SS	Substrate	n/a	0	9.5	11	-
8	RØ3	Register clock, phase 3	−2	8	10	15	±20 V
9	RØ2R	Register clock, phase 2 (right section)	−2	8	10	15	±20 V
10	RØ1R	Register clock, phase 1 (right section)	−2	8	10	15	±20 V
11	RD	Reset drain	n/a	15	18	21	−0.3 to +25 V
12	-	No connection	n/a	-			-
13	-	No connection	n/a	-			-
14	OD	Output drain	n/a	27	29	31	−0.3 to +25 V
15	RØ1L	Register clock, phase 1 (left section)	−2	8	10	15	±20 V
16	RØ2L	Register clock, phase 2 (left section)	−2	8	10	15	±20 V
17	ØR	Reset pulse	0	8	12	15	±20 V
18	SS	Substrate	n/a	0	9.5	11	-
19	OSL	Output transistor source (left amplifier)	n/a	see note 11			−0.3 to +25 V
20	OG	Output gate	n/a	1	3	5	±20 V
21	IØ1	Image area clock, phase 1	0	8	12	15	±20 V
22	IØ2	Image area clock, phase 2	0	8	12	15	±20 V
23	IØ3	Image area clock, phase 3	0	8	12	15	±20 V
24	ABD	Anti-blooming drain (see note 9)	n/a	V <sub>OD</sub>			−0.3 to +25 V

## NOTES

9. Although anti-blooming is not incorporated, bias is still necessary.
10. This gate is normally low. It should be pulsed high for charge dump.
11. 3 to 5 V below OD. Connect to ground using a 2 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).

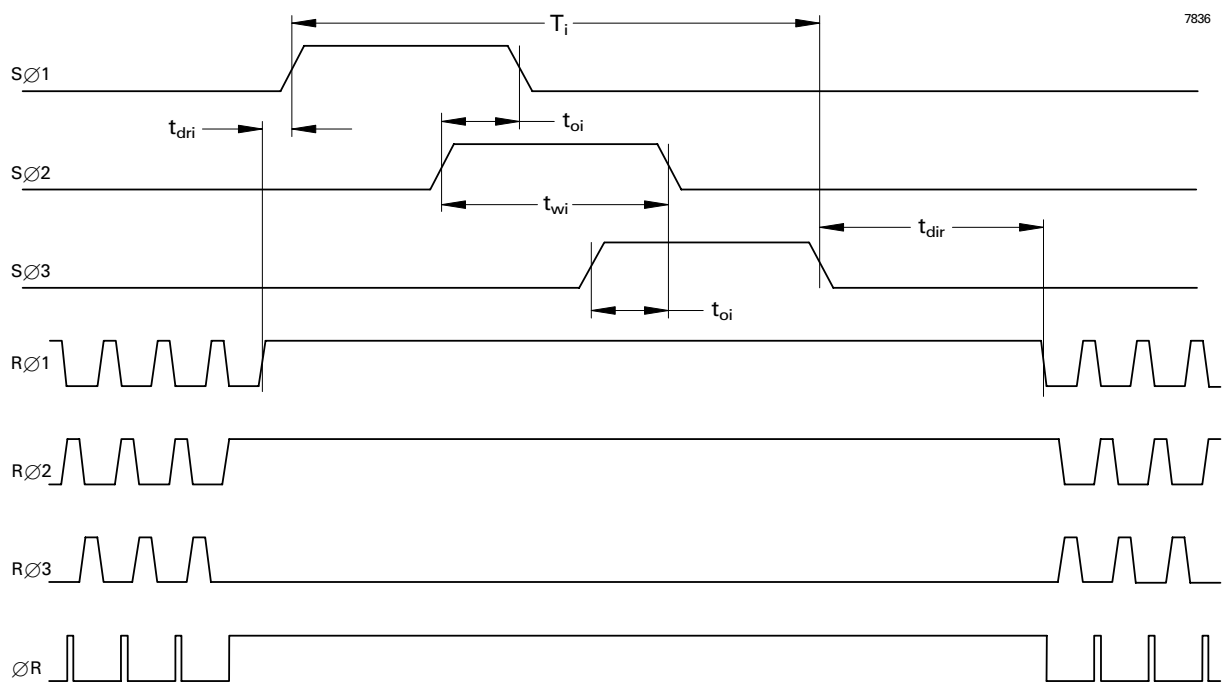
# FRAME TRANSFER TIMING DIAGRAM

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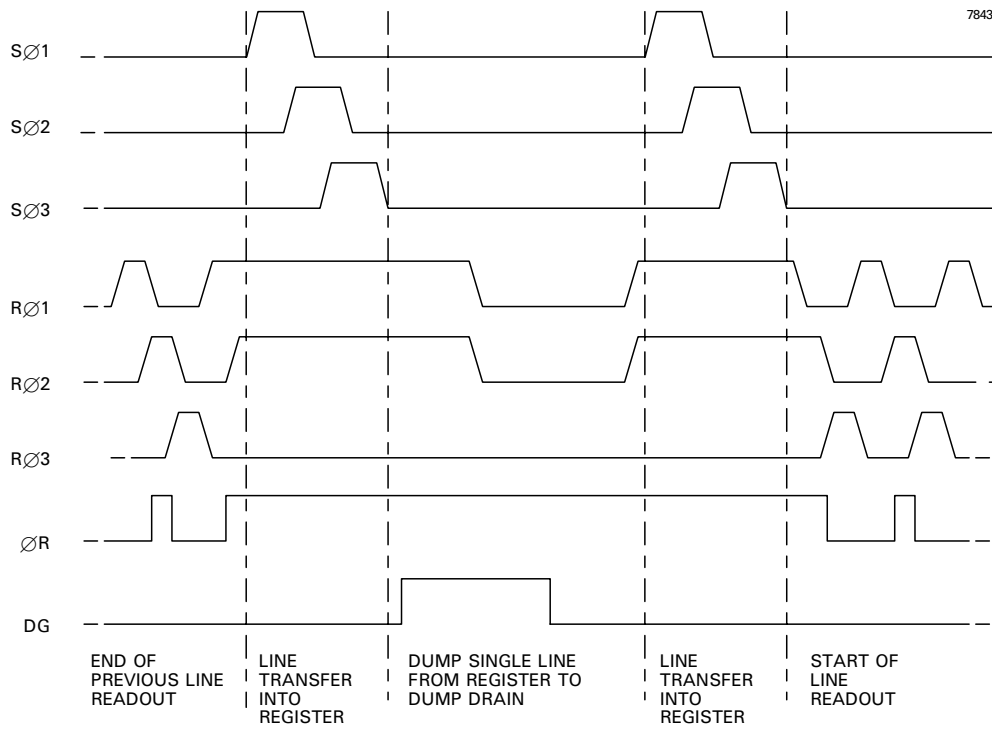


# DETAIL OF LINE TRANSFER

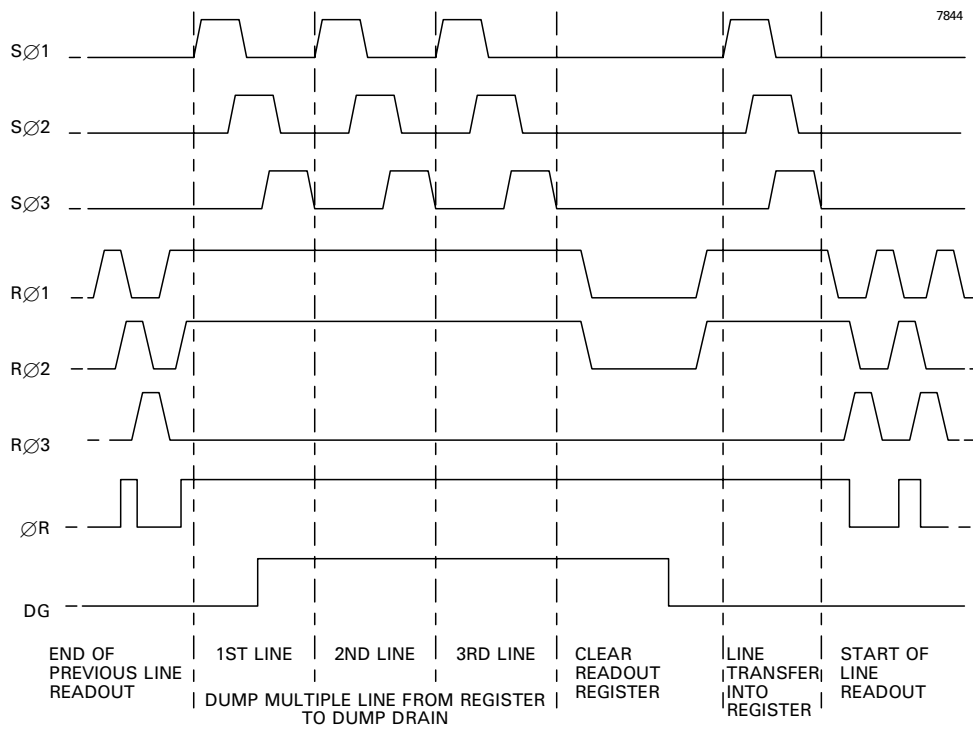
7836



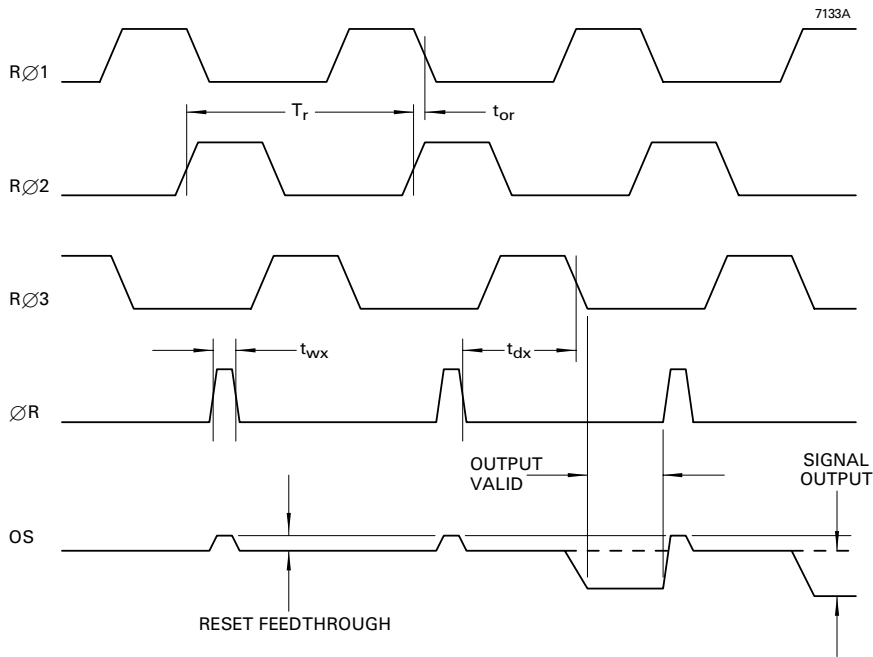
## DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



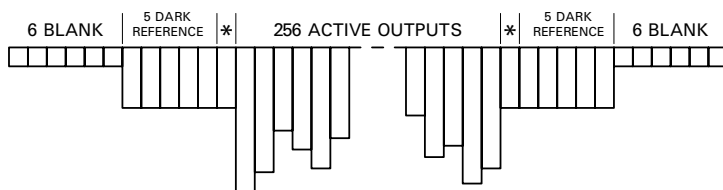
## DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



## DETAIL OF OUTPUT CLOCKING



## LINE OUTPUT FORMAT



\* = Partially shielded transition elements

8120

## CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
$T_{fi}$	First frame transfer pulse width	100	150	see note 12	$\mu s$
$T_{ti}$	Frame transfer clock period	2	5	see note 12	$\mu s$
$t_{w_{ti}}$	Frame transfer image clock pulse width	1	2	$T_{ti}/3 + t_{oi}$	$\mu s$
$T_i$	Store clock period	25	50	see note 12	$\mu s$
$t_{wi}$	Image/store clock pulse width	8	16	see note 12	$\mu s$
$t_{ri}$	Image/store clock pulse rise time (10 to 90%)	0.03	0.1	$0.2T_{ti}$	$\mu s$
$t_{fi}$	Image/store clock pulse fall time (10 to 90%)	$t_{ri}$	0.1	$0.2T_{ti}$	$\mu s$
$t_{oi}$	Image/store clock pulse overlap	0.2	0.3	$0.2T_{ti}$	$\mu s$
$t_{dir}$	Delay time, $S\emptyset$ stop to $R\emptyset$ start	1	2	see note 12	$\mu s$
$t_{dri}$	Delay time, $R\emptyset$ stop to $S\emptyset$ start	1	1	see note 12	$\mu s$
$T_r$	Output register clock cycle period	200	1000	see note 12	ns
$t_{rr}$	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
$t_{fr}$	Clock pulse fall time (10 to 90%)	$t_{rr}$	$0.1T_r$	$0.3T_r$	ns
$t_{or}$	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
$t_{wx}$	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
$t_{rx}, t_{fx}$	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
$t_{dx}$	Delay time, $\emptyset R$ low to $R\emptyset 3$ low	30	$0.5T_r$	$0.8T_r$	ns

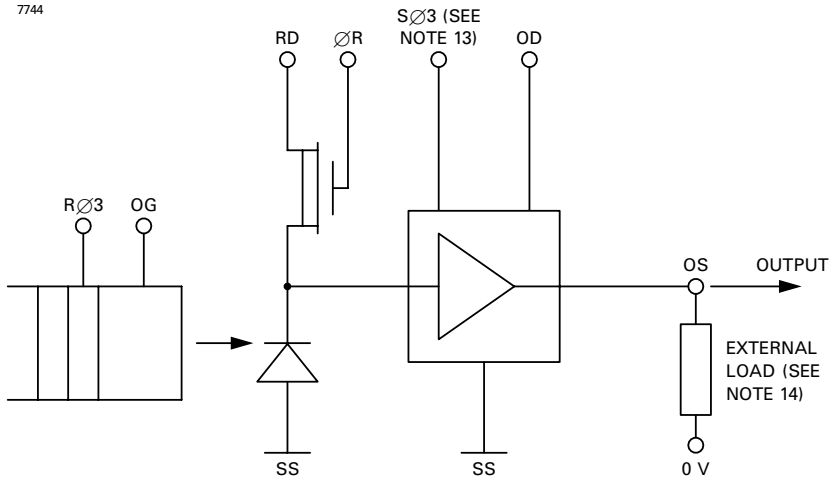
## NOTES

12. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.



## OUTPUT CIRCUIT (Right-hand amplifier)

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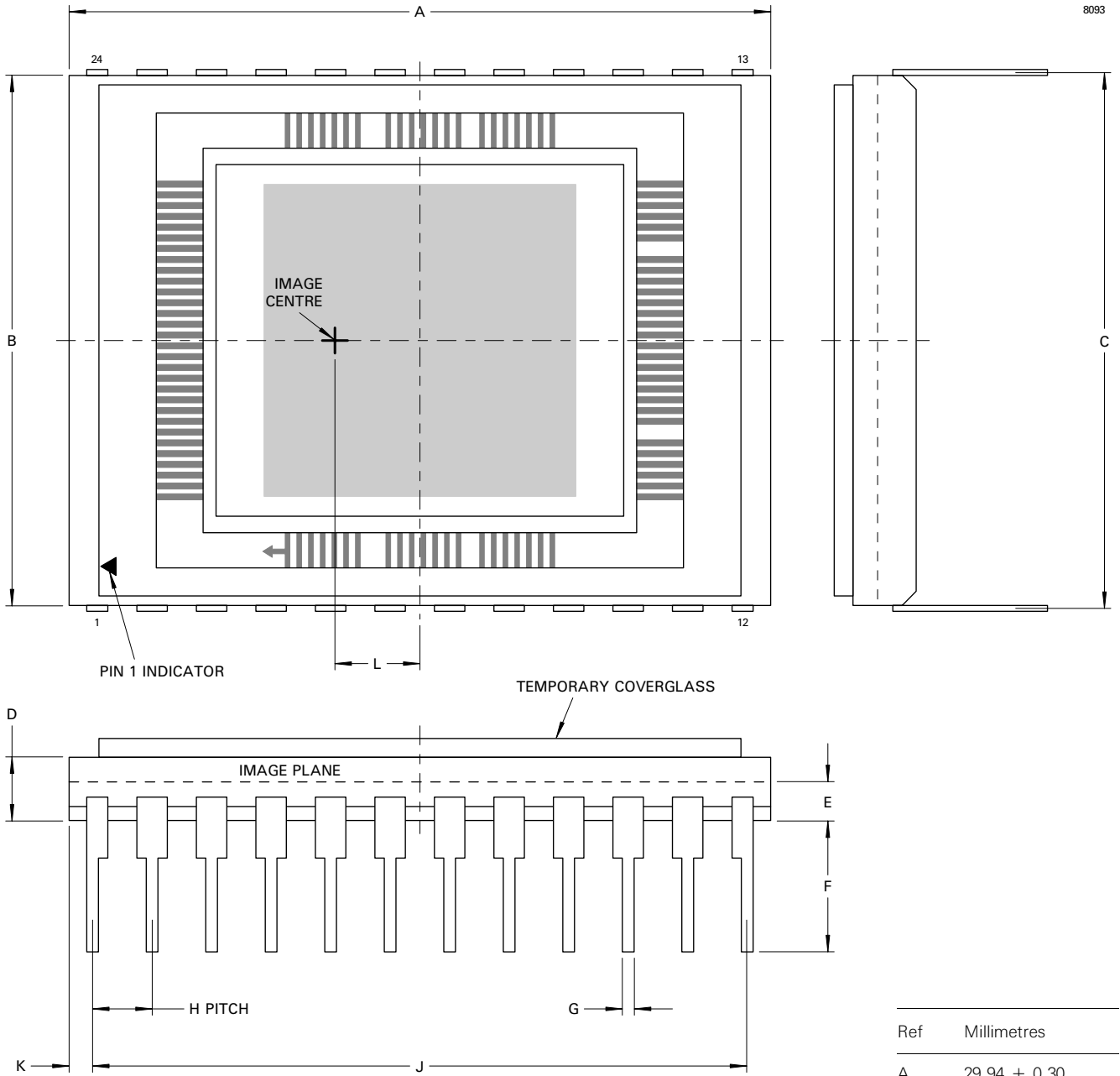


### NOTES

13. The amplifier has a DC restoration circuit which is internally activated whenever SØ3 is high.
14. Not critical; can be a 2 to 5 mA constant current supply or an appropriate load resistor.

# OUTLINE

(All dimensions without limits are nominal)



Ref	Millimetres
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3
L	3.62

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