FEATURES
- 1024 by 1024 1:1 Image Format
- Image Area 13.3 x 13.3 mm
- Frame Transfer Operation
- 13 µm Square Pixels
- Symmetrical Anti-static Gate Protection
- High Speed Output Amplifiers
- 100% Active Area
- Shielded Anti-bloom Pixel Structure

APPLICATIONS
- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION
This version of the CCD48-20 is a back-face illuminated, frame transfer CCD sensor with high performance, high speed output amplifiers. The image area contains a full 1024 by 1024 pixels which are 13 µm square. The output register is split, allowing either or both of the two output amplifiers to be employed. Each amplifier is provided with a dummy output.

To provide reliable imaging in the presence of bright highlights, anti-blooming is incorporated. This is of the shielded anti-blooming type, in order to maintain quantum efficiency. This version of the CCD48 is manufactured in standard NIMO format. This has the benefit of allowing faster vertical transfer rates than AIMO format.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE
Maximum readout frequency ........ 10 MHz
Output responsivity .............. 2 µV/e−
Peak signal ..................... 90 e−/pixel
Dynamic range at 10 MHz ....... 2500:1
Spectral range ................. 200 - 1100 nm
Readout noise at 10 MHz ....... 35 e− rms

GENERAL DATA
Format
Image area ............. 13.3 x 13.3 mm
Active pixels (H) ....... 1024
(V) ........... 1024
Pixel size .............. 13 x 13 µm
Storage area ............. 13.3 x 13.3 mm
Pixels (H) ............... 1024
(V) ............... 1024

Additional pixels are provided in both the image and storage areas for dark reference and over-scanning purposes.

Number of output amplifiers ........ 2
Weight (approx, no window) ....... 7.5 g

Package
Package size ............... 22.7 x 42.0 mm
Number of pins .............. 32
Inter-pin spacing ........... 2.54 mm
Window material ............ quartz or removable glass
Type ............... ceramic DIL array
PERFORMANCE

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak charge storage (see note 1)</td>
<td>70</td>
<td>90</td>
<td>-</td>
</tr>
<tr>
<td>Peak output voltage (unbinned)</td>
<td>-</td>
<td>180</td>
<td>-</td>
</tr>
<tr>
<td>Dark signal at 293 K (see notes 2 and 3)</td>
<td>-</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>Dynamic range (see note 4)</td>
<td>-</td>
<td>2500:1</td>
<td>-</td>
</tr>
<tr>
<td>Charge transfer efficiency (see note 5):</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>parallel</td>
<td>-</td>
<td>99.9999</td>
<td>-</td>
</tr>
<tr>
<td>serial</td>
<td>-</td>
<td>99.9993</td>
<td>-</td>
</tr>
<tr>
<td>Output amplifier responsivity (see note 3)</td>
<td>1.2</td>
<td>2.0</td>
<td>2.8</td>
</tr>
<tr>
<td>Readout noise at 10 MHz (see note 6)</td>
<td>-</td>
<td>35</td>
<td>-</td>
</tr>
<tr>
<td>Maximum readout frequency (see note 7)</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Dark signal non-uniformity (std. deviation) (see notes 3 and 8)</td>
<td>-</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

Spectral Response at 268 K

<table>
<thead>
<tr>
<th>Wavelength (nm)</th>
<th>Minimum Response (QE)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Enhanced Process UV Coated</td>
</tr>
<tr>
<td>300</td>
<td>45</td>
</tr>
<tr>
<td>350</td>
<td>45</td>
</tr>
<tr>
<td>400</td>
<td>55</td>
</tr>
<tr>
<td>500</td>
<td>60</td>
</tr>
<tr>
<td>650</td>
<td>60</td>
</tr>
<tr>
<td>900</td>
<td>30</td>
</tr>
</tbody>
</table>

The uncoated process is suitable for soft X-ray and EUV applications.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>SΩ/ICΩ interphase</td>
<td>-</td>
<td>3.5</td>
<td>-</td>
</tr>
<tr>
<td>IΩ/IΩ interphase</td>
<td>-</td>
<td>3.5</td>
<td>-</td>
</tr>
<tr>
<td>IΩ/SS and SΩ/SS</td>
<td>-</td>
<td>4.5</td>
<td>-</td>
</tr>
<tr>
<td>RΩ/RΩ interphase</td>
<td>-</td>
<td>40</td>
<td>-</td>
</tr>
<tr>
<td>RΩ/(SS + OD)</td>
<td>-</td>
<td>60</td>
<td>-</td>
</tr>
<tr>
<td>ΩζR/(SS)</td>
<td>-</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>Output impedance at typical operating conditions</td>
<td>-</td>
<td>300</td>
<td>Ω</td>
</tr>
</tbody>
</table>

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 233 and 273 K and V_SSS + 9.0 V. Dark signal at any temperature T (kelvin) may be estimated from:

   \[ Q_d/Q_{d0} = 122 T^3 e^{-6400/T} \]

   where \( Q_{d0} \) is the dark signal at \( T = 293 \) K (20 °C).
3. Test carried out at e2v technologies on all sensors.
4. Dynamic range is the ratio of readout noise to full well capacity measured at 10 MHz readout speed.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
7. Readout at speeds in excess of 10 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 233 and 273 K, excluding white defects.
BLEMISH SPECIFICATION

Traps  
Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 $e^-$ at 243 K.

Slipped columns  
Are counted if they have an amplitude greater than 200 $e^-$.

Black spots  
Are counted when they have a signal level less than 80% of the local mean at a signal level of approximately half full-well.

White spots  
Are counted when they have a generation rate 25 times the specified maximum dark signal generation rate (measured between 233 and 273 K). The amplitude of white spots will vary in the same manner as dark current, i.e.:

$$\frac{Q_d}{Q_{d0}} = 122T^3e^{-6400/T}$$

White column  
A column which contains at least 21 white defects.

Black column  
A column which contains at least 21 black defects.

<table>
<thead>
<tr>
<th>GRADE</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column defects:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>black or slipped white</td>
<td>0</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Black spots</td>
<td>50</td>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>Traps &gt; 200 $e^-$</td>
<td>2</td>
<td>5</td>
<td>12</td>
</tr>
<tr>
<td>White spots</td>
<td>50</td>
<td>80</td>
<td>100</td>
</tr>
</tbody>
</table>

Grade 5  
Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters.

Minimum separation between adjacent black columns . . . . . . . . . . . . . 50 pixels

Note  
The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 233 K. The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL SPECTRAL RESPONSE (No window)
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE
(Two I paras builds low)

TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE

PACKAGE TEMPERATURE (°C)
DEVELOPMENT SCHEMATIC

There is a total of 3 shielded rows as shown, but the nominal position of the image section may vary by ± 1 row and ± 1 column.
## CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>PIN</th>
<th>REF</th>
<th>DESCRIPTION</th>
<th>PULSE AMPLITUDE OR DC LEVEL (V) (See note 9)</th>
<th>MAXIMUM RATINGS with respect to $V_{SS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SS</td>
<td>Substrate</td>
<td>Min 9 Typical 10</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>ABD</td>
<td>Anti-blooming drain</td>
<td>16   18 20</td>
<td>$-0.3$ to $+25$ V</td>
</tr>
<tr>
<td>3</td>
<td>IØ3</td>
<td>Image area clock</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>4</td>
<td>IØ2</td>
<td>Image area clock</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>5</td>
<td>IØ1</td>
<td>Image area clock</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>6</td>
<td>SS</td>
<td>Substrate</td>
<td>0    9 10</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>OG</td>
<td>Output gate</td>
<td>1    3 5</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>8</td>
<td>RDL</td>
<td>Reset transistor drain (left amplifier)</td>
<td>15   17 19</td>
<td>$-0.3$ to $+25$ V</td>
</tr>
<tr>
<td>9</td>
<td>DOSL</td>
<td>Output transistor source (dummy)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>OSL</td>
<td>Output transistor source (left amplifier)</td>
<td>see note 10</td>
<td>$-0.3$ to $+25$ V</td>
</tr>
<tr>
<td>11</td>
<td>ODL</td>
<td>Output transistor drain (left amplifier)</td>
<td>20   22 25</td>
<td>$-0.3$ to $+35$ V</td>
</tr>
<tr>
<td>12</td>
<td>SS</td>
<td>Substrate</td>
<td>0    9 10</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>ØRL</td>
<td>Output reset pulse (left amplifier)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>14</td>
<td>RØ3L</td>
<td>Output register clock (left section)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>15</td>
<td>RØ2L</td>
<td>Output register clock (left section)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>16</td>
<td>RØ1L</td>
<td>Output register clock (left section)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>17</td>
<td>RØ1R</td>
<td>Output register clock (right section)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>18</td>
<td>RØ2R</td>
<td>Output register clock (right section)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>19</td>
<td>RØ3R</td>
<td>Output register clock (right section)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>20</td>
<td>ØRR</td>
<td>Output reset pulse (right amplifier)</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>21</td>
<td>SS</td>
<td>Substrate</td>
<td>0    9 10</td>
<td>-</td>
</tr>
<tr>
<td>22</td>
<td>ODR</td>
<td>Output transistor drain (right amplifier)</td>
<td>20   22 25</td>
<td>$-0.3$ to $+35$ V</td>
</tr>
<tr>
<td>23</td>
<td>OSR</td>
<td>Output transistor source (right amplifier)</td>
<td>see note 10</td>
<td>$-0.3$ to $+25$ V</td>
</tr>
<tr>
<td>24</td>
<td>DOSR</td>
<td>Output transistor source (dummy)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>25</td>
<td>RDR</td>
<td>Reset transistor drain (right amplifier)</td>
<td>15   17 19</td>
<td>$-0.3$ to $+25$ V</td>
</tr>
<tr>
<td>26</td>
<td>BG</td>
<td>Bias gate (see note 11)</td>
<td>0    0 2</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>27</td>
<td>SS</td>
<td>Substrate</td>
<td>0    9 10</td>
<td>-</td>
</tr>
<tr>
<td>28</td>
<td>SØ1</td>
<td>Storage area clock</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>29</td>
<td>SØ2</td>
<td>Storage area clock</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>30</td>
<td>SØ3</td>
<td>Storage area clock</td>
<td>8    12 15</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>31</td>
<td>ABG</td>
<td>Anti-blooming gate</td>
<td>0    0 5</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>32</td>
<td>SS</td>
<td>Substrate</td>
<td>0    9 10</td>
<td>-</td>
</tr>
</tbody>
</table>

Maximum voltages between pairs of pins:
- pin 10 (OSL) to pin 11 (ODL) $\pm 15$ V
- pin 22 (ODR) to pin 23 (OSR) $\pm 15$ V

Maximum output transistor current $10$ mA

### NOTES

9. Clock low levels $0 \pm 0.5$ V.

10. $3$ to $5$ V below OD. Connect to ground using a $2$ to $5$ mA current source or appropriate load resistor (typically $5$ to $10$ kΩ).

11. Adjust for output transistor bias current.

12. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required for to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.

13. With the RØ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs RØ1(L) and RØ2(L) should be reversed.
FRAME TRANSFER TIMING DIAGRAM

CHARGE COLLECTION PERIOD

1033 CYCLES

5028 CYCLES

SEE DETAIL OF LINE TRANSFER

FRAME TRANSFER PERIOD

>1 LINE TIME

SEE DETAIL OF OUTPUT CLOCKING

READOUT PERIOD

DETAIL OF LINE TRANSFER (For output from a single amplifier)
DETAIL OF OUTPUT CLOCKING

LINE OUTPUT FORMAT

CLOCK TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_i$</td>
<td>Image clock period</td>
<td>2</td>
<td>5</td>
<td>see note 14</td>
</tr>
<tr>
<td>$t_{wi}$</td>
<td>Image clock pulse width</td>
<td>1</td>
<td>2.5</td>
<td>see note 14</td>
</tr>
<tr>
<td>$t_{ri}$</td>
<td>Image clock pulse rise time (10 to 90%)</td>
<td>0.1</td>
<td>0.5</td>
<td>0.2 $T_i$</td>
</tr>
<tr>
<td>$t_{ff}$</td>
<td>Image clock pulse fall time (10 to 90%)</td>
<td>$t_{ri}$</td>
<td>0.5</td>
<td>0.2 $T_i$</td>
</tr>
<tr>
<td>$t_{oi}$</td>
<td>Image clock pulse overlap</td>
<td>$(t_{ri} + t_{ff})/2$</td>
<td>0.5</td>
<td>0.2 $T_i$</td>
</tr>
<tr>
<td>$t_{df}$</td>
<td>Delay time, $S\not{\bigcirc}$ stop to $R\not{\bigcirc}$ start</td>
<td>1</td>
<td>2</td>
<td>see note 14</td>
</tr>
<tr>
<td>$t_{dfi}$</td>
<td>Delay time, $R\not{\bigcirc}$ stop to $S\not{\bigcirc}$ start</td>
<td>1</td>
<td>1</td>
<td>see note 14</td>
</tr>
<tr>
<td>$T_r$</td>
<td>Output register clock cycle period</td>
<td>100</td>
<td>1000</td>
<td>see note 14</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Clock pulse rise time (10 to 90%)</td>
<td>50</td>
<td>0.1 $T_r$</td>
<td>0.3 $T_r$</td>
</tr>
<tr>
<td>$t_{fr}$</td>
<td>Clock pulse fall time (10 to 90%)</td>
<td>$t_{fr}$</td>
<td>0.1 $T_r$</td>
<td>0.3 $T_r$</td>
</tr>
<tr>
<td>$t_{or}$</td>
<td>Clock pulse overlap</td>
<td>20</td>
<td>0.5 $t_{fr}$</td>
<td>0.1 $T_r$</td>
</tr>
<tr>
<td>$t_{wx}$</td>
<td>Reset pulse width</td>
<td>30</td>
<td>0.1 $T_r$</td>
<td>0.3 $T_r$</td>
</tr>
<tr>
<td>$t_{wx}$, $t_{fx}$</td>
<td>Reset pulse rise and fall times</td>
<td>$0.2t_{wx}$</td>
<td>0.5$t_{fr}$</td>
<td>0.1 $T_r$</td>
</tr>
<tr>
<td>$t_{dx}$</td>
<td>Delay time, $S\not{\bigcirc}$ low to $R\not{\bigcirc}3$ low</td>
<td>30</td>
<td>0.5 $T_r$</td>
<td>0.8 $T_r$</td>
</tr>
</tbody>
</table>

NOTES
14. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
15. To minimise dark current, two of the I$\not{\bigcirc}$ clocks should be held low during integration. I$\not{\bigcirc}$ timing requirements are identical to S$\not{\bigcirc}$ (as shown above).
OUTPUT CIRCUIT

NOTES
16. 3.3 kΩ resistors shown connected to OS and DOS are external to the CCD.
OUTLINE
(All dimensions without limits are nominal)

<table>
<thead>
<tr>
<th>Ref</th>
<th>Millimetres</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>42.00 ± 0.42</td>
</tr>
<tr>
<td>B</td>
<td>22.73 ± 0.26</td>
</tr>
<tr>
<td>C</td>
<td>16.60 ± 0.25</td>
</tr>
<tr>
<td>D</td>
<td>3.64 ± 0.37</td>
</tr>
<tr>
<td>E</td>
<td>22.86 ± 0.25</td>
</tr>
<tr>
<td>F</td>
<td>0.254 ± 0.051</td>
</tr>
<tr>
<td>G</td>
<td>5.0 ± 0.5</td>
</tr>
<tr>
<td>H</td>
<td>0.457 ± 0.051</td>
</tr>
<tr>
<td>J</td>
<td>2.54 ± 0.13</td>
</tr>
<tr>
<td>K</td>
<td>38.1</td>
</tr>
<tr>
<td>L</td>
<td>1.65 ± 0.50</td>
</tr>
<tr>
<td>M</td>
<td>13.3</td>
</tr>
<tr>
<td>N</td>
<td>13.3</td>
</tr>
<tr>
<td>P</td>
<td>12.2 ± 0.5</td>
</tr>
</tbody>
</table>
ORDERING INFORMATION
Options include:
- Permanent Quartz Window
- Temporary Glass Window
- Permanent Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS
CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:
- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 3, 4, 5, 7, 13, 14, 15, 16, 17, 18, 19, 20, 26, 28, 29, 30, 31) but not to the other pins.

HIGH ENERGY RADIATION
Device characteristics will change when subject to ionising radiation.

Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage</td>
<td>153</td>
<td>-</td>
<td>373 K</td>
</tr>
<tr>
<td>Operating</td>
<td>153</td>
<td>243</td>
<td>323 K</td>
</tr>
</tbody>
</table>

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min