e2v technologies

CCD48-20 Back Illuminated High Performance NIMO CCD Sensor

FEATURES

- 1024 by 1024 1:1 Image Format
- Image Area 13.3 x 13.3 mm
- Frame Transfer Operation
- 13 μm Square Pixels
- Symmetrical Anti-static Gate Protection
- High Speed Output Amplifiers
- 100% Active Area
- Shielded Anti-bloom Pixel Structure

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION

This version of the CCD48-20 is a back-face illuminated, frame transfer CCD sensor with high performance, high speed output amplifiers. The image area contains a full 1024 by 1024 pixels which are 13 μm square. The output register is split, allowing either or both of the two output amplifiers to be employed. Each amplifier is provided with a dummy output.

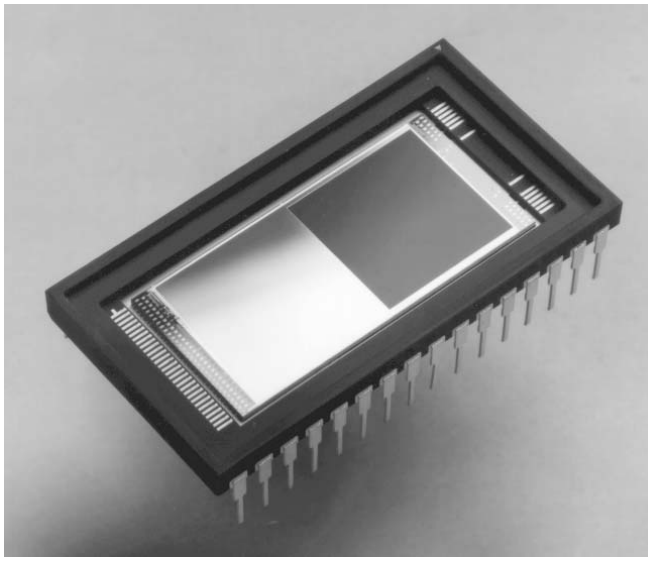
To provide reliable imaging in the presence of bright highlights, anti-blooming is incorporated. This is of the shielded anti-blooming type, in order to maintain quantum efficiency.

This version of the CCD48 is manufactured in standard NIMO format. This has the benefit of allowing faster vertical transfer rates than AIMO format.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE

Maximum readout frequency	10	MHz
Output responsivity	2	$\mu V/e^-$
Peak signal	90	ke^-/pixel
Dynamic range at 10 MHz	2500:1	
Spectral range	200 - 1100	nm
Readout noise at 10 MHz	35	e^- rms



GENERAL DATA

Format

Image area	13.3 x 13.3	mm
Active pixels (H)	1024	
(V)	1024	
Pixel size	13 x 13	μm
Storage area	13.3 x 13.3	mm
Pixels (H)	1024	
(V)	1024	

Additional pixels are provided in both the image and storage areas for dark reference and over-scanning purposes.

Number of output amplifiers	2	
Weight (approx, no window)	7.5	g

Package

Package size	22.7 x 42.0 mm
Number of pins	32
Inter-pin spacing	2.54 mm
Window material	quartz or removable glass
Type	ceramic DIL array

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	70	90	-	ke^-/pixel
Peak output voltage (unbinned)	-	180	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	20	40	ke^-/pixel/s
Dynamic range (see note 4)	-	2500:1	-	
Charge transfer efficiency (see note 5): parallel serial	 - -	 99.9999 99.9993	 - -	 % %
Output amplifier responsivity (see note 3)	1.2	2.0	2.8	$\mu V/e^-$
Readout noise at 10 MHz (see note 6)	-	35	-	rms e^-/pixel
Maximum readout frequency (see note 7)	-	10	-	MHz
Dark signal non-uniformity (std. deviation) (see notes 3 and 8)	-	2	4	ke^-/pixel/s

Spectral Response at 268 K

Wavelength (nm)	Minimum Response (QE)					Maximum Response Non-uniformity (1σ)	
	Enhanced Process UV Coated	Enhanced Process Broadband Coated	Basic Process Mid-band Coated	Basic Process Broadband Coated	Basic Process Uncoated		
300	45	-	-	-	-	-	%
350	45	50	15	25	10	5	%
400	55	80	40	55	25	3	%
500	60	80	85	75	55	3	%
650	60	75	85	75	50	3	%
900	30	30	30	30	30	5	%

The uncoated process is suitable for soft X-ray and EUV applications.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

	Min	Typical	Max	
S∅/S∅ interphase	-	3.5	-	nF
I∅/I∅ interphase	-	3.5	-	nF
I∅/SS and S∅/SS	-	4.5	-	nF
R∅/R∅ interphase	-	40	-	pF
R∅/(SS + OD)	-	60	-	pF
∅R/(SS)	-	10	-	pF
Output impedance at typical operating conditions	-	300	-	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 233 and 273 K and V_{SS} +9.0 V. Dark signal at any temperature T (kelvin) may be estimated from:
   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
   where Q_{d0} is the dark signal at T = 293 K (20 °C).
3. Test carried out at e2v technologies on all sensors.
4. Dynamic range is the ratio of readout noise to full well capacity measured at 10 MHz readout speed.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
6. Measured using correlated double sampling (CDS).
7. Readout at speeds in excess of 10 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 233 and 273 K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a signal level less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 25 times the specified maximum dark signal generation rate (measured between 233 and 273 K). The amplitude of white spots will vary in the same manner as dark current, i.e.:

$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

White column A column which contains at least 21 white defects.

Black column A column which contains at least 21 black defects.

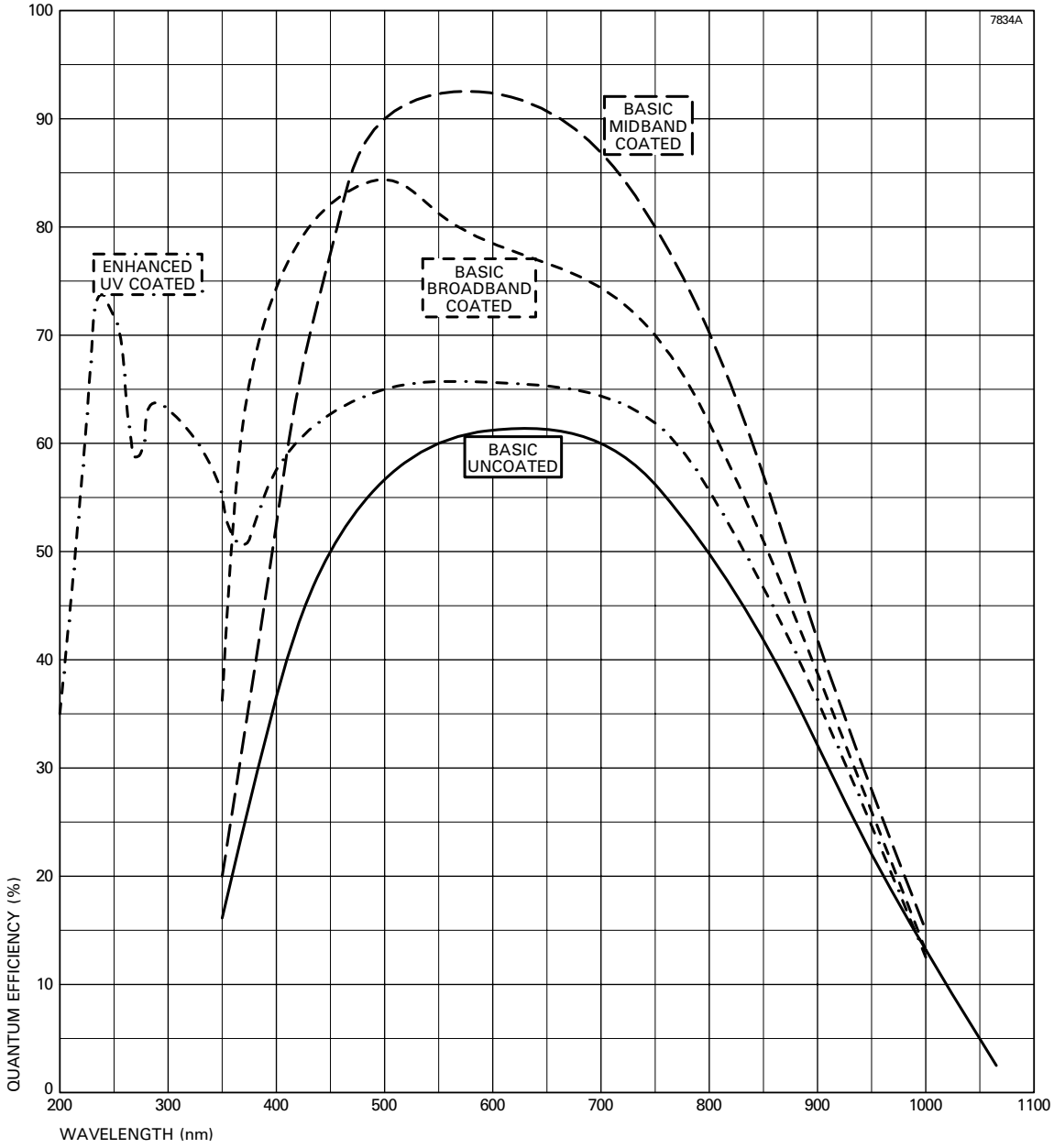
GRADE	0	1	2
Column defects:			
black or slipped	0	2	6
white	0	0	0
Black spots	50	100	200
Traps > 200 e^-	2	5	12
White spots	50	80	100

Grade 5 Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters.

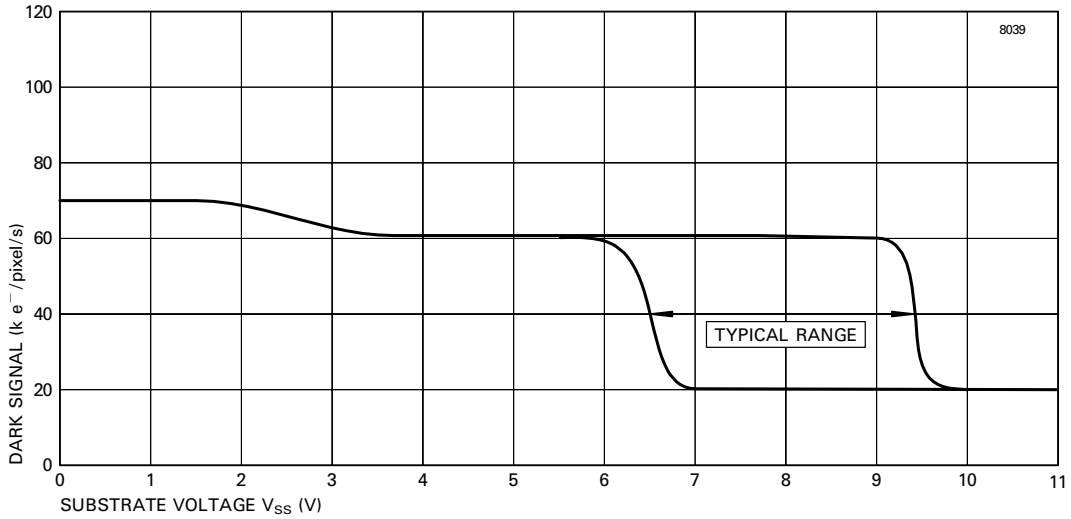
Minimum separation between adjacent black columns . . . . . 50 pixels

Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 233 K. The amplitude of white spots and columns will decrease rapidly with temperature.

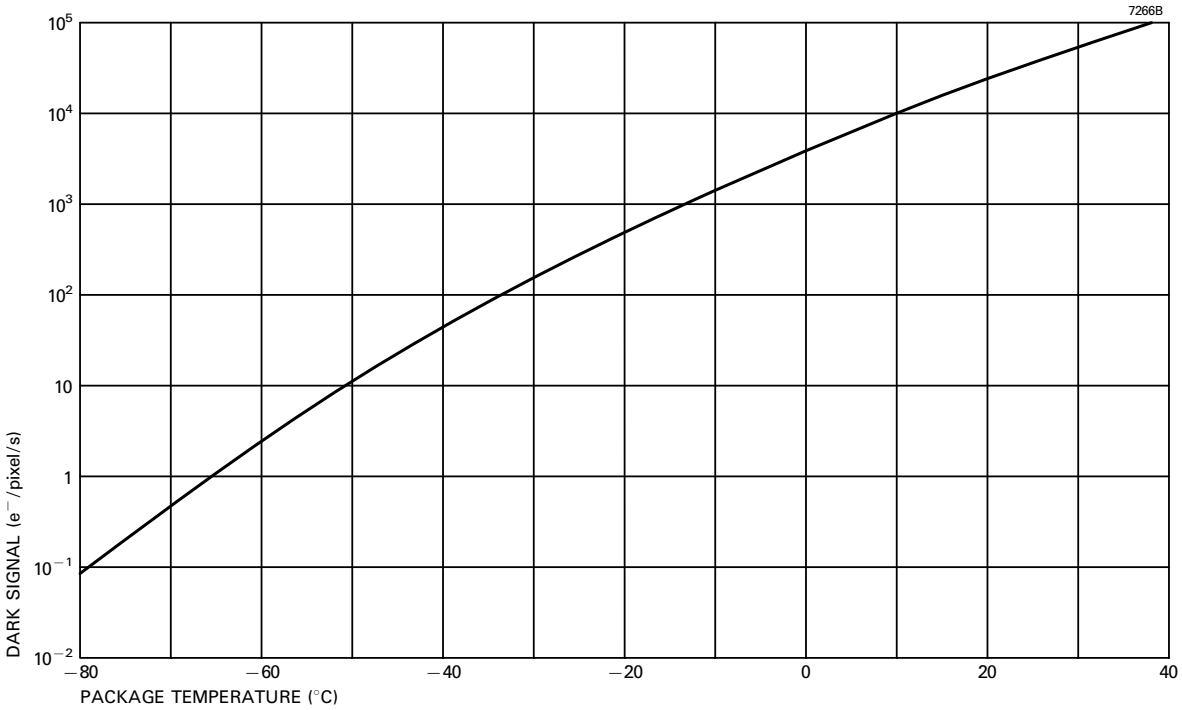
TYPICAL SPECTRAL RESPONSE (No window)



TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE
(Two I∅ phases held low)

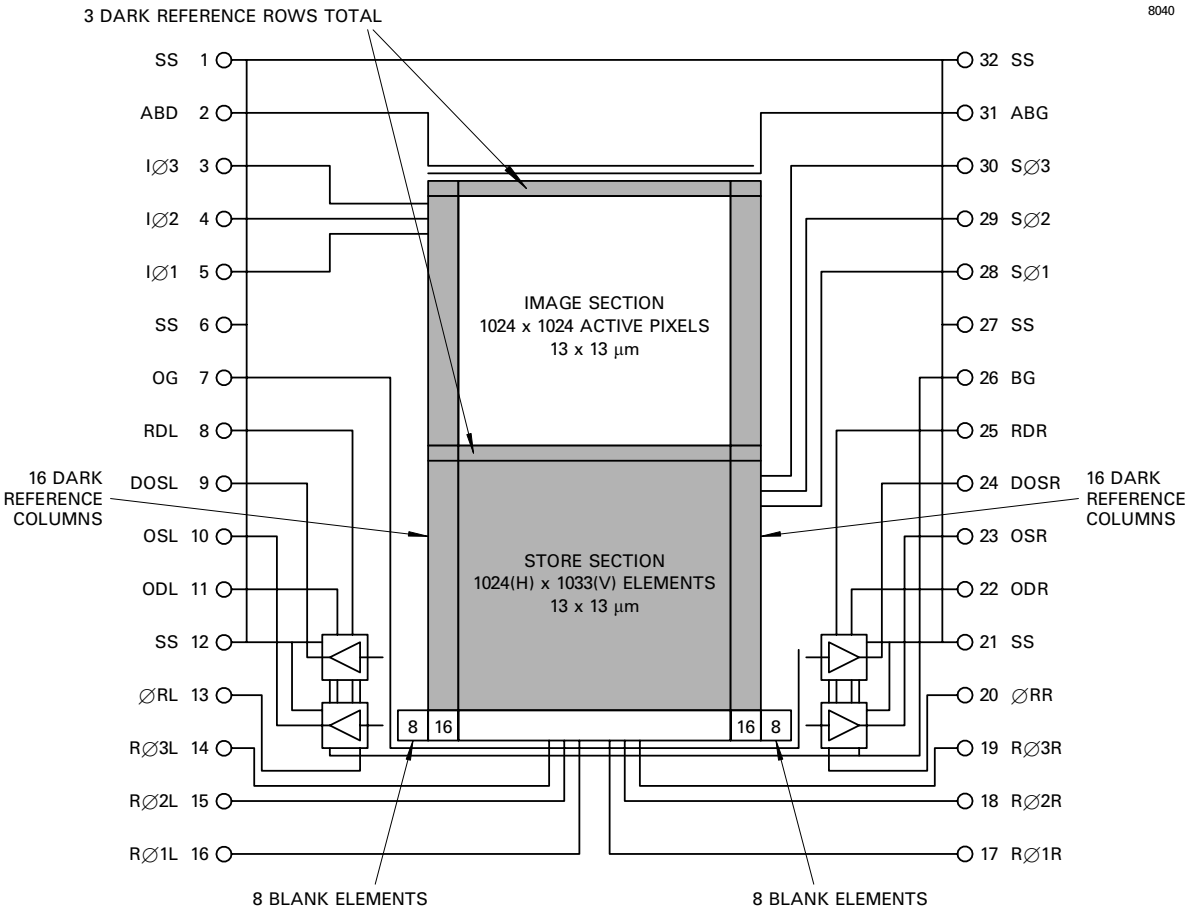


TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



DEVICE SCHEMATIC

There is a total of 3 shielded rows as shown, but the nominal position of the image section may vary by ± 1 row and ± 1 column.



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (See note 9)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	SS	Substrate	0	9	10	-
2	ABD	Anti-blooming drain	16	18	20	−0.3 to +25 V
3	I∅3	Image area clock	8	12	15	±20 V
4	I∅2	Image area clock	8	12	15	±20 V
5	I∅1	Image area clock	8	12	15	±20 V
6	SS	Substrate	0	9	10	-
7	OG	Output gate	1	3	5	±20 V
8	RDL	Reset transistor drain (left amplifier)	15	17	19	−0.3 to +25 V
9	DOSL	Output transistor source (dummy)		-		-
10	OSL	Output transistor source (left amplifier)		see note 10		−0.3 to +25 V
11	ODL	Output transistor drain (left amplifier)	20	22	25	−0.3 to +35 V
12	SS	Substrate	0	9	10	-
13	∅RL	Output reset pulse (left amplifier)	8	12	15	±20 V
14	R∅3L	Output register clock (left section)	8	12	15	±20 V
15	R∅2L	Output register clock (left section)	8	12	15	±20 V
16	R∅1L	Output register clock (left section)	8	12	15	±20 V
17	R∅1R	Output register clock (right section)	8	12	15	±20 V
18	R∅2R	Output register clock (right section)	8	12	15	±20 V
19	R∅3R	Output register clock (right section)	8	12	15	±20 V
20	∅RR	Output reset pulse (right amplifier)	8	12	15	±20 V
21	SS	Substrate	0	9	10	-
22	ODR	Output transistor drain (right amplifier)	20	22	25	−0.3 to +35 V
23	OSR	Output transistor source (right amplifier)		see note 10		−0.3 to +25 V
24	DOSR	Output transistor source (dummy)		-		-
25	RDR	Reset transistor drain (right amplifier)	15	17	19	−0.3 to +25 V
26	BG	Bias gate (see note 11)	0	0	2	±20 V
27	SS	Substrate	0	9	10	-
28	S∅1	Storage area clock	8	12	15	±20 V
29	S∅2	Storage area clock	8	12	15	±20 V
30	S∅3	Storage area clock	8	12	15	±20 V
31	ABG	Anti-blooming gate	0	0	5	±20 V
32	SS	Substrate	0	9	10	-

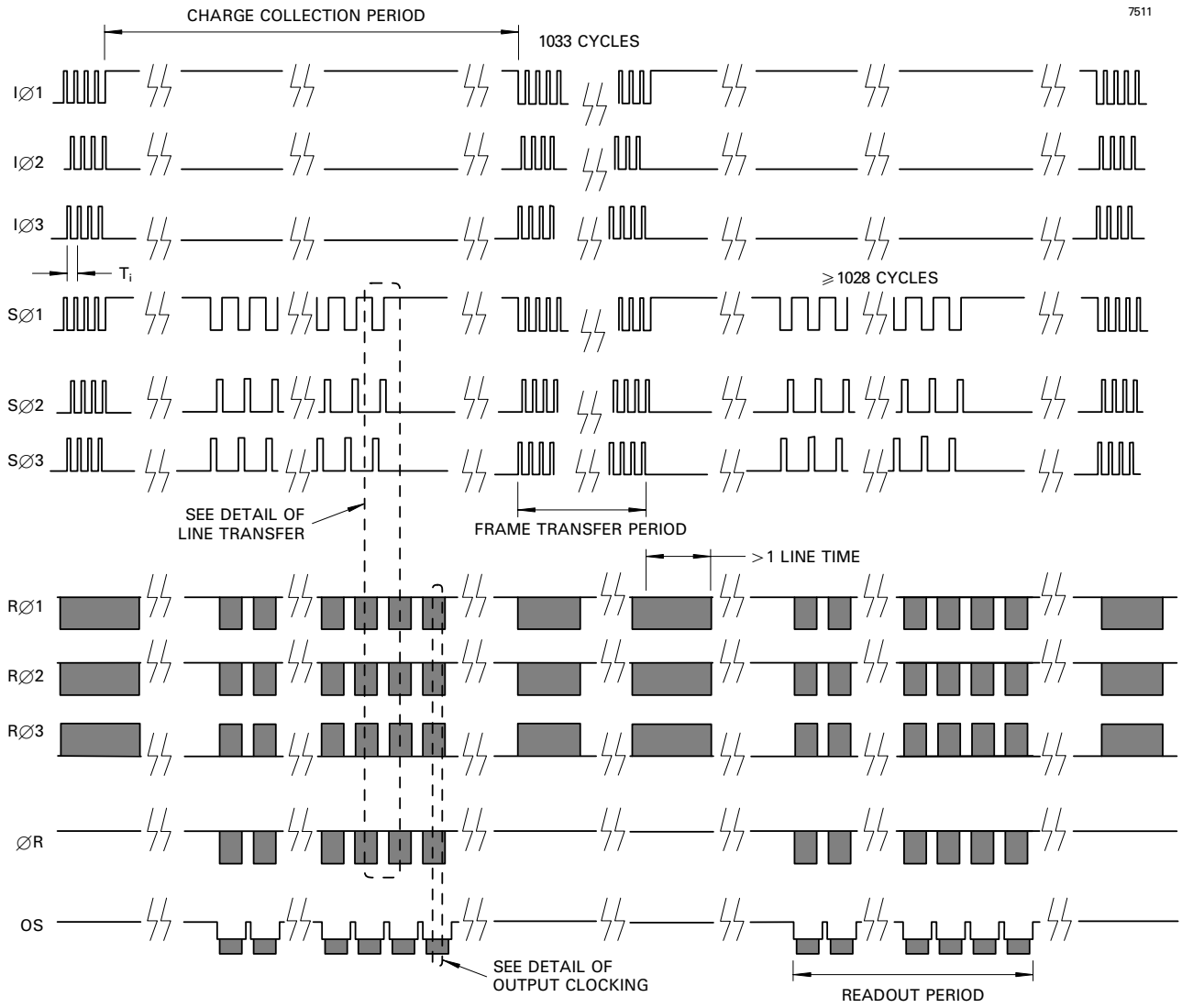
Maximum voltages between pairs of pins:
- pin 10 (OSL) to pin 11 (ODL) . . . . . ±15 V
- pin 22 (ODR) to pin 23 (OSR) . . . . . ±15 V

Maximum output transistor current . . . . . 10 mA

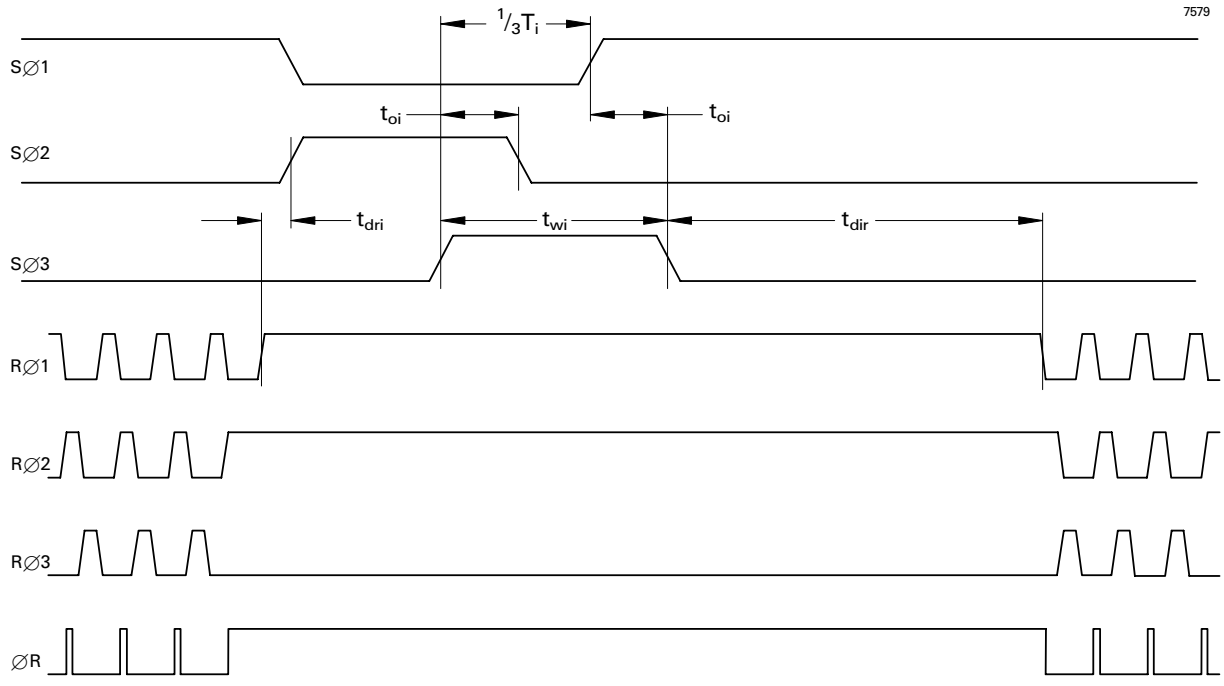
NOTES

9. Clock low levels 0 ± 0.5 V.
10. 3 to 5 V below OD. Connect to ground using a 2 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
11. Adjust for output transistor bias current.
12. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required for to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
13. With the R∅ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs R∅1(L) and R∅2(L) should be reversed.

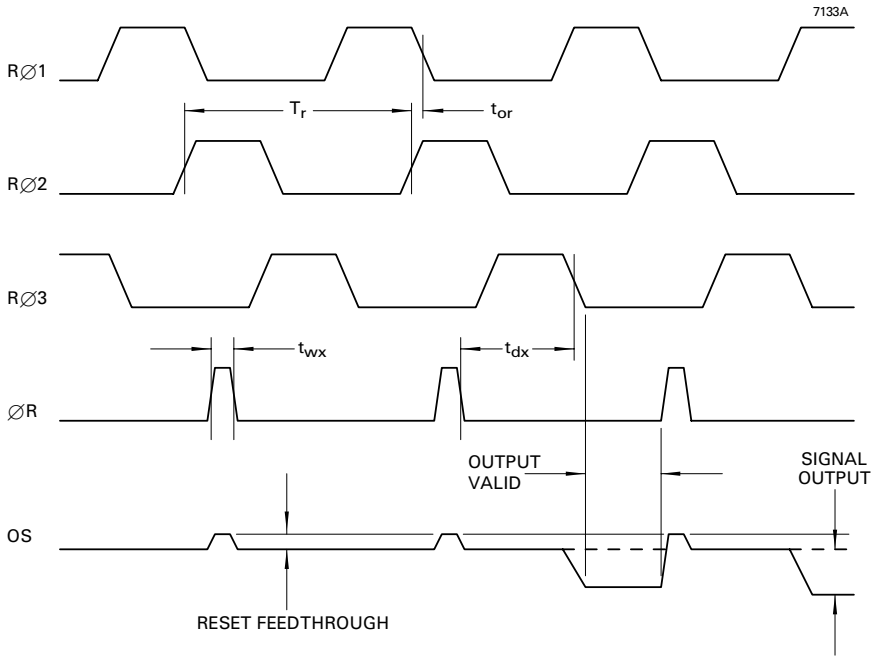
FRAME TRANSFER TIMING DIAGRAM



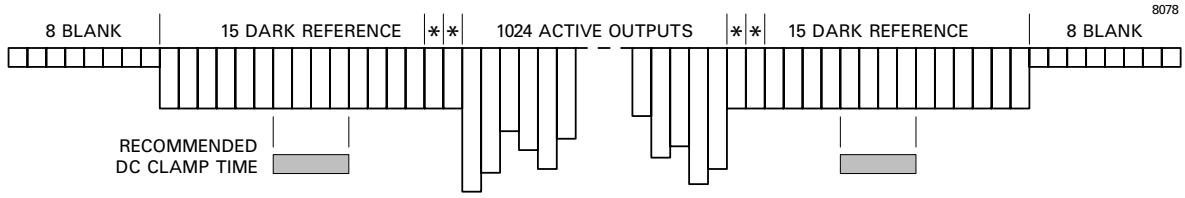
DETAIL OF LINE TRANSFER (For output from a single amplifier)



DETAIL OF DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



* = Partially shielded transition elements

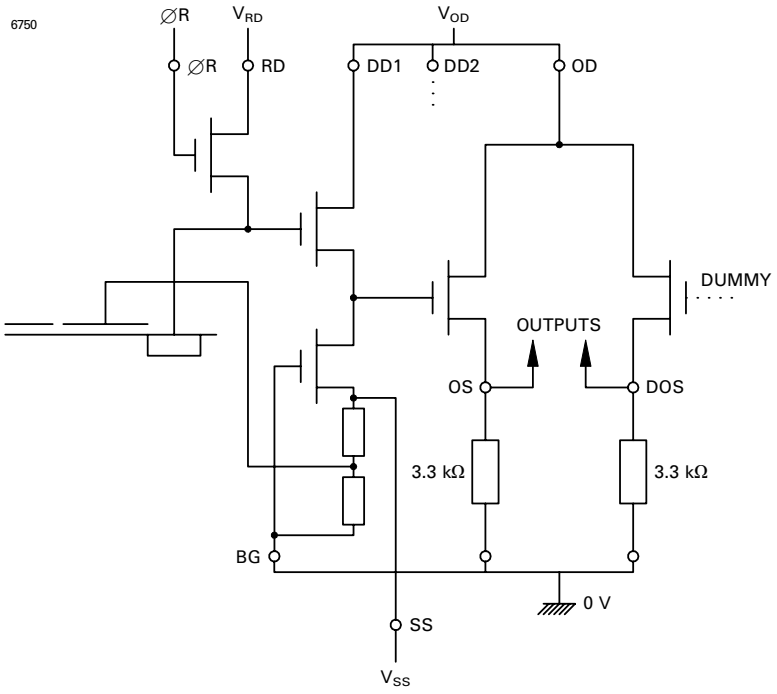
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	2	5	see note 14	µs
t_{wi}	Image clock pulse width	1	2.5	see note 14	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	0.5	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	0.5	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri}+t_{fi})/2$	0.5	$0.2T_i$	µs
t_{dir}	Delay time, SØ stop to RØ start	1	2	see note 14	µs
t_{dri}	Delay time, RØ stop to SØ start	1	1	see note 14	µs
T_r	Output register clock cycle period	100	1000	see note 14	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

14. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
15. To minimise dark current, two of the IØ clocks should be held low during integration. IØ timing requirements are identical to SØ (as shown above).

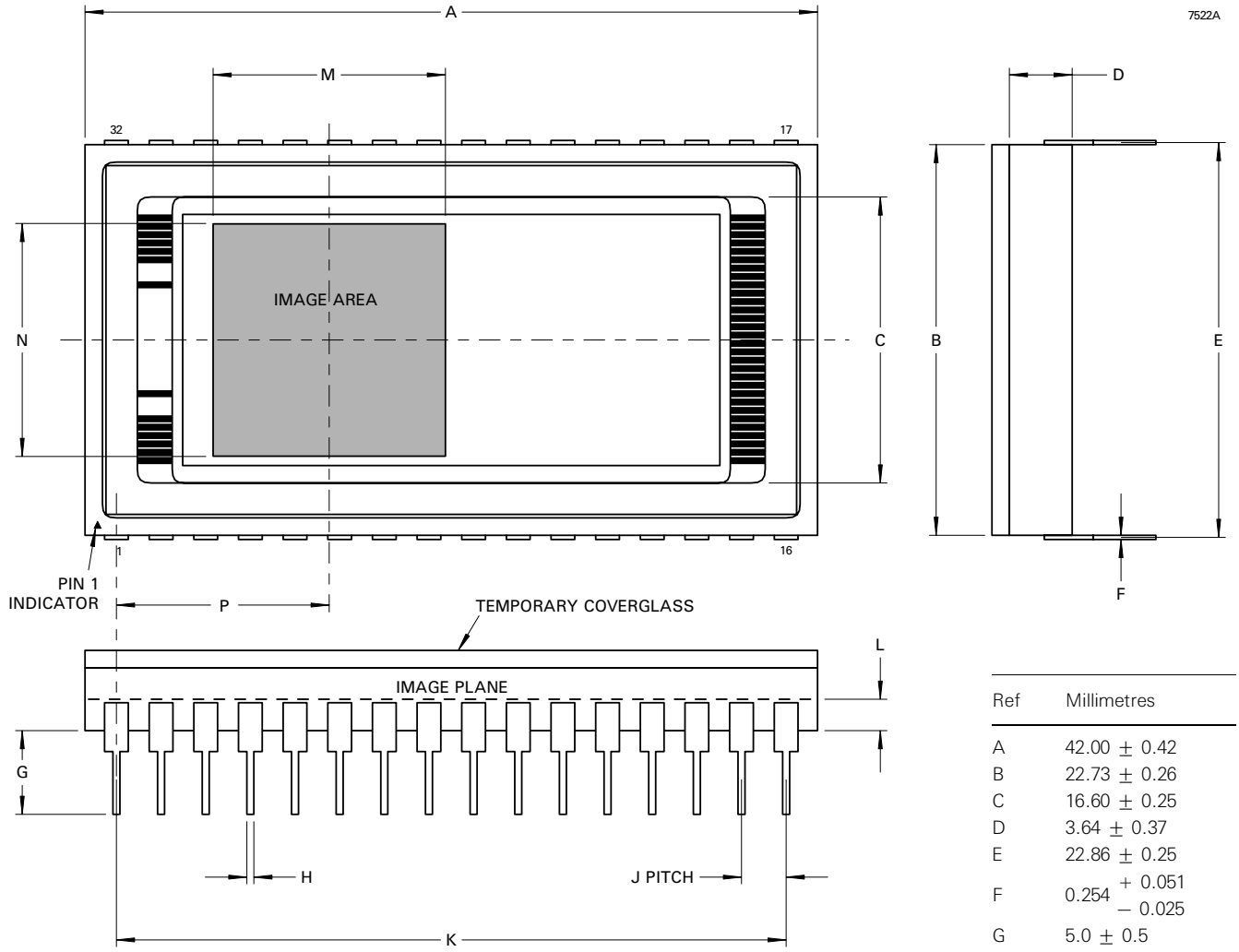
OUTPUT CIRCUIT



NOTES

16. 3.3 kΩ resistors shown connected to OS and DOS are external to the CCD.

OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	42.00 ± 0.42
B	22.73 ± 0.26
C	16.60 ± 0.25
D	3.64 ± 0.37
E	22.86 ± 0.25
F	$0.254^{+\ 0.051}_{-\ 0.025}$
G	5.0 ± 0.5
H	0.457 ± 0.051
J	2.54 ± 0.13
K	38.1
L	1.65 ± 0.50
M	13.3
N	13.3
P	12.2 ± 0.5

ORDERING INFORMATION

Options include:

- Permanent Quartz Window
- Temporary Glass Window
- Permanent Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 3, 4, 5, 7, 13, 14, 15, 16, 17, 18, 19, 20, 26, 28, 29, 30, 31) but not to the other pins.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.

Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	–	373	K
Operating	153	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min