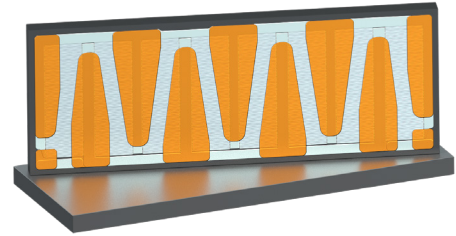
TELEDYNE HIREL ELECTRONICS Everywhereyoulook™

TDG100E90
100 V enhancement mode GaN transistor die
Preliminary Information



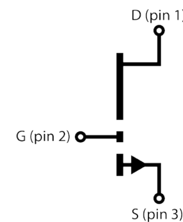
Description

- GaN enhancement mode power switch die
- $R_{DS(on)}$ = 7 mΩ
- Ultra-low FOM Island Technology™ die
- Easy gate drive requirements (0 V to 6 V)
- Fast and controllable fall and rise times
- Reverse current capability
- Dual gate pads for optimal module layout
- Zero reverse recovery loss

Applications

- DC-DC Power Stages

Circuit Symbol



The die substrate should be connected to the source pad for optimal performance.

Key Parameters

Parameter	Value	Unit
V_{DS}	100	V
I_D	90	A
Die Size	5.47 x 2.05	mm x mm
Die Thickness	265	µm

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_S	-55 to +150	°C
Storage Temperature Range	T_J	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	100	V
Drain to Source Voltage - transient (note 1)	$V_{DS(transient)}$	130	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to + 10	V
Continuous Drain Current (T_{case}=25 °C) (note 2)	I_{DS}	90	A
Continuous Drain Current (T_{case}=100 °C) (note 2)	I_{DS}	65	A

(1) For 1 µs
(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Unit
Thermal Resistance (junction-to-substrate)	$R_{\theta J\text{-}SUB}$	0.38	°C/W
Thermal Resistance (junction-to-top side RDL)	$R_{\theta J\text{-}RDL}$	0.70	°C/W

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Mechanical Parameters

Die Size	5.467 mm x 2.053 mm
Die Thickness	0.265 mm
Passivation	Polyimide
Top side metal	See figures 1, 2 and 3
Bottom side metal	See figures 1, 2 and 3

Electrical Characteristics at Wafer Level

(Typical values at T_J = 25 °C, V_{GS} = 6V unless otherwise noted)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	100			V	V_{GS}=0V, $I_{DSS} \leq$ 50 µA
Drain-to-Source On Resistance (note 3)	$R_{DS(on)}$		7	9.5	mΩ	V_{GS} = 6 V, T_J = 25 °C, I_{DS} = 9.0 A
Gate Threshold Turn on Voltage	$V_{GS(th)}$	1.1	1.3	2.5	V	V_{DS} = V_{GS}, I_D = 7 mA
Drain to Source Leakage Current	I_{DSS}		0.5	50	µA	V_{DS}= 100 V, V_{GS}= 0 V
Gate to Source Current	I_{GSS}		200		µA	V_{GS} = 6 V, V_{DS} = 0 V
Internal Gate Resistance	R_G		0.64		Ω	f=1 MHz, open drain
Input Capacitance	C_{ISS}		588		pF	V_{DS} = 80 V, V_{GS} = 0 V, f = 1 MHz
Output Capacitance	C_{OSS}		254		pF	
Reverse Transfer Capacitance	C_{RSS}		9.9		pF	
Total Gate Charge	Q_G		12		nC	V_{GS} = 0 to 6 V V_{DS} = 50 V I_D = 90 A
Gate-to-Source Charge	Q_{GS}		4.5		nC	
Gate-to-Drain Charge	Q_{GD}		1.5		nC	
Output Charge	Q_{OSS}		35		nC	V_{GS} = 0 V, V_{DS} = 50 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(3) Die is not tested to full current in production. Please refer to GS61008P data sheet for more detailed characteristics

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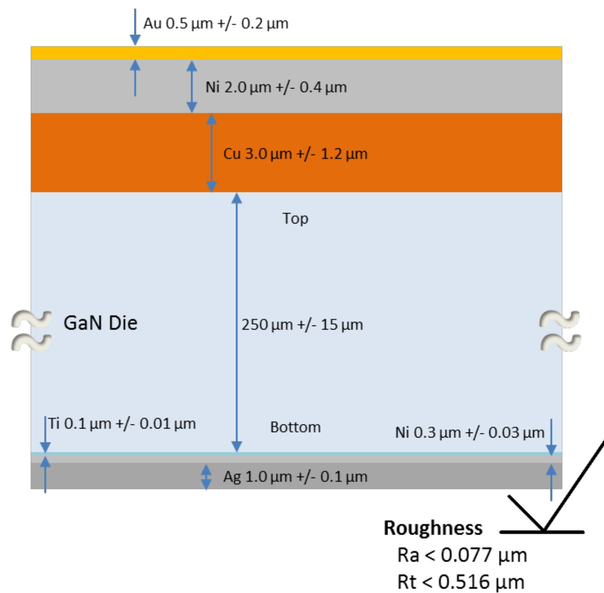
Ordering Information

Part number	Die Finish	Packing Method
TDG100E90D1	Option 1: NiAu/Ag	Contact Factory
TDG100E90D2	Option 2: Cu/Cu	Contact Factory
TEG100E90D3	Option 3: Cu/Ag	Contact Factory

Die Finish Options



Material	Thickness	Comment
Au	0.5 µm +/- 0.2 µm	Die top side = gold finish
Ni	2.0 µm +/- 0.4 µm	
Cu	3.0 µm +/- 1.2 µm	
GaN	250 µm +/- 15 µm	Die Core
Ti	0.1 µm +/- 0.01 µm	Die bottom side = silver finish
Ni	0.3 µm +/- 0.03 µm	
Ag	1.0 µm +/- 0.1 µm	

Figure 1: TDG100E90AD1X Ni/Au/Ag Die Finish

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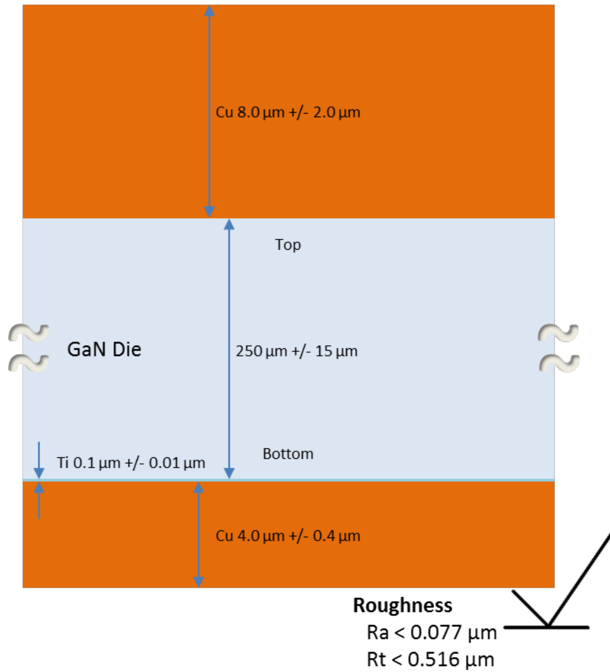
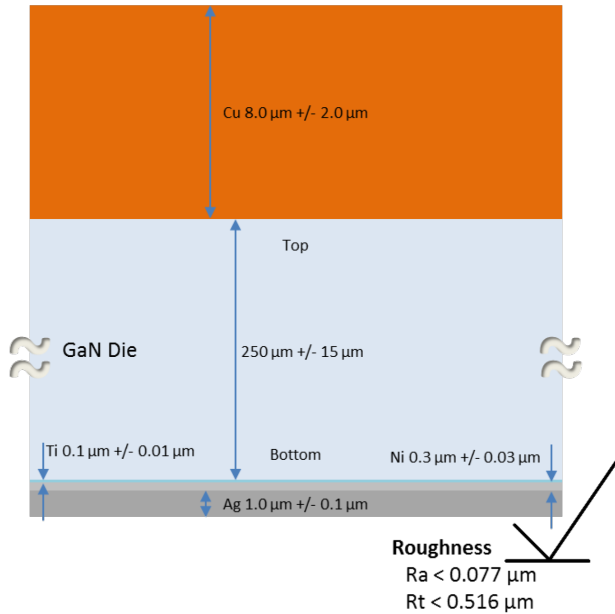


Material	Thickness	Comment
Cu	8.0 µm +/- 2.0 µm	Die top side = copper finish
GaN	250 µm +/- 15 µm	Die Core
Ti	0.1 µm +/- 0.01 µm	Die bottom side = copper finish
Cu	4.0 µm +/- 0.4 µm	

Figure 2: TDG100E90AD2X Cu/Cu Die Finish



Material	Thickness	Comment
Cu	8.0 µm +/- 2.0 µm	Die top side = copper finish
GaN	250 µm +/- 15 µm	Die Core
Ti	0.1 µm +/- 0.01 µm	Die bottom side = silver finish
Ni	0.3 µm +/- 0.03 µm	
Ag	1.0 µm +/- 0.1 µm	

Figure 3: TDG100E90AD3X Cu/Ag Die Finish

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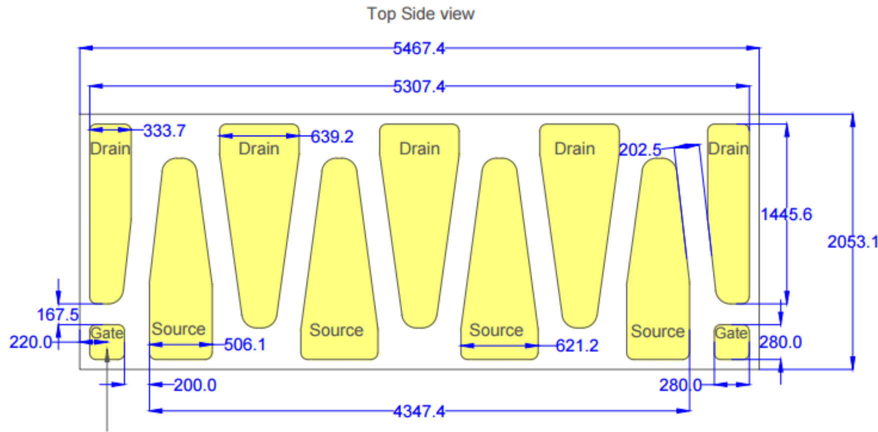
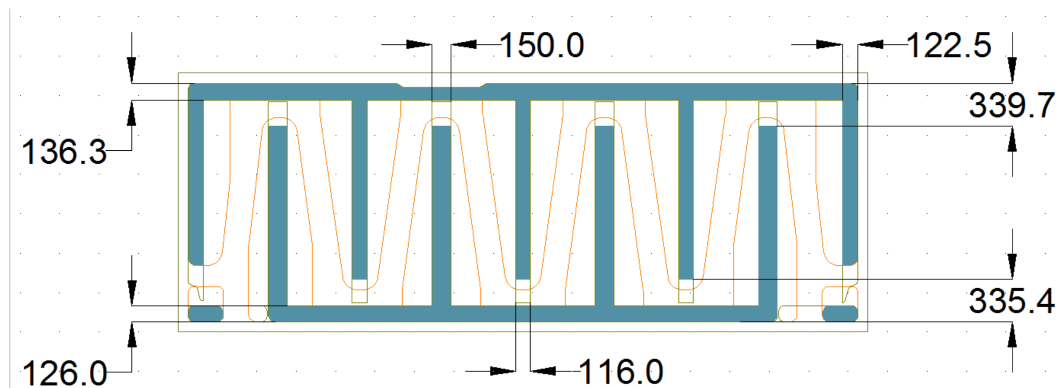
Dimensions



Dimension Drawing Notes:

1. All dimensions are in µm.
2. The drawing shows view of die facing up, substrate down.
3. The total die thickness is 265 µm.

Figure 4: Die Top View



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