TELEDYNE HIREL ELECTRONICS
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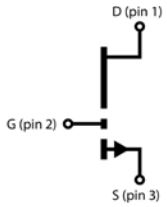
EVG100E15
100 V enhancement mode GaN transistor
Preliminary Specification

February 2018

Features

- 100 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 19 mΩ (Typ)
- $I_{DS(max)}$ = 15 A
- Ultra-low FOM Island Technology™ die
- Low inductance 1.5 nH (Typ)
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (f>10 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss

Circuit Symbol



The Source (S- pin 3) and substrate are internally connected and serves as the thermal pad for the device

Applications

- High efficiency power conversion
- High density power conversion
- Enterprise and Networking Power
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Motor Drives
- Fast Battery Charging

Description

The EVG100E15 is an enhancement mode GaN-on-Silicon power transistor based on GaN Systems technology. The properties of GaN allow for high current, high voltage breakdown, high switching frequency and high temperature operation. GaN Systems implements patented Island Technology® cell layout for high-current die performance & yield. e2v ceramic packaging enables low inductance & low thermal resistance in the SMD 05 ceramic package. The EVG100E15 is a bottom-cooled transistor for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Temperature	T_a	-55 to +125	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	100	V
Transient Drain to Source Voltage (note 1)	$V_{DS(transient)}$	130	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C) (note 2)	I_{DS}	15	A
Continuous Drain Current (T_{case}=100 °C) (note 2)	I_{DS}	15	A

(1) For 1 µs, duty cycle D<0.1

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance (junction-to-case)	$R_{\Theta JC}$		TBD		°C /W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$		TBD		°C /W
Thermal Resistance (junction-to-ambient)	$R_{\Theta JA}$		TBD		°C /W
Maximum Soldering Temperature	T_{SOLD}			260	°C

Ordering Information

Part Number	Package Type	Ordering Code	Packing Method	Quantity
EVG100E15B	SMD 0.5 bottom cooled	EVG100E15B	Tube	10 pcs

Electrical Characteristics (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}		100		V	V_{GS} = 0V, I_{DSS} = 50 µA
Drain-to-Source On Resistance	$R_{DS(on)}$	TBD	19	21	mΩ	V_{GS} = 6V, T_J = 25 °C, I_{DS} = 15 A
Drain-to-Source On Resistance	$R_{DS(on)}$		TBD		mΩ	V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 13.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS}, I_D = 7 mA
Gate-to-Source Current	I_{GS}		100		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 80 V, I_D = 45 A
Drain-to-Source Leakage Current	I_{DSS}		0.3		µA	V_{DS} =100 V, V_{GS} = 0 V, T_J = 25°C
Drain-to-Source Leakage Current	I_{DSS}		50		µA	V_{DS} = 100 V, V_{GS} = 0 V, T_J = 150 °C
Internal Gate Resistance	R_G		1.5		Ω	f = 1 MHz, open drain
Input Capacitance	C_{ISS}		TBD		pF	V_{DS} = 80 V, V_{GS} = 0 V, f = 1 MHz
Output Capacitance	C_{OSS}		TBD		pF	
Reverse Transfer Capacitance	C_{RSS}		TBD		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		TBD		pF	V_{GS} = 0 V, V_{DS} = 0 to 100 V
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		TBD		pF	
Total Gate Charge	Q_G		6.2		nC	V_{GS} = 0 to 6V, V_{DS} = 50 V I_{DS}= 45 A
Gate-to-Source Charge	Q_{GS}		2.4		nC	
Gate-to-Drain Charge	Q_{GD}		0.9		nC	
Output Charge	Q_{OSS}		11.5		nC	V_{GS} = 0 V, V_{DS} = 50 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

Electrical Performance Graphs

EVG100E15B I_{DS} vs. V_{DS} Characteristic

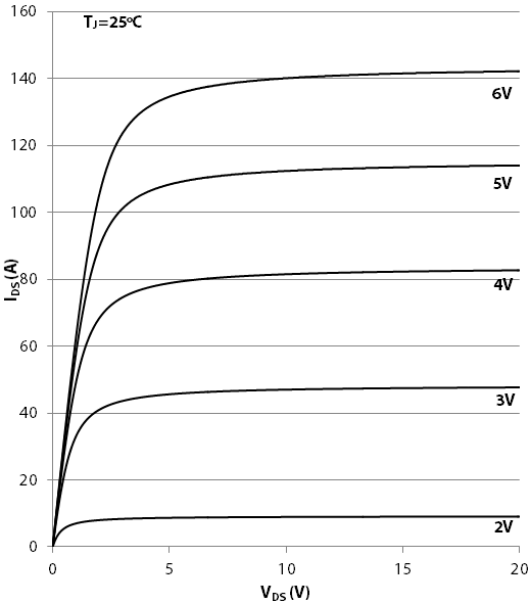


Figure 1 : Typical I_{DS} vs. V_{DS} @ T_J = 25 ºC

EVG100E15B I_{DS} vs. V_{DS} Characteristic

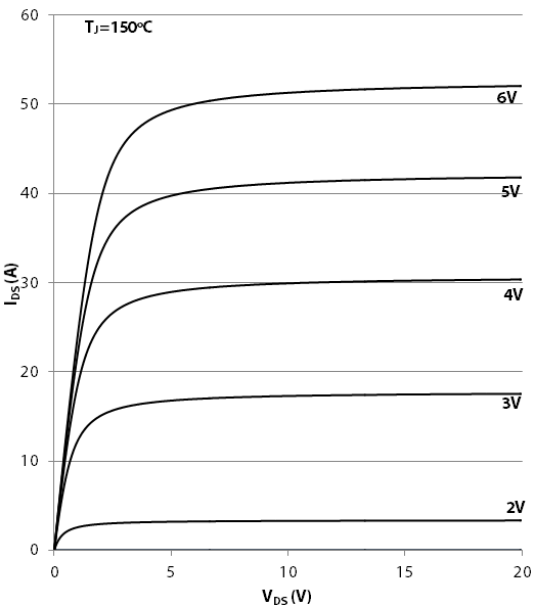


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 ºC

$R_{DS(on)}$ vs. I_{DS} Characteristic

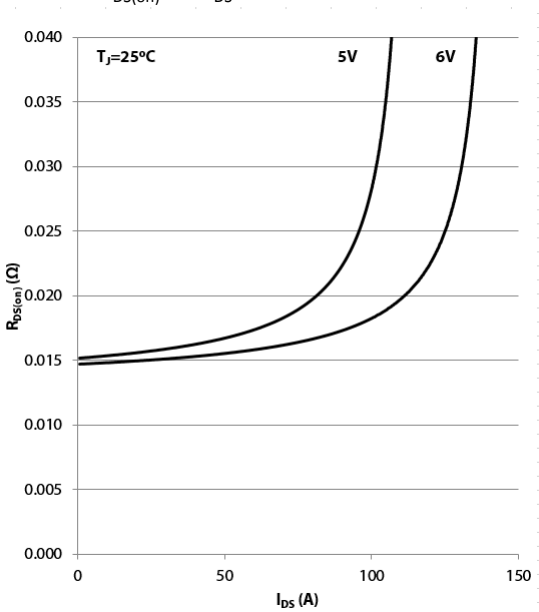


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 ºC

$R_{DS(on)}$ vs. I_{DS} Characteristic

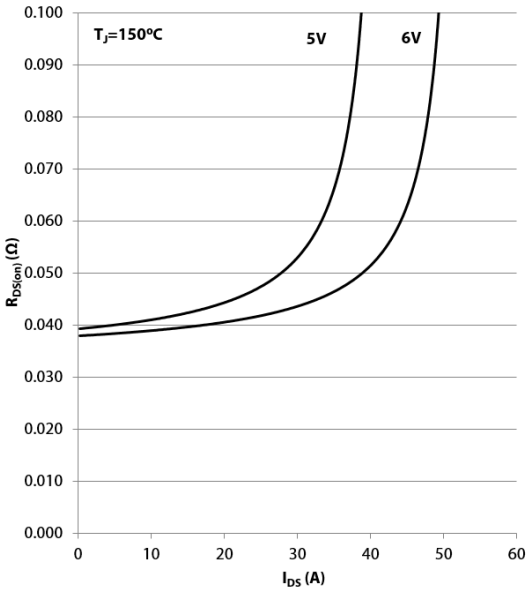


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 ºC

Electrical Performance Graphs

EVG100E15B I_{DS} vs. V_{DS} , T_J dependence

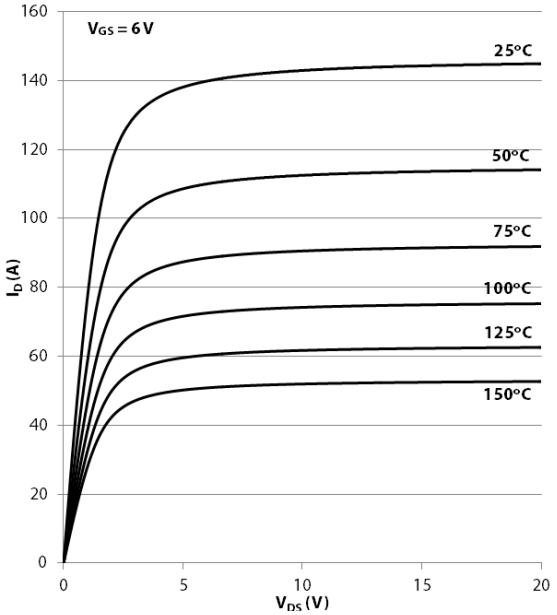


Figure 5 : Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

EVG100E15B Gate Charge, Q_G Characteristic

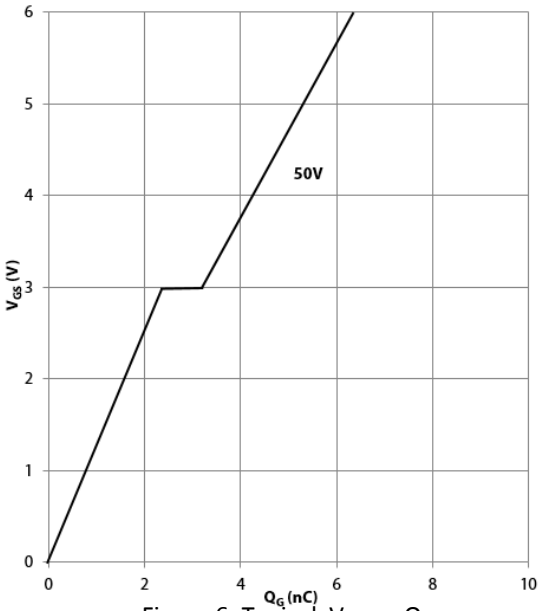


Figure 6: Typical V_{GS} vs. Q_G

EVG100E15B Capacitance Characteristics

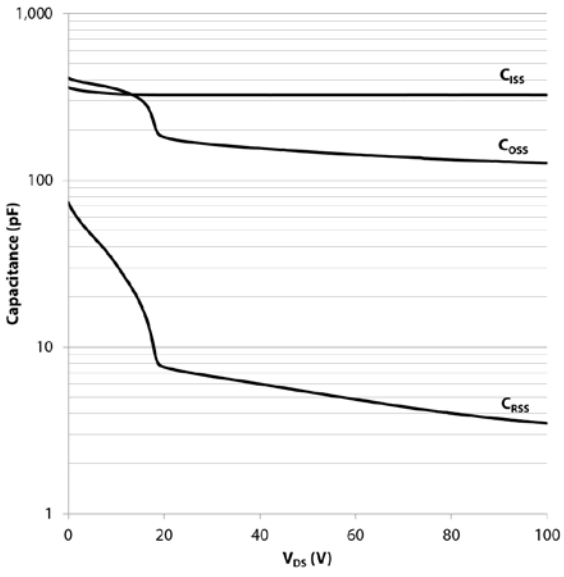


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

EVG100E15B Stored Energy Characteristic

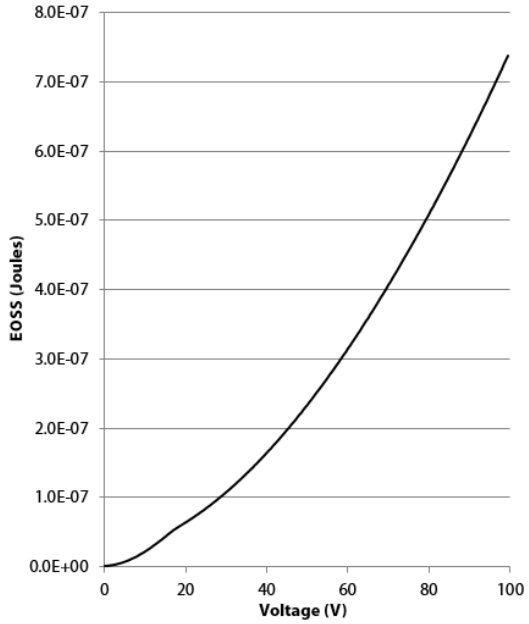


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

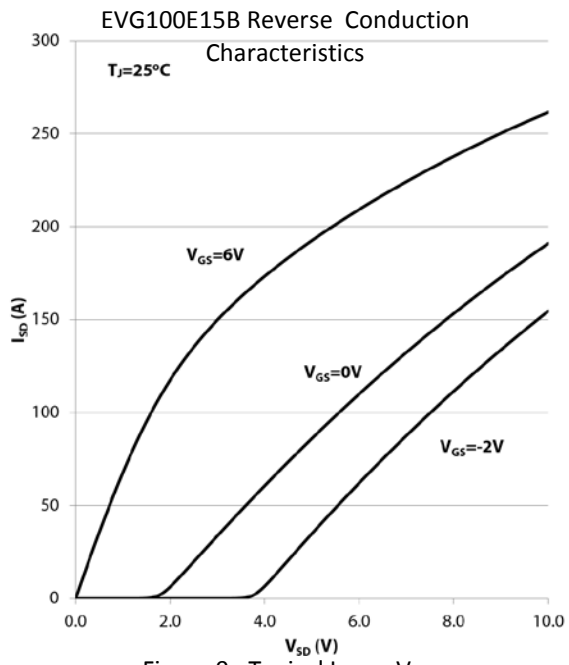


Figure 9 : Typical I_{SD} vs. V_{SD}

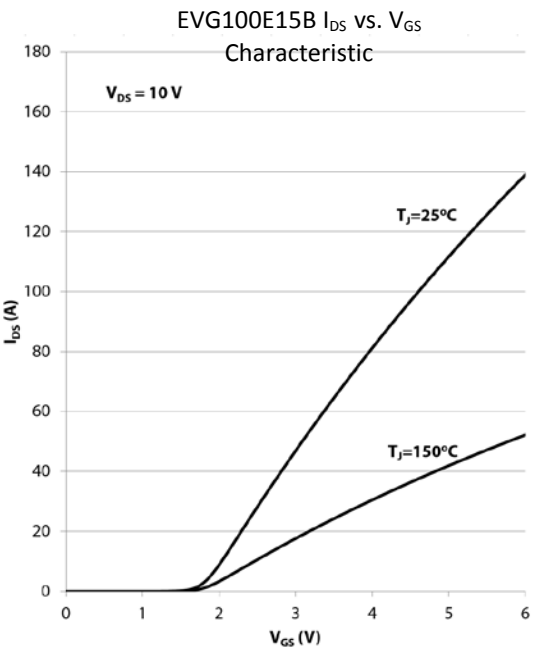


Figure 10 : Typical I_{DS} vs. V_{GS}

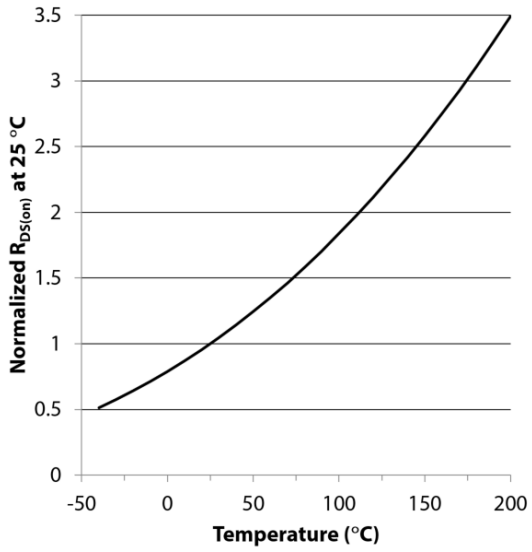


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs

EVG100E15BI$_{DS}$-V$_{DS}$ SOA

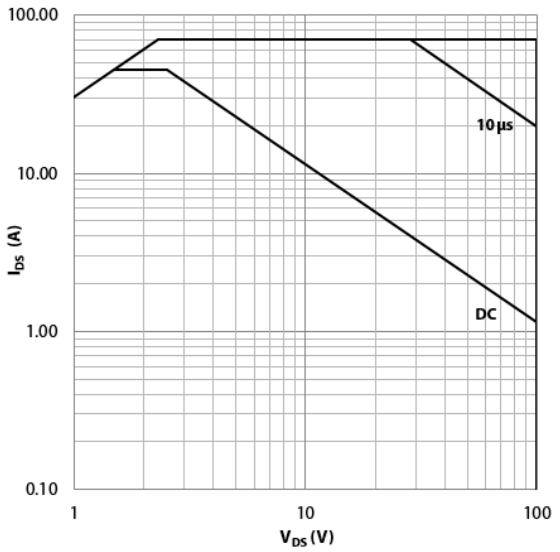


Figure 14: Safe Operating Area @ T_{case} = 25 °C

EVG100E15B Power Dissipation – Temperature Derating

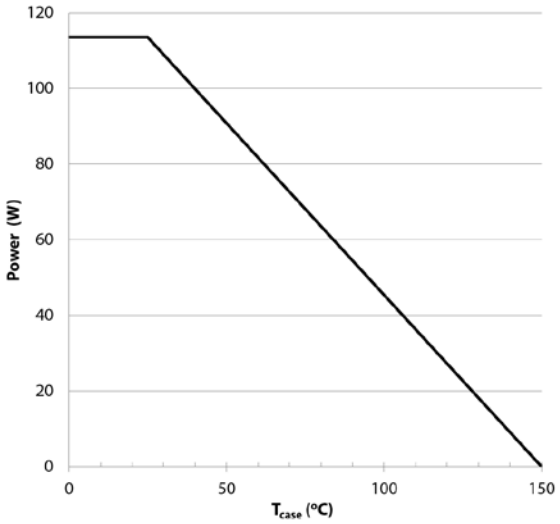


Figure 15: Derating vs. Case Temperature

EVG100E15B Transient $R_{\theta JC}$

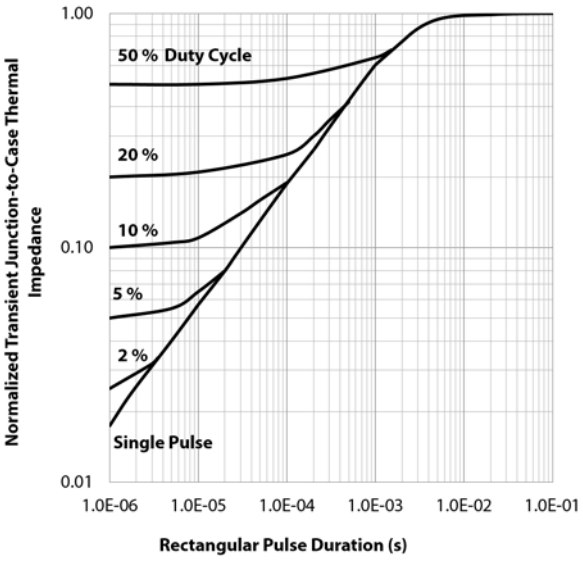


Figure 16: Transient Thermal Impedance

Application Information

Gate Drive

The recommended gate drive voltage for optimal RDS(on) performance and long life is +5 to 6 V. The absolute maximum gate-to-source voltage rating is +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs and duty cycle, D, < 0.1. These specifications allow designers to easily use 5 V-to-6 V, or even 6.5 V gate drive voltage.

A standard MOSFET driver can be used if its UVLO supports 5 V-to-6 V operation for gate drive output. Gate drivers with low output impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower QG when compared to equally sized RDS(on) MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

The dead time period in half bridge applications, should be minimized for optimum efficiency. Choose a 100 V half bridge driver that can support 5 V-to-6 V gate drive and small dead time. The Texas Instruments LM5113 is an example of a half-bridge driver for GaN E-HEMTs. It is recommended to add a voltage clamp circuit (5.1 V or 6.2 V Zener diode for example) in parallel with bootstrap capacitor to limit the bootstrap voltage for high-side switch, if driver does not provide this functionality.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-to-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

Although the EVG100E15B does not have a dedicated source sense pin, the packaging utilizes no wire bonds so the source connection is very low inductance directly connected to the power pad. By simply using a dedicated “source sense” connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a “source sense” connection to improve drive performance.

Thermal

The substrate is internally connected to the thermal pad and to the source pad on the bottom side of the EVG100E15B. The transistor is designed to be cooled using the printed circuit board.

Reverse Conduction

GaN Systems HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending upon the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors, as is the case for IGBTs, to achieve reverse conduction performance.

On-state condition (VGS = +6 V): The reverse conduction characteristics is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, RDS(on), similar to forward conduction operation.

Off-state condition (VGS ≤ 0 V): The reverse characteristics in the off-sate are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, (VGD) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher VF and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than VGS(th)+VGS(off) in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “VF” and hence increase the reverse conduction loss.

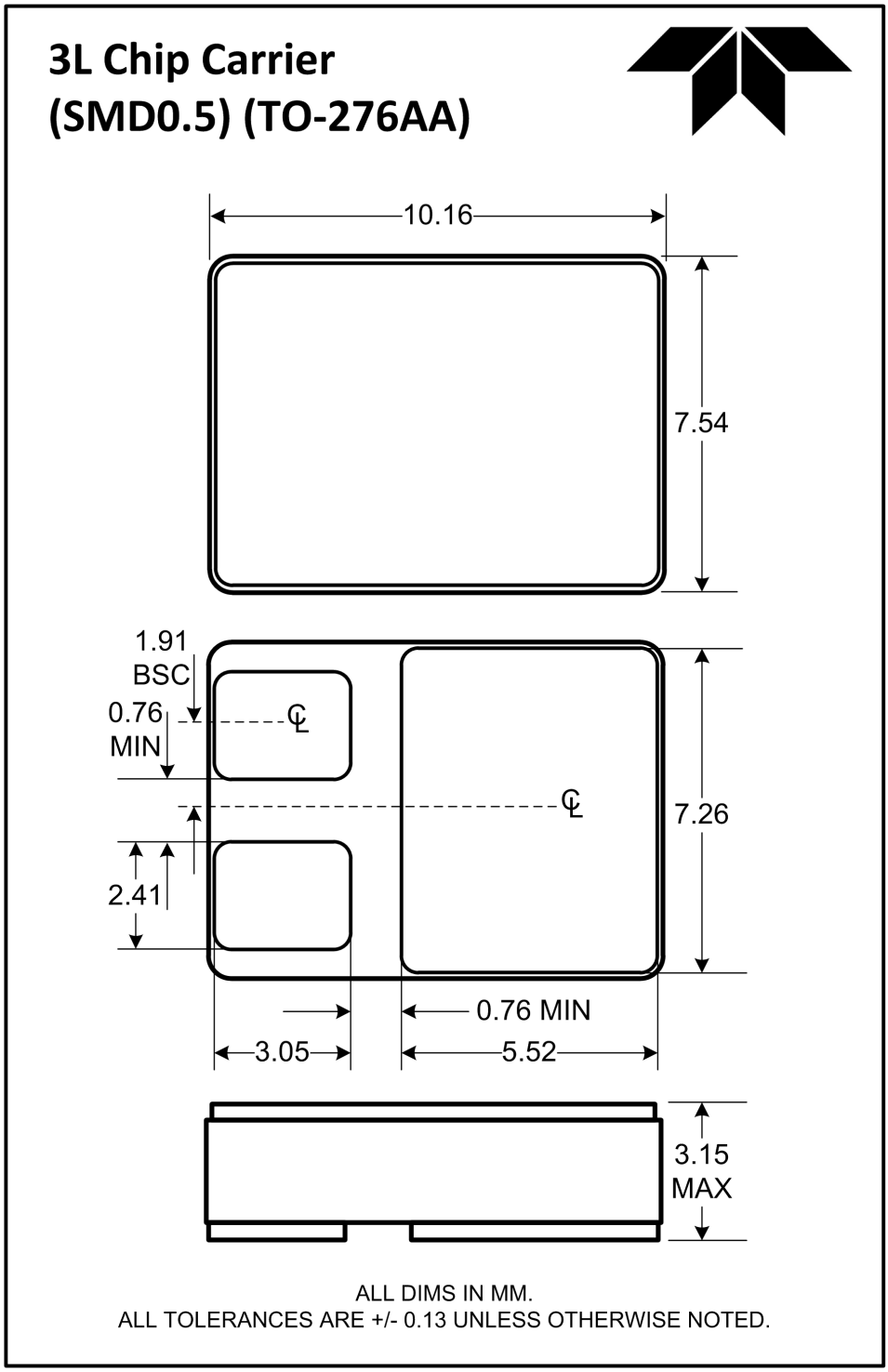
Blocking Voltage

The blocking voltage rating, BVDS, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated BVDS. As a general practice, the maximum drain voltage should be de-rated in a similar manner as silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating.

The absolute maximum drain-to-source rating is 100 V and doesn’t change with negative gate voltage.

Packaging and Soldering
TBD

Package Dimensions



Ordering Information

TBD