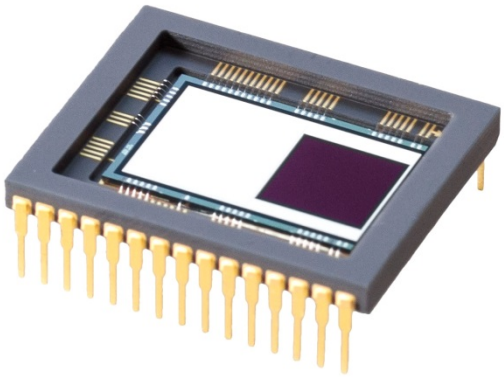
CCD97-00 Datasheet
Electron Multiplying CCD Sensor
Back Illuminated, 512 x 512 pixels
2-Phase IMO

MAIN FEATURES

- 512 x 512 active pixels
- 16µm square pixels
- Variable multiplicative gain
- Additional conventional output amplifier
- Inverted mode operation for low dark current.
- 30-pin ceramic dual-in-line package



OVERVIEW

The CCD97 is a frame transfer, electron multiplying CCD sensor designed for extreme performance in high frame rate ultra-low light applications. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by the Large Signal Output amplifier (OSL).

The device can also be read out without using the gain register via the High Responsivity Output amplifier (OSH).

The multiplication gain in the readout chain allows L3Vision devices to effectively eliminate readout noise. The gain may be varied from 1x to over 1000x by adjustment of the multiplication phase amplitude RØ2HV.

GENERAL DATA

Image section	512 x 512
Pixel size	16 µm × 16 µm
Active image area	8.19 × 8.19 mm
Package size	22.86 × 28.00 mm
Typical amplifier responsivity	5.3 µV/e^- (OSH) 1.1 µV/e^- (OSL)
Typical readout noise 1MHz at 1000x Gain 50kHz using OSH amp.	 <1e^- 2.2e^-
Max output data rate	15 MHz
Typical pixel charge capacity	130 ke^-/pixel
Typical dark signal (20°C)	400 e^-/pixel/s

ORDERING INFORMATION

CCD97-00-G-XYZ
G = cosmetic grade
XYZ = specific variant type (e.g. AR coating)
e.g. XYZ = 095 for basic process with midband coating
e.g. XYZ = S28 for no OSH amplifier variant.

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IMAGING PERFORMANCE

ELECTRO-OPTICAL PERFORMANCE

Except where otherwise specified, the following are measured at 18°C at a pixel rate of 11 MHz, with typical operating voltages. For the S28 variant, the parameters relating to the OSH amplifier do not apply; all other parameters are unchanged.

Parameter	Min	Typical	Max	Units	Notes
Output amplifier responsivity, OSH amplifier	-	5.3	-	μV/e⁻	Note 1
Output amplifier responsivity, OSL amplifier	-	1.1	-	μV/e⁻	Note 1, Note 2
Multiplication register gain, OSL amplifier	1	-	1000		Note 3
Peak signal - 2-phase IMO	90k	130k	-	e⁻/pixel	Note 4
Charge handling capacity of multiplication register	-	800k	-	e⁻/pixel	Note 5
Readout noise at 50 kHz with CDS, OSH amplifier	-	2.2	-	e⁻ rms	Note 6
Readout noise at 1 MHz with CDS, OSH amplifier	-	5.4	-	e⁻ rms	Note 6
Amplifier reset noise (without CDS), OSH amplifier	-	50	-	e⁻ rms	Note 6
Readout noise at 50 kHz with CDS, OSL amplifier	-	6	-	e⁻ rms	Note 2, Note 6
Readout noise at 15 MHz with CDS, OSL amplifier	-	14	-	e⁻ rms	Note 2, Note 6
Amplifier reset noise (without CDS), OSL amplifier	-	120	-	e⁻ rms	Note 2, Note 6
Readout noise at 1 MHz and 1000X gain	-	<1	-	e⁻ rms	Note 6
Maximum frequency (settling to 1%), OSH amplifier	-	-	3	MHz	Note 6, Note 7
Maximum frequency (settling to 5%), OSH amplifier	-	-	4.5	MHz	Note 6, Note 7
Maximum frequency (settling to 1%), OSL amplifier	-	-	9	MHz	Note 6, Note 7
Maximum frequency (settling to 5%), OSL amplifier	-	-	15	MHz	Note 6, Note 7
Maximum parallel transfer frequency	-	1.6	-	MHz	Note 1
Dark signal equivalent at 20°C	-	400	800	e⁻/pixel/s	Note 8, Note 9
Dark signal non-uniformity (DSNU) equivalent at 20°C	-	60	-	e⁻/pixel/s	Note 10
Excess noise factor	-	√2	-		Note 11

Notes

Note 1. Measured at a pixel rate of 1 MHz.

Note 2. No EM gain applied.

Note 3. Some increase of RØ2HV may be required throughout life to maintain gain performance.

Note 4. For shielded anti-blooming variants, the peak signal is reduced to approx. 90k e⁻ typical and 65k e⁻ min.

Note 5. When multiplicative gain is used, a linear response is achieved for output signals up to 400 ke⁻

Note 6. Values are inferred from design

Note 7. The quoted maximum frequencies assume a 20 pF load and correlated double sampling (CDS) are being implemented. If instead a single sampling is used, the output will be settled to 1% at 15 MHz typically.

Note 8. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a significant component generated during readout through the non-inverted mode register.

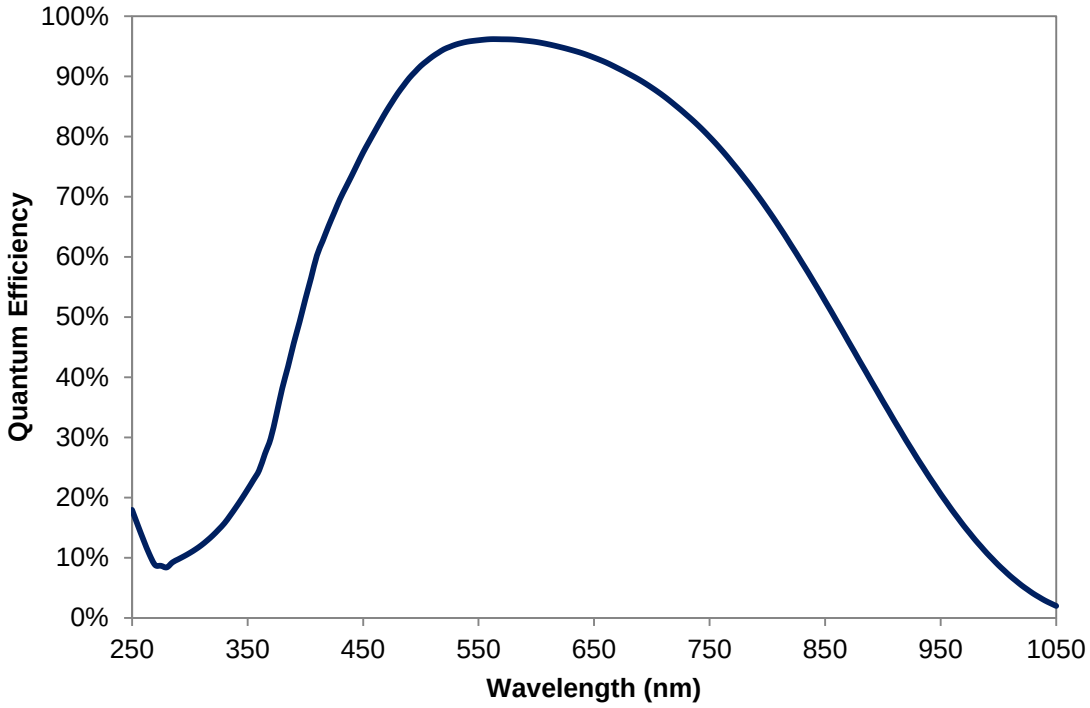
There exists a further weakly temperature dependant component, the clock induced charge (CIC), which is independent of integration time. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".

Note 9. For fringe suppression variants, the dark signal will be higher (typical and maximum are 600 and 900 e⁻/pixel/s respectively)

Note 10. DSNU is defined as the 1σ variation of the dark signal

Note 11. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

FIGURE 1: TYPICAL SPECTRAL RESPONSE (At -20°C, no window, basic process, standard thickness, midband coating) (Not measured)



Devices can be supplied with alternative anti-reflection coatings optimised for different wavelengths – details from Teledyne e2v.

For shielded anti-blooming variants, the quantum efficiency will be slightly reduced up to a maximum relative reduction of 10% at NIR wavelengths.

FIGURE 2: TYPICAL VARIATION OF MULTIPLICATIVE GAIN WITH RØ2HV MINUS RØDC

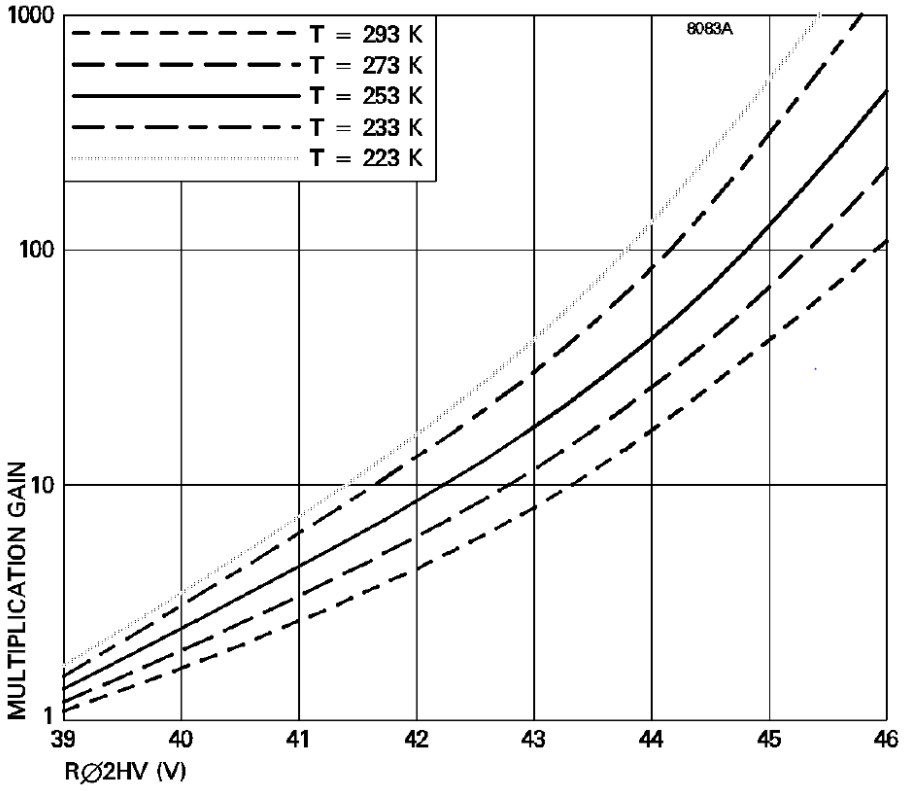
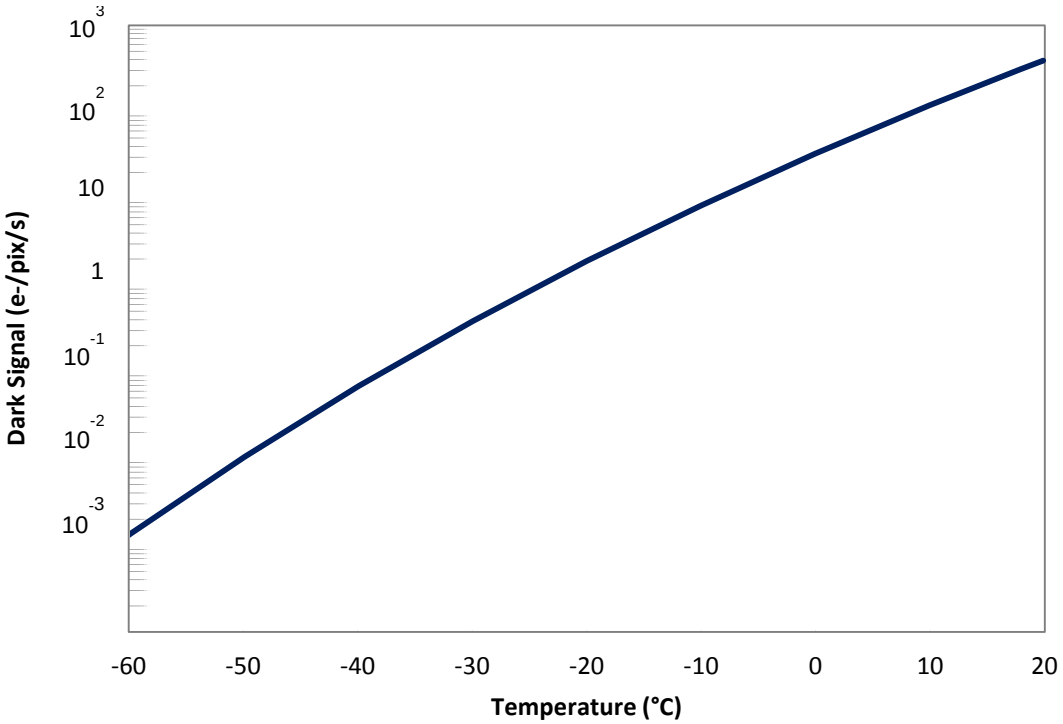


FIGURE 3: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

Dark signal is a strong function of temperature and the typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by $Q_d/Q_{do} = 1.14 \times 10^6 T^3 e^{-9080/T}$ where Q_{do} is the dark current at 293 K.



DEFECT DEFINITIONS

All cosmetic tests are performed at 18 ± 3ºC in 2-phase inverted mode at 11MHz.

SPECIFICATION

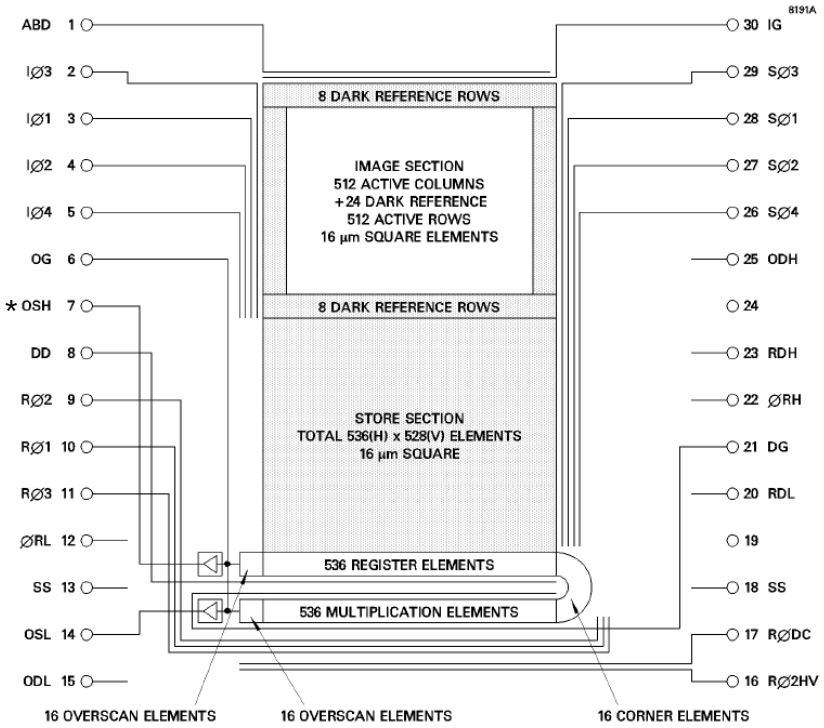
Parameter	Grade 1	Definition
White Defects	10	White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum dark signal level.
White Columns	0	A white column contains at least 9 white defects.
Black/Pin-head Columns	0	Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified gain and level of illumination. A black column contains at least 9 black defects. Pin-head columns are manifest as a partial dark column with a bright pixel showing photo-response at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

Grade 5 devices are functional but with an image quality below grade 1. Other specifications may also not be met or may not have been tested.

Incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

DEVICE DESCRIPTION

FIGURE 4: DEVICE ARCHITECTURE



* Pin 7 has no connection for S28 variant

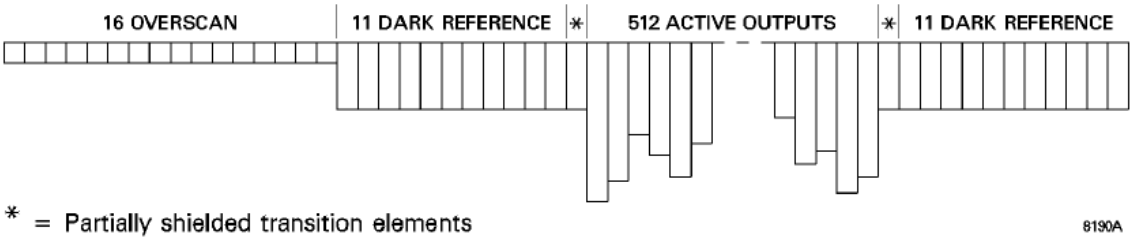
The rows and colums immediately adjacent to the active image area may be only partially shielded, i.e. transition elements, and should not be used for reference purposes.

The electrodes of the image and store sections are configured for four-phase clocking, but adjacent phases need to be joined off chip to run in two phase operation.

The multiplication register requires two extra drive phases, RØDC and RØ2HV.

There is a dump drain DD below the 536 register elements adjacent to the store section with the charge dumping operation controlled by the dump gate DG.

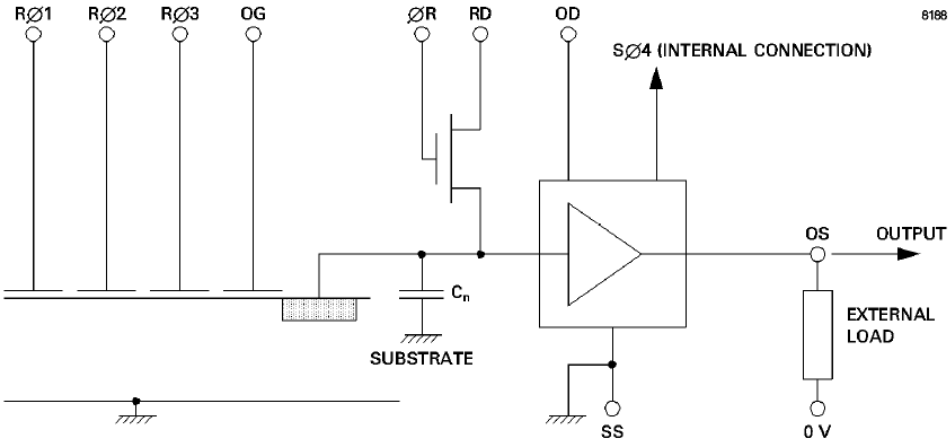
FIGURE 5: LINE OUTPUT FORMAT



Notes

Note 12. There will be a one row propagation delay between transferring a row from the store section to the conventional register and then reading it out through the CCD output.

FIGURE 6: OUTPUT CIRCUIT SCHEMATIC (OSL and OSH Amplifiers)



The amplifiers have a DC restoration circuit that is internally activated whenever SØ4 is high.

Nominal Design Features (Not measured)

Feature	OSH	OSL
Output	OSH (pin 15)	OSL (pin 16)
External load	5 kΩ or 5 mA	5 kΩ or 5 mA
Output impedance	250 Ω	350 Ω
On-chip dissipation	30 mW	40 mW

ELECTRICAL PERFORMANCE

PIN DESCRIPTIONS

The table below gives the pin connections, functions and maximum ratings with respect to the substrate (SS).

Pin	Ref	Function	Min (V)	Max (V)	Ref	Function	Min (V)	Max (V)	Pin
1	ABD	Anti-blooming drain	-0.3	+25	IG	Isolation gate	-20	+20	**30**
2	IØ3	Image section clock phase 3	-20	+20	SØ3	Store section clock phase 3	-20	+20	**29**
3	IØ1	Image section clock phase 1	-20	+20	SØ1	Store section clock phase 1	-20	+20	**28**
4	IØ2	Image section clock phase 2	-20	+20	SØ2	Store section clock phase 2	-20	+20	**27**
5	IØ4	Image section clock phase 4	-20	+20	SØ4	Store section clock phase 4	-20	+20	**26**
6	OG	Output gate	-20	+20	ODH	Output drain high	-0.3	+25	**25**
7	OSH*	Output source high	-0.3	+25	n.c.	No connection	-		**24**
8	DD	Dump drain	-0.3	+25	RDH	Reset drain high	-0.3	+25	**23**
9	RØ2	Register clock phase 2	-20	+20	ØR	Output reset pulse high	-20	+20	**22**
10	RØ1	Register clock phase 1	-20	+20	DG	Dump gate	-20	+20	**21**
11	RØ3	Register clock phase 3	-20	+20	RDL	Reset drain low	-0.3	+25	**20**
12	ØRL	Output reset pulse low	-20	+20	n.c.	No connection	-		**19**
13	SS	Substrate	0		SS	Substrate	0		**18**
14	OSL	Output source low	-0.3	+25	RØDC	Register DC phase	-20	+20	**17**
15	ODL	Output drain low	-0.3	+32	RØ2HV	Register clock phase 2 HV	-20	+50	**16**

* Pin 7 is n.c. no connection for S28 variantThe ABD pin is used for connection purposes and must be biased as specified even for non-anti-blooming variants.

Maximum Voltage Between Pairs

Pin	Ref	Pin	Ref	Min (V)	Max (V)
7	OSH	**25**	ODH	-15	+15
14	OSL	**15**	ODL	-15	+15
16	RØ2HV	**17**	RØDC	-20	+50
16	RØ2HV	**11**	RØ3	-20	+50
Output Transistor Current (mA)					20

Permanent damage may result if, in operation, OSL or OSH experiences short-circuit conditions.

OPERATING VOLTAGES

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

Connection	Description	Phase Amplitude or DC level (V)			Notes
		Min	Typical	Max	
IØ1, 2, 3, 4 high	Image section: clock high	+5	+7	+9	Note 13
IØ1, 2, 3, 4 low	Image section: clock low	-6	-5	-4	
SØ1, 2, 3, 4 high	Store section: clock high	+5	+7	+9	Note 13
SØ1, 2, 3, 4 low	Store section: clock low	-6	-5	-4	
RØ1, 2, 3 high	Register: clock high	+8	+12	+13	
RØ1, 2, 3 low	Register: clock low	-	0	-	
RØ2HV high	Register HV phase high	+20	+40	+50	Note 3
RØ2HV low	Register HV phase low	0	+4	+5	
ØR high	Reset clock high	-	+10	-	Note 14
ØR low	Reset clock low	-	0	-	
RØDC	Register DC phase	+2	+3	+5	
OG	Output gate voltage	+1	+3	+5	Note 15
IG	Isolation gate voltage	-	-5	-	
SS	Substrate	0	+4.5	+7	
ODL, ODH	Output drain	+25	+28	+32	
RD	Reset drain voltage	+15	+17	+20	
ABD	Anti-blooming Drain	+10	+18	+20	
DG high	Dump gate high	-	0	-	
DG low	Dump gate low	+10	+12	+13	
DD	Dump drain	+20	+24	+25	

Notes

Note 13. IØ and SØ adjustment may be common. The high level may need to be adjusted to achieve correct charge transfer and the low level may need to be separately adjusted to achieve correct inverted mode operation that is uniform across the array.

Note 14. ØRL and ØRH high level may be adjusted in common with RØ1, 2, 3.

Note 15. Other than the output gates (OG), there are no common connections made between the two amplifiers, and either can be powered down by connecting the appropriate output drain (OD) connection to the substrate (SS). The reset drains (RD) should remain biased, with the reset gate (ØR) clocked normally or held at clock low level.

ELECTRICAL INTERFACE CHARACTERISTICS (Not measured)

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS				
Connection	**Capacitance to SS**	**Inter-phase Capacitance**	**Total Capacitance**	**Units**
IØ1	3.7	1.6	5.3	nF
IØ2	1.6	1.6	3.2	nF
IØ3	3.7	1.6	5.3	nF
IØ4	1.6	1.6	3.2	nF
SØ1	3.7	1.6	5.3	nF
SØ2	1.6	1.6	3.2	nF
SØ3	3.7	1.6	5.3	nF
SØ4	1.6	1.6	3.2	nF
RØ1	50	65	115	pF
RØ2	32	43	75	pF
RØ3	62	63	125	pF
RØ2HV	28	37	65	pF

SERIES RESISTANCES		
Connection	**Approximate Total Series Resistance**	**Units**
IØ1	17	Ω
IØ2	17	Ω
IØ3	17	Ω
IØ4	17	Ω
SØ1	17	Ω
SØ2	17	Ω
SØ3	17	Ω
SØ4	17	Ω
RØ1	6	Ω
RØ2	6	Ω
RØ3	6	Ω
RØ2HV	2	Ω

TIMING

CLOCK TIMING REQUIREMENTS

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases Ø1 and Ø2, and phases Ø3 and Ø4 of the image and store sections. Suggested timing diagrams are shown in Figs. 4-11.

The following are suggested pulse rise and fall times:

Clock Pulse	Typical Rise Time τ (ns)	Typical Fall Time τ (ns)	Typical Pulse Overlap
IØ	120 < τ <200	120 < τ <200	@90% points
SØ	120 < τ <200	120 < τ <200	@90% points
RØ1	10	10	@70% points
RØ2	10	10	@70% points
RØ3	10	10	@70% points
RØ2HV	25	25	See Note 16
RØ2HV	Sine	Sine	Sinusoid – high on falling edge of RØ1

Notes

Note 16. RØ2HV can be operated with a normal clock pulse, as shown in Fig. 6. Alternatively a sinusoidal clocking scheme is shown in Fig. 5. The requirement for successful clocking is that RØ2HV reaches its maximum amplitude before RØ1 goes low.

FIGURE 7: CLOCKING SCHEME FOR 2-PHASE INVERTED MODE OPERATION

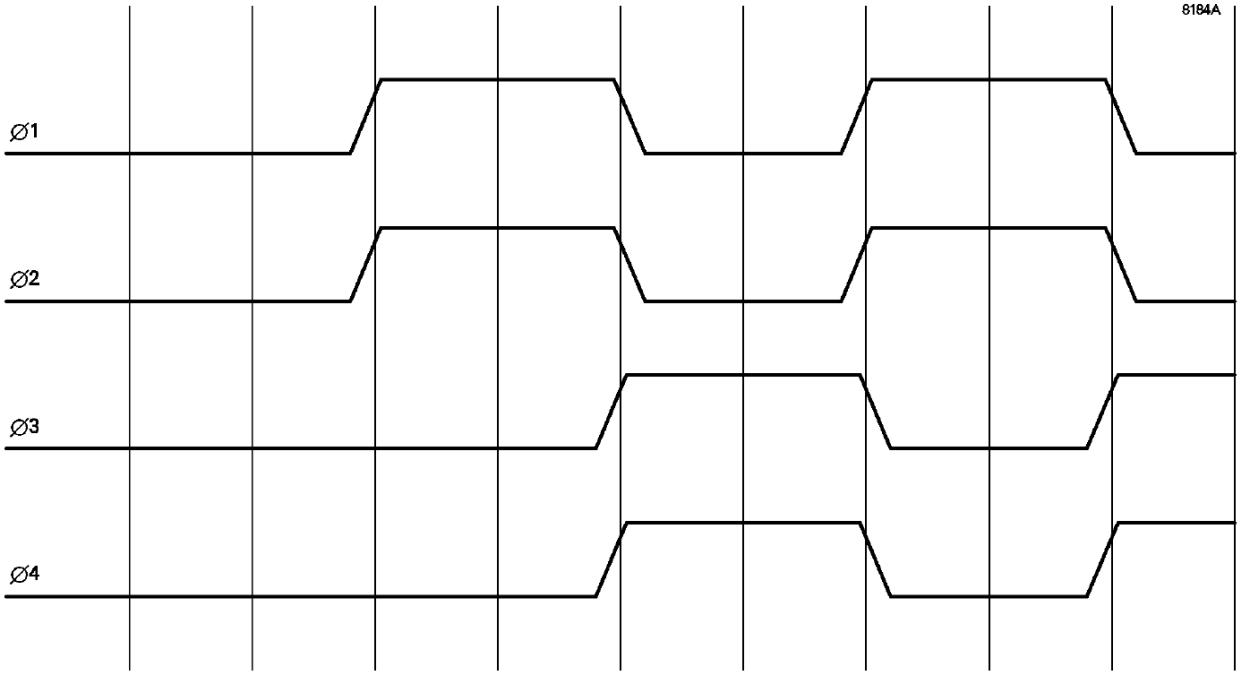


FIGURE 8: CLOCKING SCHEME FOR MULTIPLICATION GAIN

(Sinusoidal Clocking Scheme, see Note 17, used for factory testing)

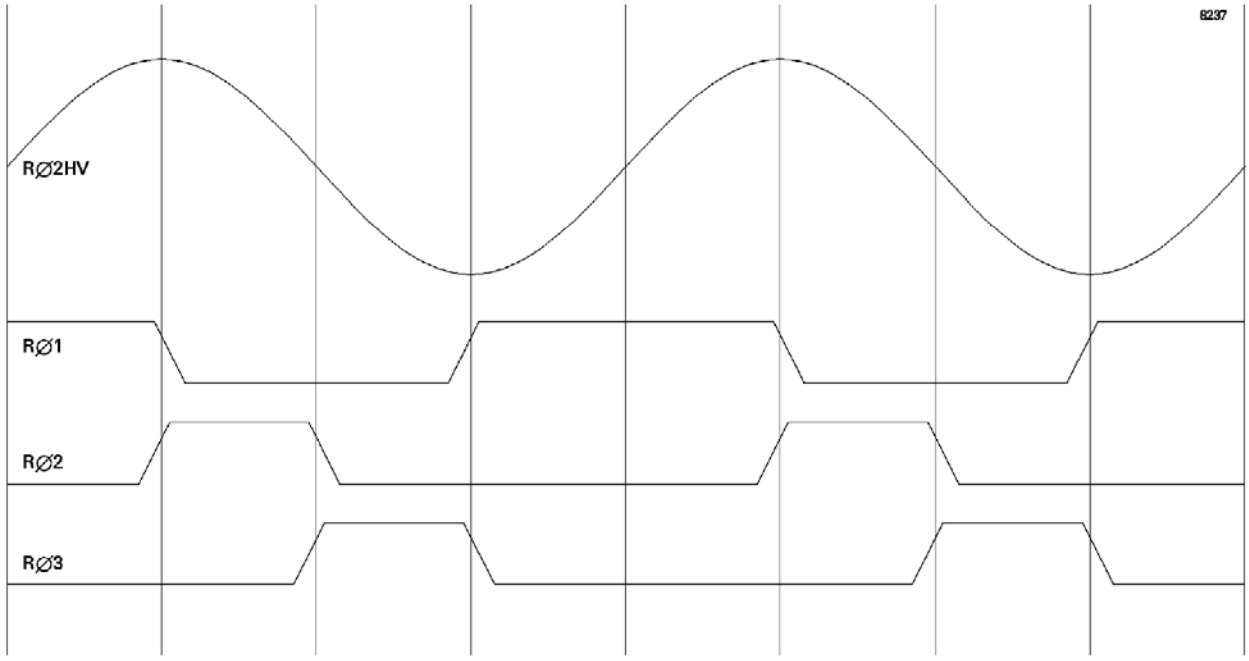
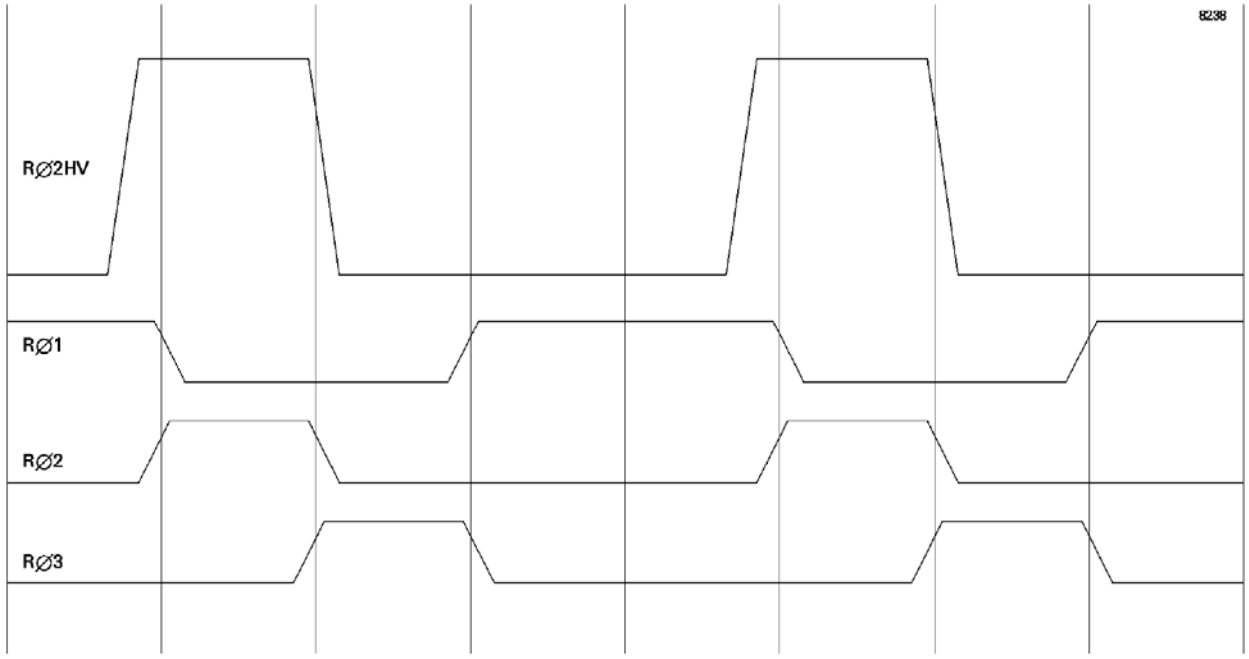


FIGURE 9: CLOCKING SCHEME FOR MULTIPLICATION GAIN

(Trapezoidal Clocking Scheme, see Note 17, not used in factory testing)

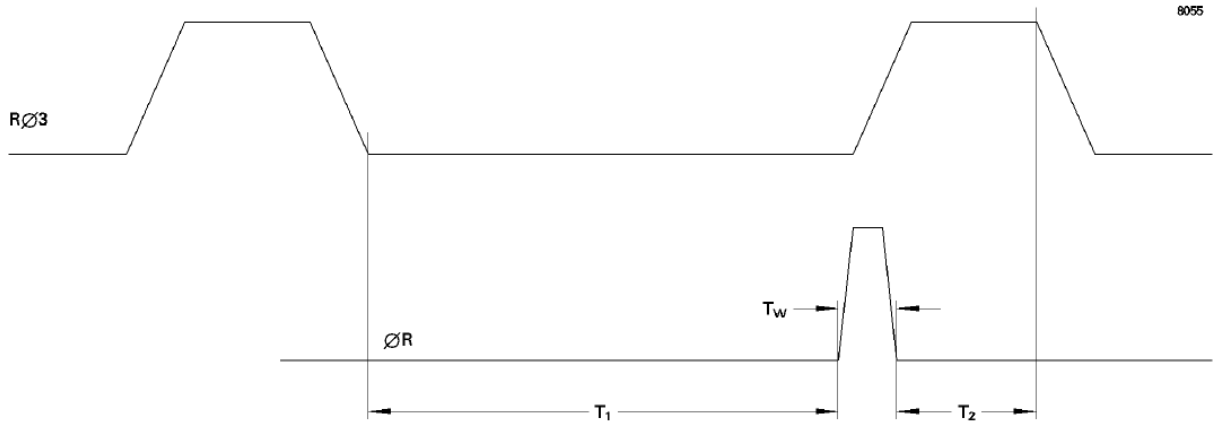


Notes

Note 17. To operate through the OSH output amplifier, the RØ1 and RØ2 waveforms should be interchanged.

PULSE TIMINGS AND OVERLAPS

FIGURE 10: RESET PULSE



T_W = 10 ns typical
T_1 = output valid
T_2 > 0 ns

FIGURE 11: PULSE AND OUTPUT TIMING

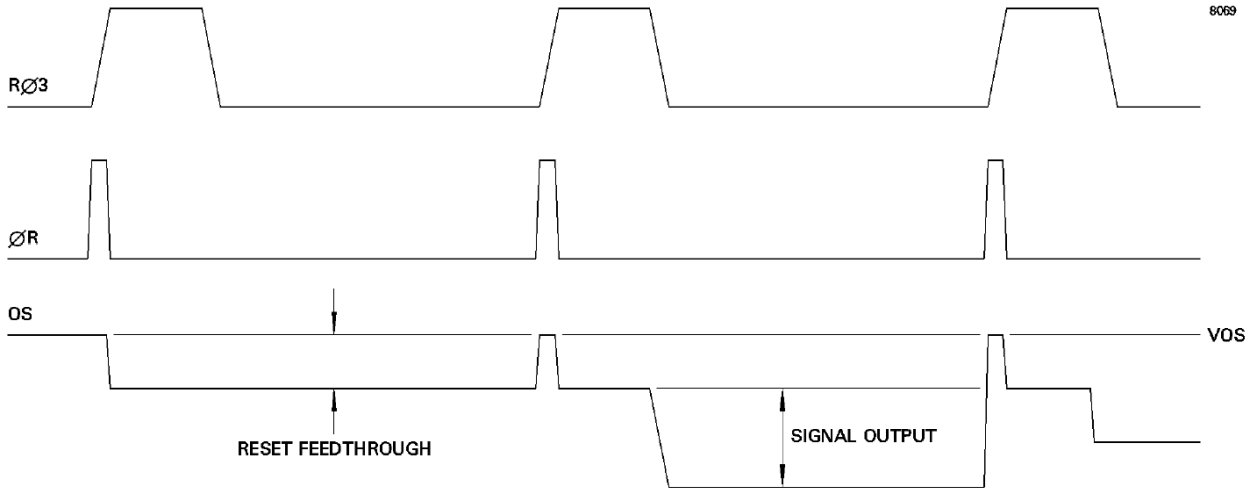


FIGURE 12: EXAMPLE FRAME TIMING DIAGRAM

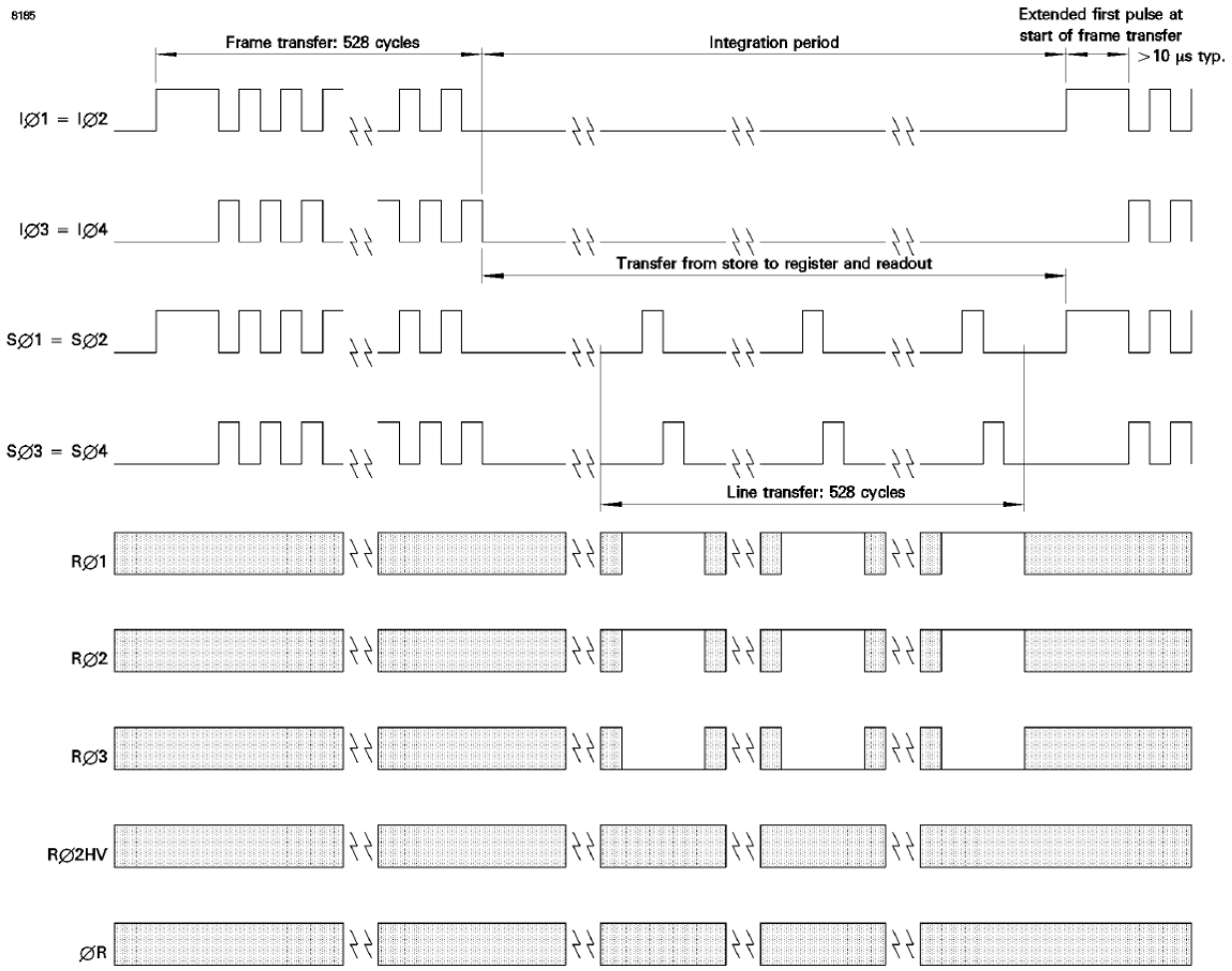


FIGURE 13: EXAMPLE LINE TIMING DIAGRAM

(Operation through OSL, see Note 12 and Note 17)

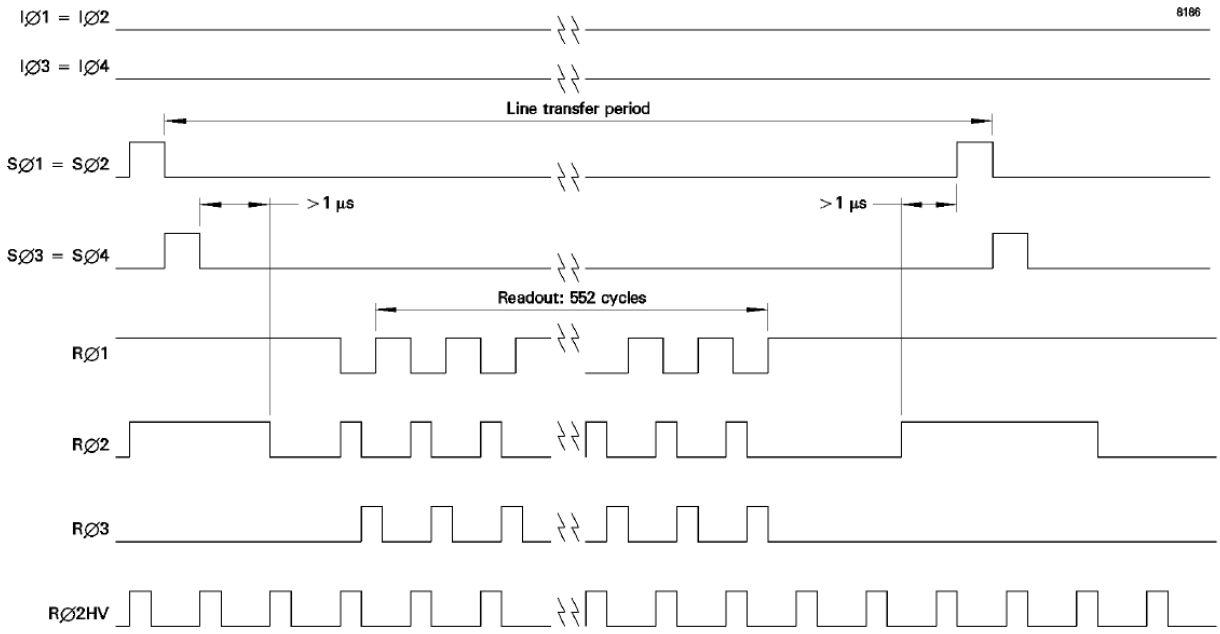
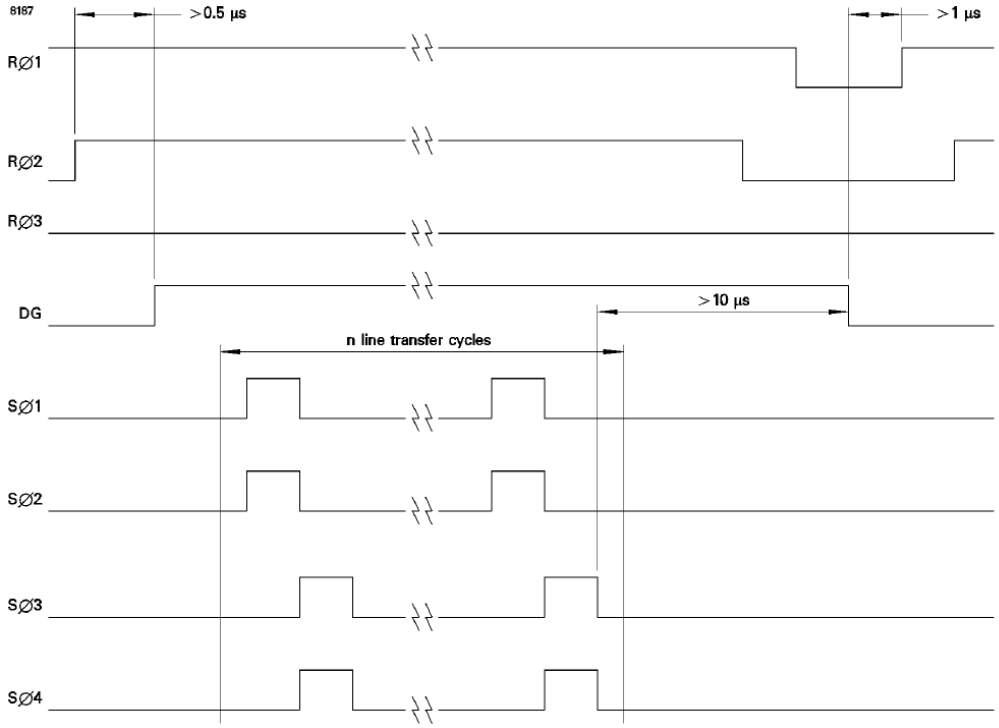


FIGURE 14: OPERATION OF THE DUMP GATE TO DUMP n LINES OF UNWANTED DATA FROM THE STANDARD REGISTER



Wanted lines of data must be completely read out before dumping unwanted data.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Furthermore, unlike most Teledyne e2v devices, the CCD97 is NOT provided with anti-static protection devices on all gate connections – during operation RØ2HV requires a high voltage peak amplitude for gain multiplication that is not compatible with standard gate protection structures. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be grounded

Evidence of incorrect handling will invalidate the warranty.

The devices are assembled in a clean room environment and Teledyne e2v recommend that similar precautions are taken by the user to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at Teledyne e2v with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

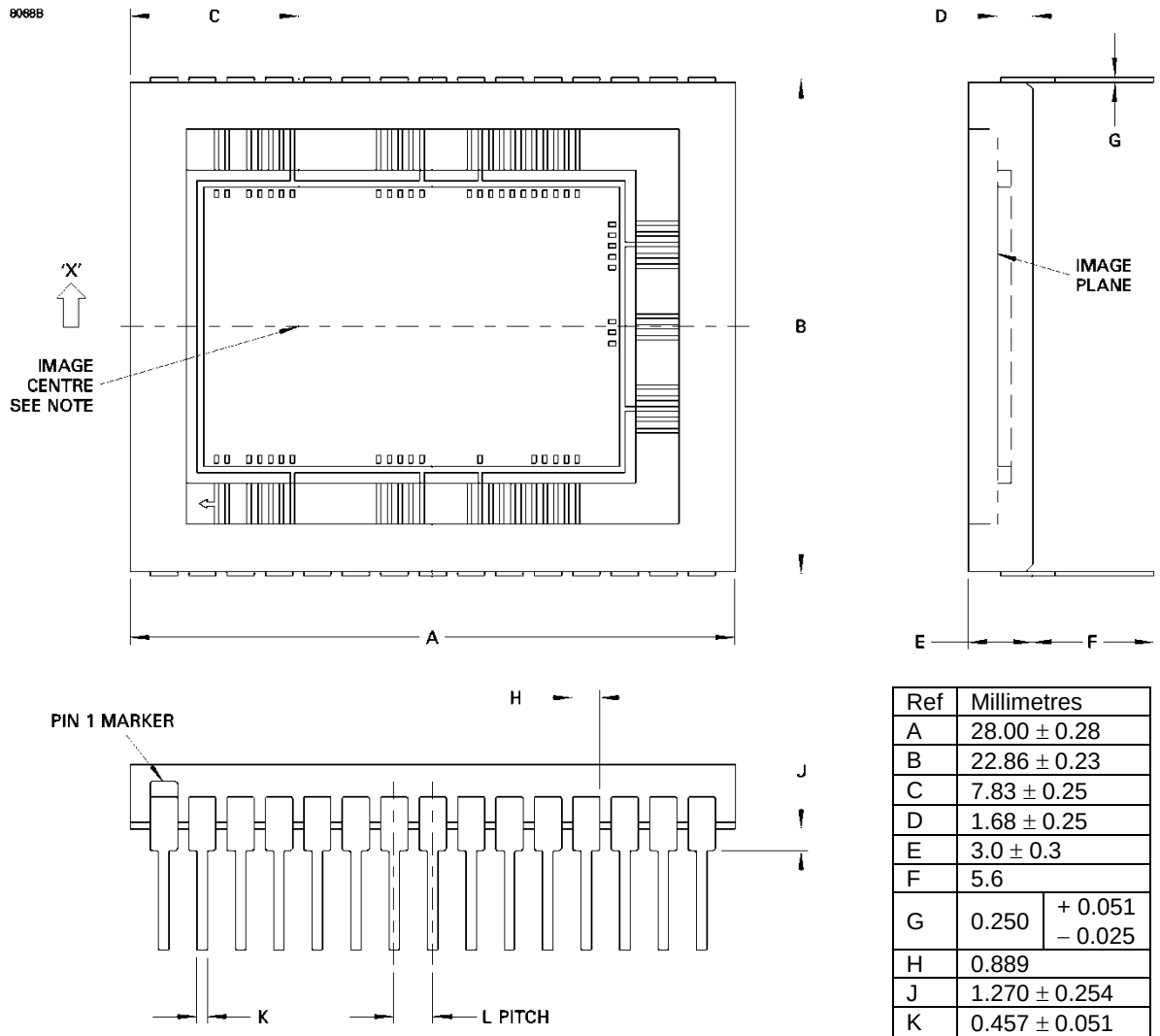
TEMPERATURE RANGES

Component	Min	Max
Operating Temperature	-120°C	+75°C
Non-Operating Temperature	-200°C	+100°C
Rate of change		5°C/min

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage. Full performance is only guaranteed at the nominal operating temperature of 18°C.

GEOMETRY

FIGURE 15: PACKAGE OUTLINE (Tolerances are by design and not verified on each part)



Ref	Millimetres	
A	28.00 ± 0.28	
B	22.86 ± 0.23	
C	7.83 ± 0.25	
D	1.68 ± 0.25	
E	3.0 ± 0.3	
F	5.6	
G	0.250	+ 0.051 – 0.025
H	0.889	
J	1.270 ± 0.254	
K	0.457 ± 0.051	
L	1.778 ± 0.130	

The image centre is aligned centrally in the package in direction 'X', to within a tolerance of ±0.20mm.