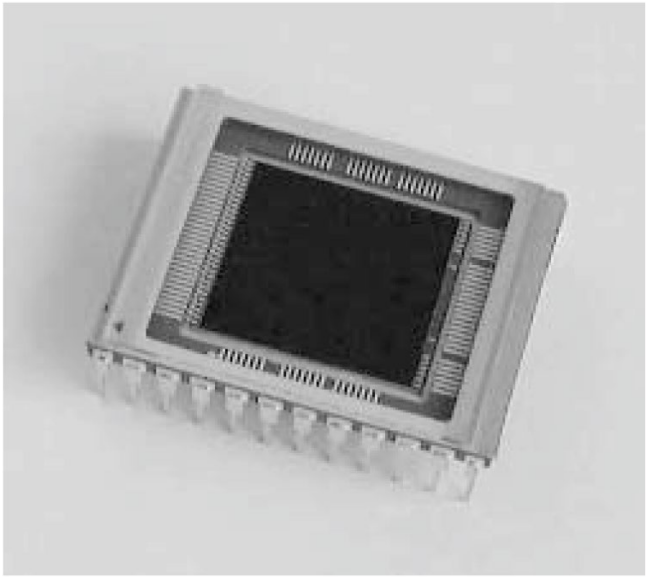
CCD77-00 Back Illuminated High Performance IMO Device

FEATURES

- 512 x 512
- Image Format
- Image Area 12.3 x 12.3 mm
- Full-Frame Operation
- 24 µm Square Pixels
- Back Illuminated for High Quantum Efficiency
- Low Noise Output Amplifiers
- 100% Active Area
- Inverted Mode Operation



APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION

The CCD77 family of sensors are full-frame devices with readout registers above and below the image section. The top register, image section and bottom register are designated A, B and C respectively. Each register has a single output at one end and a charge injection structure at the other end for test purposes.

Standard three-phase clocking and buried channel charge transfer are employed . The image section of the device operates in inverted mode for minimum dark current. To maximise the dynamic range, the CCD is manufactured without anti-blooming structures.

The e2v technologies back thinning process ensures high quantum efficiency over a wide range of wavelengths. Several different anti -reflection coatings are available to suit a range of applications. Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE

Maximum readout frequency	7MHz
Output Responsivity	2.5µV/e^-
Peak Signal	300ke^-/pixel
Dynamic Range (at 20kHz)	100 000:1
Spectral range	200 – 106 nm
Readout noise (at 20kHz)	3.0 e^- rms

GENERAL DATA

Format

Image area	12.3 x x12.3 mm
Active pixels(H)	512
(V)	512
Pixel size	24 x 24 µm
Number of output amplifiers	2

15 additional pixels are provided for over-scanning purposes in each register

PACKAGE

Package size 22.6 x 29.9
Number of pins 24
Inter-pin spacing 2.54 mm
Inter-row spacing 22.86 mm
Window material removable glass
Type ceramic DIL array
Weight (approx, no window) 6 g

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	300k	350k	-	e^-/pixel
Peak output voltage (no binning)	-	875	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	700	1500	e^-/pixel/s
Dynamic range (see note 4)	-	100 000:1	-	
Charge transfer efficiency (see note 5): parallel serial	 - -	 99.9999 99.9993	 - -	 % %
Output amplifier responsivity (see note 3)	1.8	2.5	3.5	$\mu V/e^-$
Readout noise at 253 K (see notes 3 and 6)	-	3.0	5.0	rms e^-/pixel
Maximum readout frequency (see note 7)	-	1000	7000	kHz
Dark signal non-uniformity at 293 K (std. deviation) (see notes 3 and 8)	-	175	375	e^-/pixel/s
Output node capacity	-	600k	-	electrons

Spectral Response (at 253K)

Wavelength (nm)	Minimum Response (QE) (all Basic Process)			Maximum Response Non-uniformity (1σ)	
	Midband Coated	Broadband Coated	Uncoated		
350	15	25	10	5	%
400	40	55	25	3	%
500	85	75	55	3	%
650	85	75	50	3	%
900	25	25	25	5	%

The uncoated process is suitable for soft X-ray and EUV applications

NOTES

1. Signal level at which resolution begins to degrade
2. Measured between 253 and 293K and V_{ss} + 9.5V typically. Dark signal at any temperature T (kelvin) may be estimated from:
$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9060/T}$
Where Q_{d0} is the dark signal at T=293K (20ºC)
3. Test carried out at e2v technologies on all sensors
4. Dynamic range is the ratio of full-well capacity to readout noise measured at 253K and 20kHz readout speed.
5. CCD characterisation measurements made using charge generated by x-ray photons of known energy
6. Measured using a dual-slope integrator technique (i.e. correlated double sample)
7. Readout at speeds in excess of 7MHz can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 253 and 293K, excluding white defects

BLEMISH SPECIFICATION

Traps: Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than $200e^-$ at 253K

Slipped columns: Are counted if they have an amplitude greater than $200e^-$

Black spots: Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots: Are counted when they have a generation rate 50 times the specified maximum dark signal generation rate (measured between 253 and 293K). The typical temperature dependence of white spot defects is different from that of the average dark signal and is given by
$Q_d/Q_{d0} = 122T^3 e^{-6400/T}$

White column: A column which contains at least 9 white spots

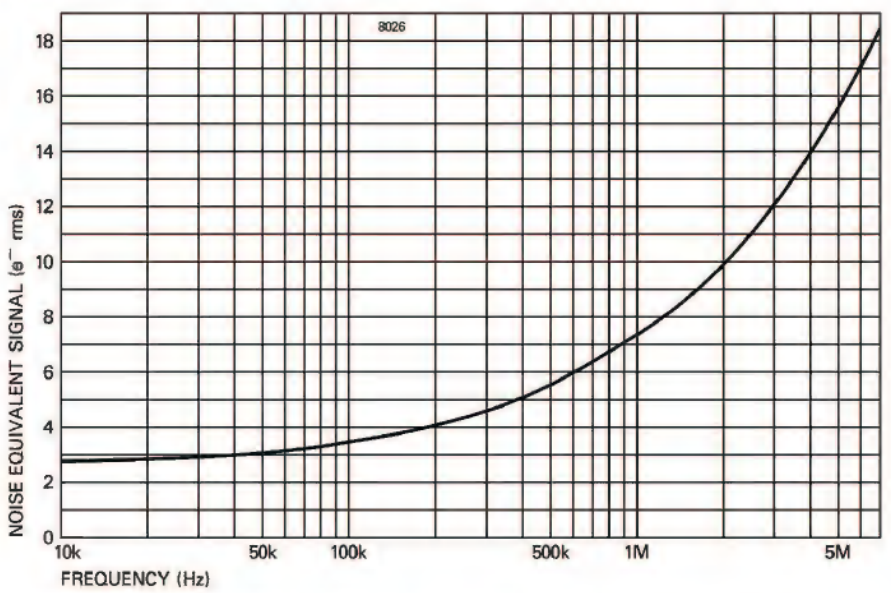
Black column: A column which contains at least 9 black defects

GRADE	0	1	2
Column defects: black or slipped white	0 0	2 0	6 1
Traps > $200e^-$	2	5	10
White spots	20	30	100
Black spots	20	30	60

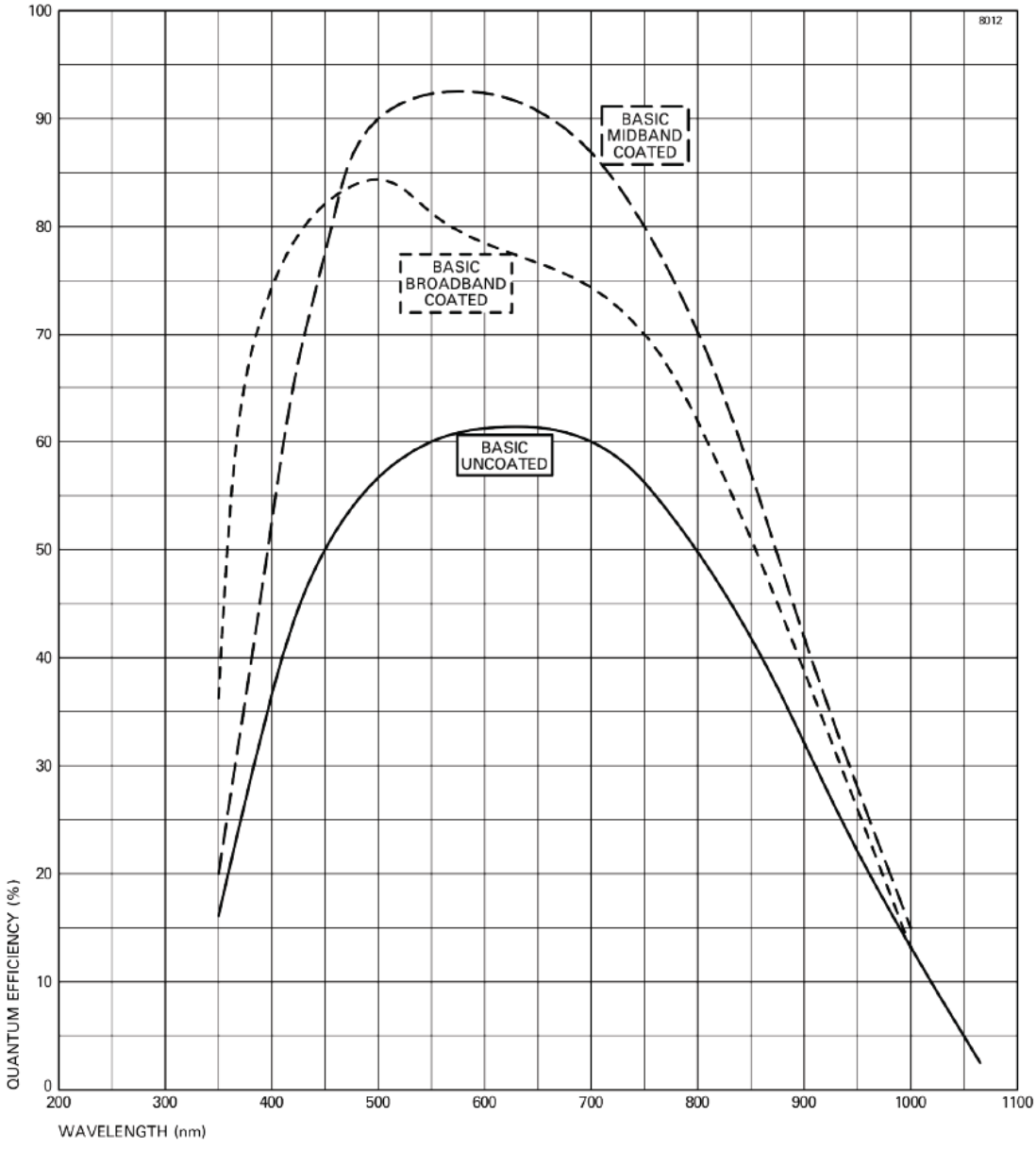
Grade 5: Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters

Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but appear below 253K. The amplitude of white spots and columns will decrease rapidly with temperature.

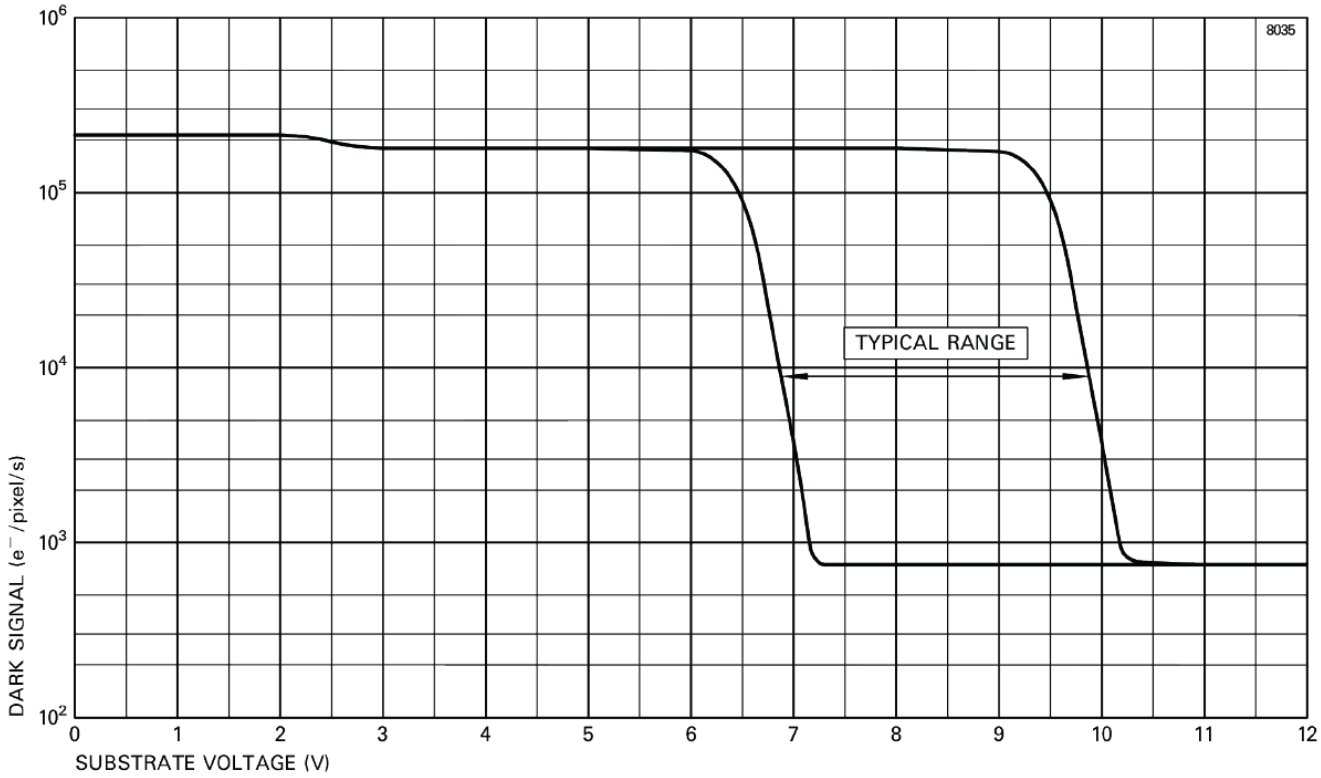
TYPICAL OUTPUT CIRCUIT NOISE



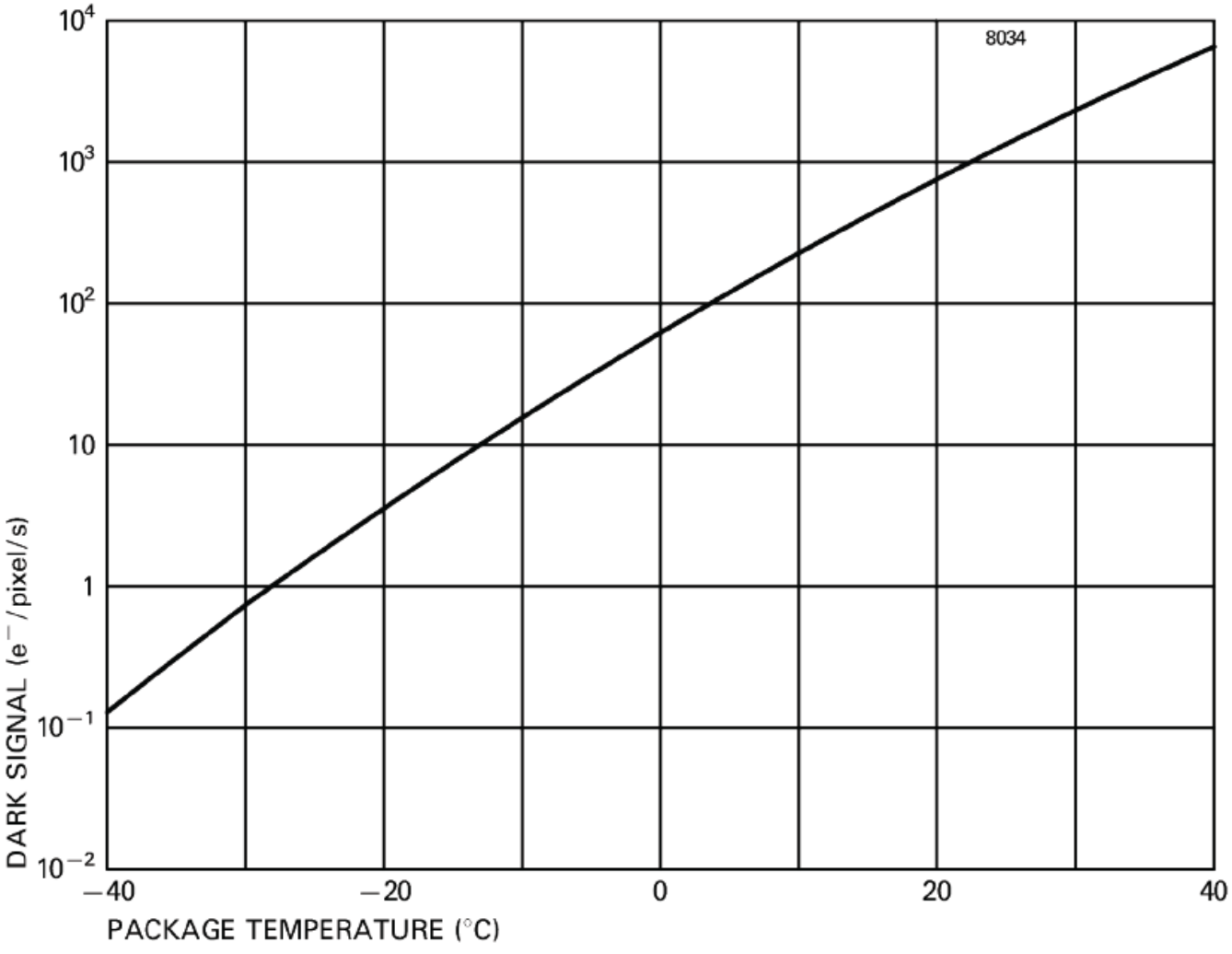
TYPICAL SPECTRAL RESPONSE



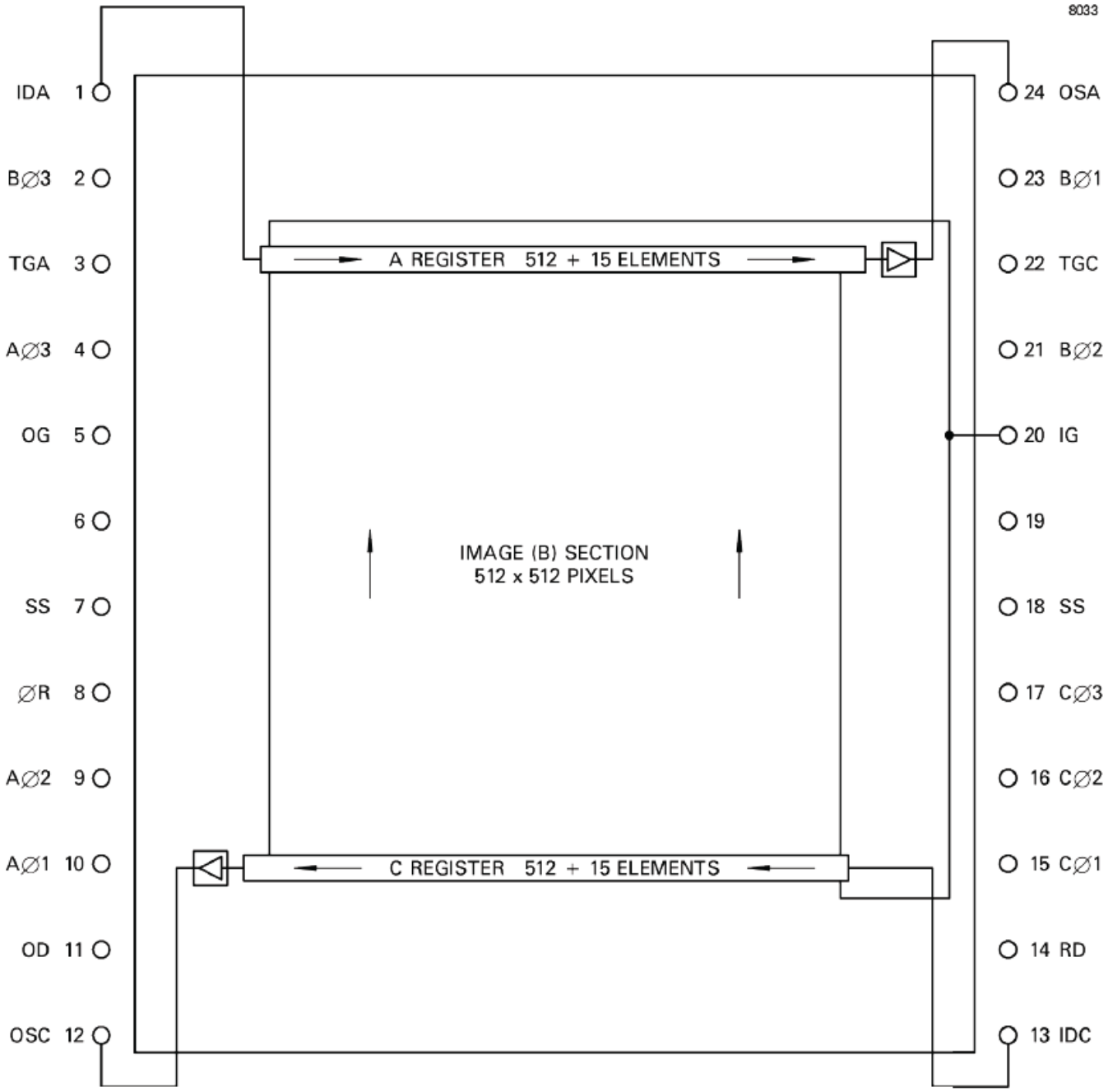
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE AT 20 °C



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE (Vss = +9.5 V)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK LOW TYPICAL	PULSE AMPLITUDE OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
				Min	Typical	Max	
1	IDA	Input diode A	0	see note 9			±20 V
2	BØ3	Image clock	0	10	12	15	±20 V
3	TGA	Transfer gate A	0	10	12	15	±20 V
4	AØ3	Register clock A	1	8	10	15	±20 V
5	OG	Output gate (A and C)	n/a	1	3	5	±20 V
6	-	No connection	0	-			-
7	SS	Substrate	n/a	8	9.5	11	-
8	ØR	Reset (A and C)	0	8	12	15	±20 V
9	AØ2	Register clock A	1	8	10	15	+20 V
10	AØ1	Register clock A	1	8	10	15	±20 V
11	OD	Output drain (A and C)	0	27	29	32	−0.3 to +35 V
12	OSC	Output source C	0	see note 10			−0.3 to +35 V
13	IDC	Input diode C	0	see note 9			−0.3 to +25 V
14	RD	Reset drain (A and C)	0	15	17	19	−0.3 to +25 V
15	CØ1	Register clock C	1	8	10	15	±20 V
16	CØ2	Register clock C	1	8	10	15	±20 V
17	CØ3	Register clock C	1	8	10	15	±20 V
18	SS	Substrate	0	8	9.5	11	-
19	-	No connection	0	-			-
20	IG	Input gate	0	8	10	15	±20 V
21	BØ2	Image clock	0	10	12	15	±20 V
22	TGC	Transfer gate C	0	10	12	15	±20 V
23	BØ1	Image clock	0	10	12	15	±20 V
24	OSA	Output source A	0	see note 10			±20 V

Maximum voltages between pairs of pins:

Pin 11 (OD) to pin 24 (OSA)	±15V
Pin 11 (OD) to pin 12 (OSC)	±15V
Maximum output transistor current	10mA

NOTES

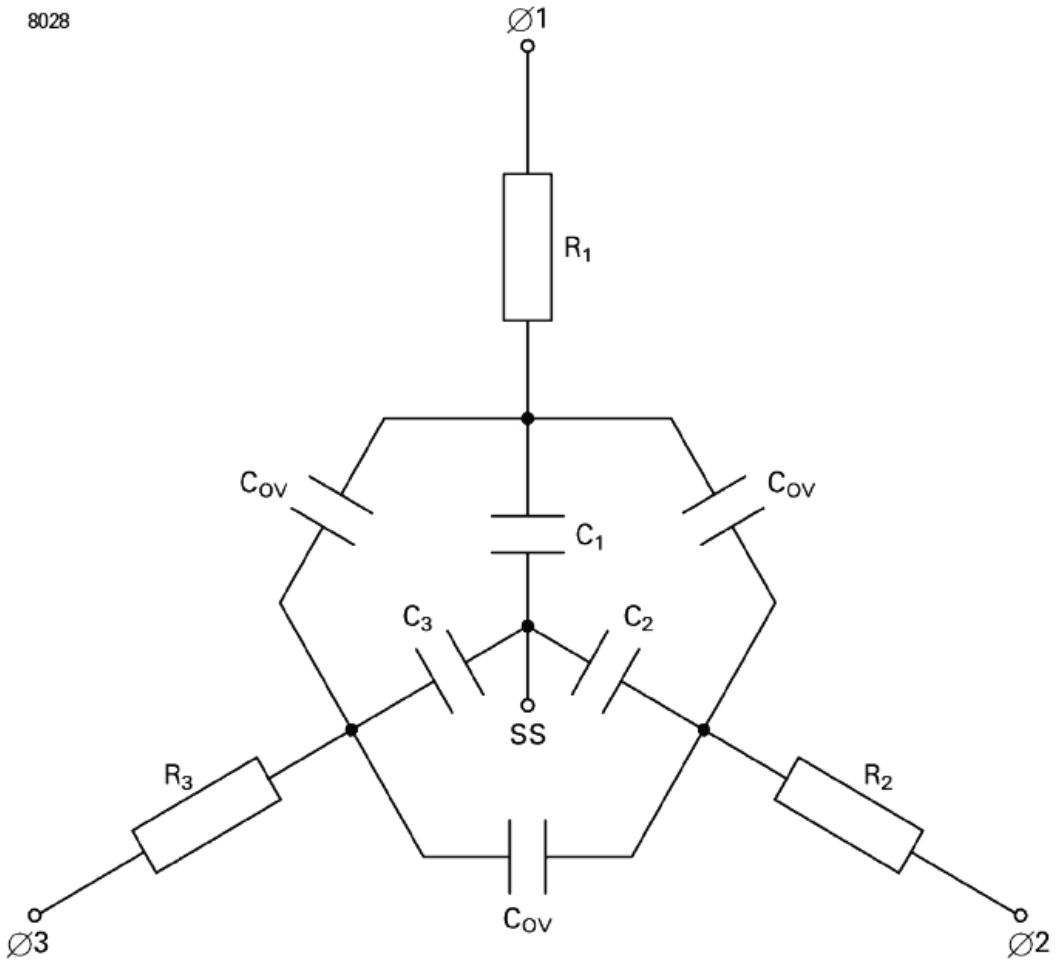
9. For normal operation, the input gate should be set to 0 V and the input diode to approx. 22 V. To inject charge for test purposes, the input gate should be pulsed high during the period when A01 is high and the input diode should be adjusted for the required charge injection. Typical uses for such charge injection include assessing charge transfer efficiency, and the measurement of output responsivity using the reset drain current method.

10. 3 to 5 V below OD. Connect to ground using a 5 mA current source or appropriate load resistor (typically 5 kΩ).

11. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device .

12. With the B0 connections shown, charge is transferred to the top register, A. In order to transfer charge to the bottom register, B0 1 and B02 connections should be reversed. Refer to the waveform diagram.

ELECTRICAL INTERFACE CHARACTERISTICS



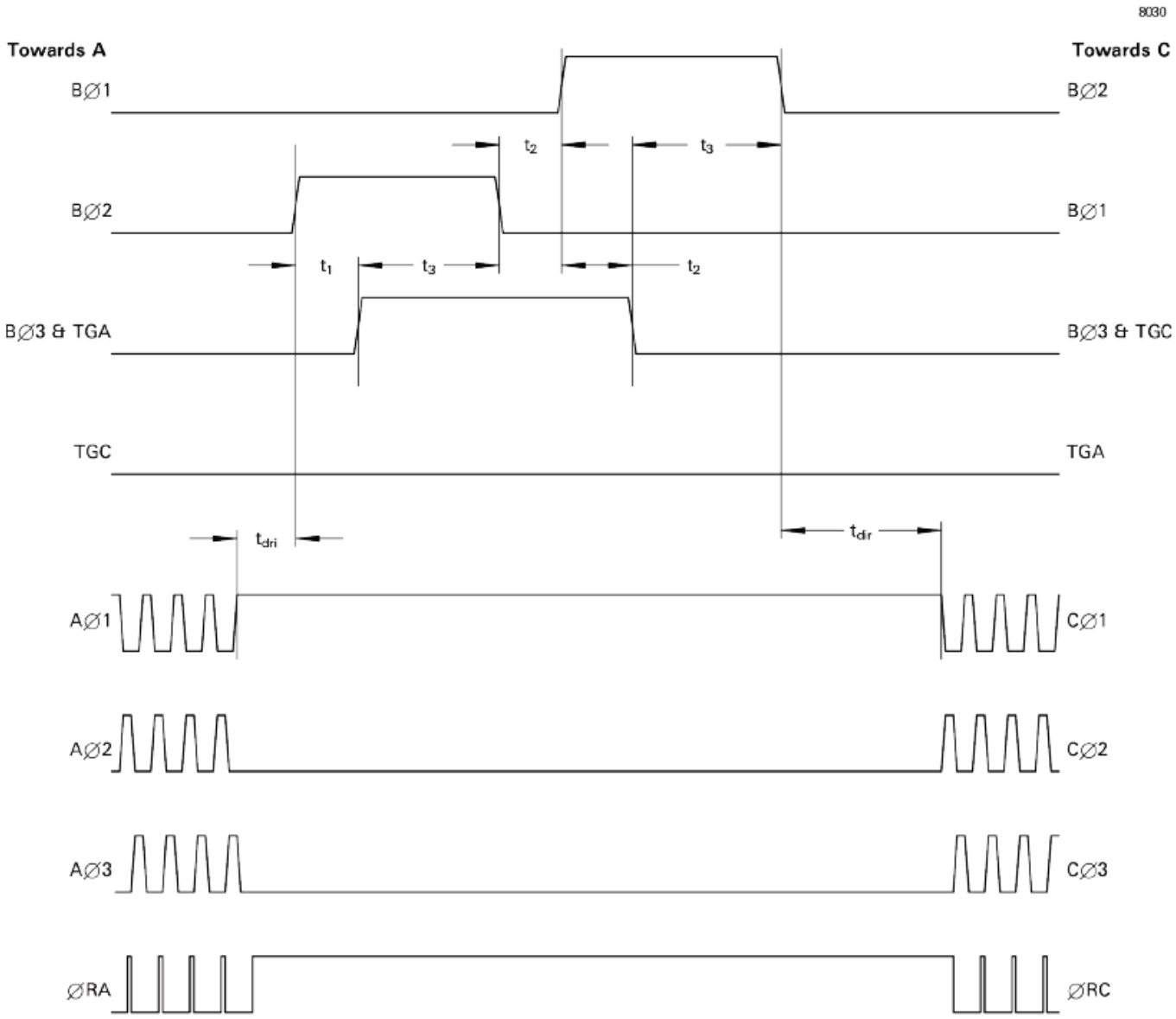
Typical Electrode Capacitances (measured at mid-clock level)

IØ/IØ interphase (C_{0V})	1.6nF
IØ1/SS and IØ2/SS (C_1, C_2)	3.5nF
IØ3/SS (C_3)	12nF
RØ/RØ interphase	30pF
RØ/SS	60pF
ØR/SS	20pF

Typical Electrode Series Resistance

IØ1 and IØ2 (R_1, R_2)	20Ω
IØ3 (R_3)	14Ω
RØ1, 2, 3	20 Ω
Output amplifier impedance at typical operating conditions	400 Ω

DETAIL OF LINE TRANSFER



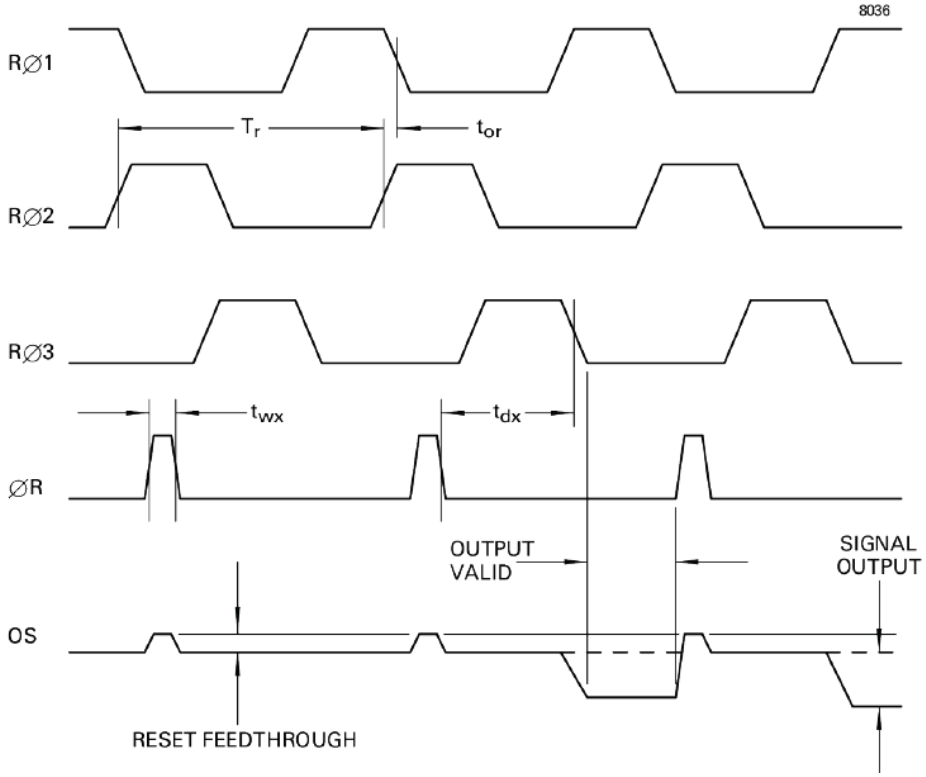
Clocking Sequence

During the integration period, all B0 electrodes should below - the I MO implant takes care of charge gathering. For transfer to the A register, use the labelling of waveforms on the left of the diagram. Charge is transferred to the register when B03 and TGA are taken from high to low.

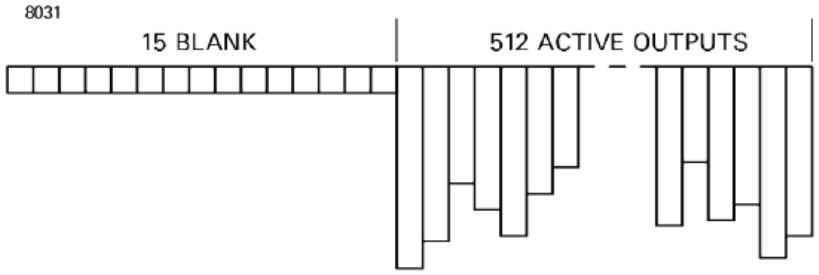
For transfer to the C register, use the labelling of waveforms on the right of the diagram. Charge is transferred to the register when B03 and TGC are taken from high to low.

If only one register is used, the recommended approach for the unused register is to tie its clocks high and its TG low. Any charge collected in the unused register would then spill over OG and drain out through RD, thus keeping unwanted charge out of the image section. Continuous clocking of the unused register can be used but may generate extra heat, potentially causing more dark current in the image area.

DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



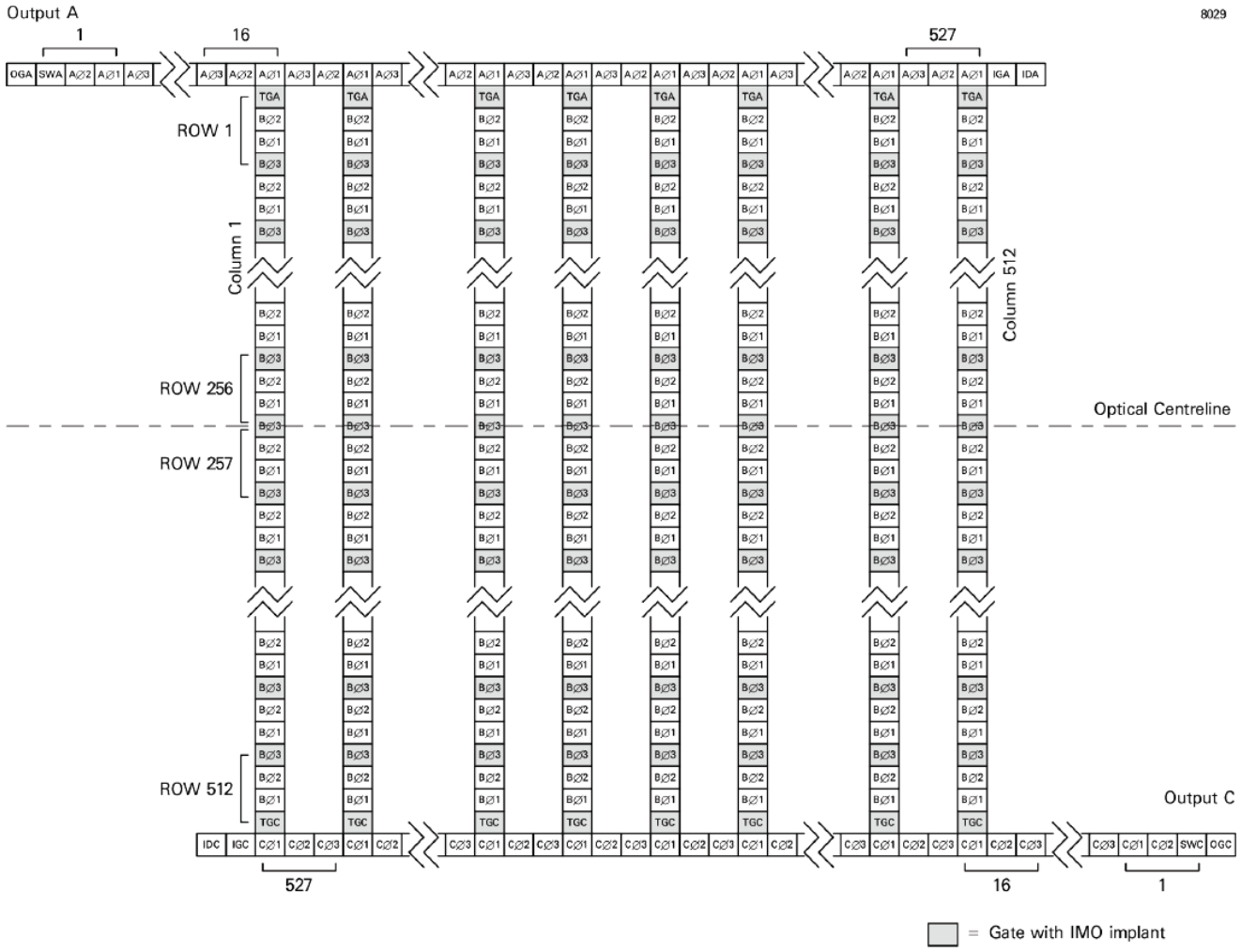
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
t_1	Image clock overlap/delay	10.0	20.0	see note 13	µs
t_2	Image clock overlap/delay	0.65	1.0	see note 13	µs
t_3	Image clock overlap/delay	1.1	2.0	see note 13	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	5	$T_i - 2t_{wi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$T_i - 2t_{wi}$	µs
t_{dri}	Post register clocking delay	1.0	2.0	see note 13	µs
t_{dir}	Pre register clocking delay	1.65	3.0	see note 13	µs
t_{lt}	Line transfer/vertical shift time	16.0	32.0	see note 13	µs
T_r	Output register clock cycle period	140	1000	see note 13	ns
t_{rr}	Clock pulse rise time (10 to 90%)	20	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	10	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	20	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

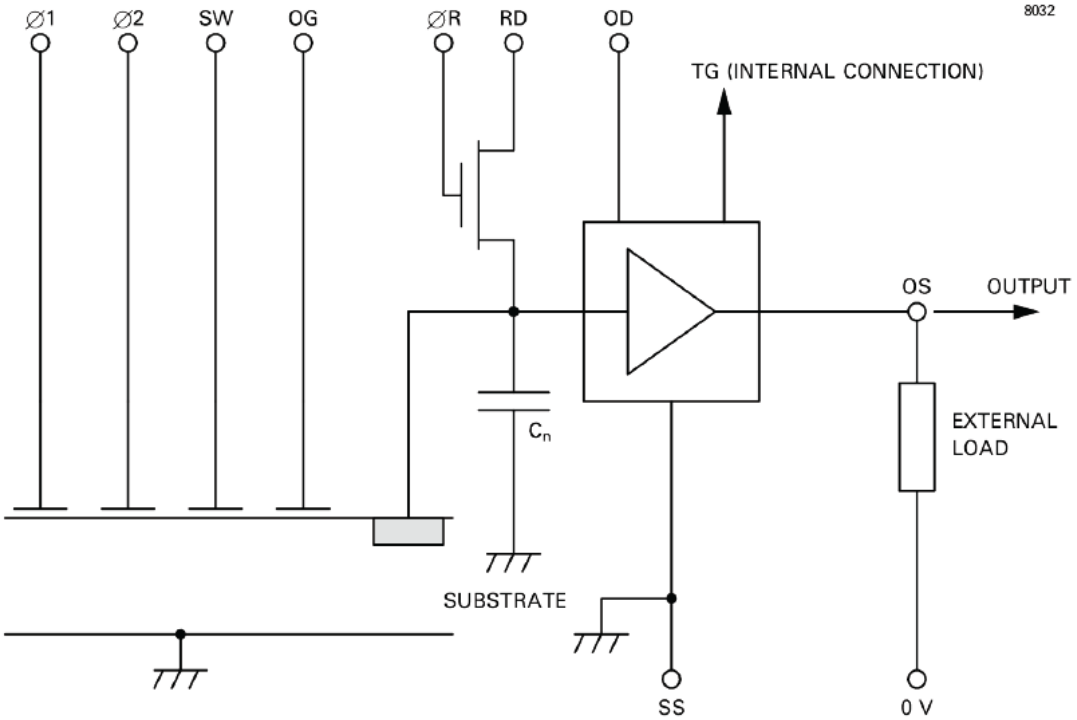
NOTES

13. No maximum other than that set by system constraints on the total readout period.

FUNCTIONAL DIAGRAM



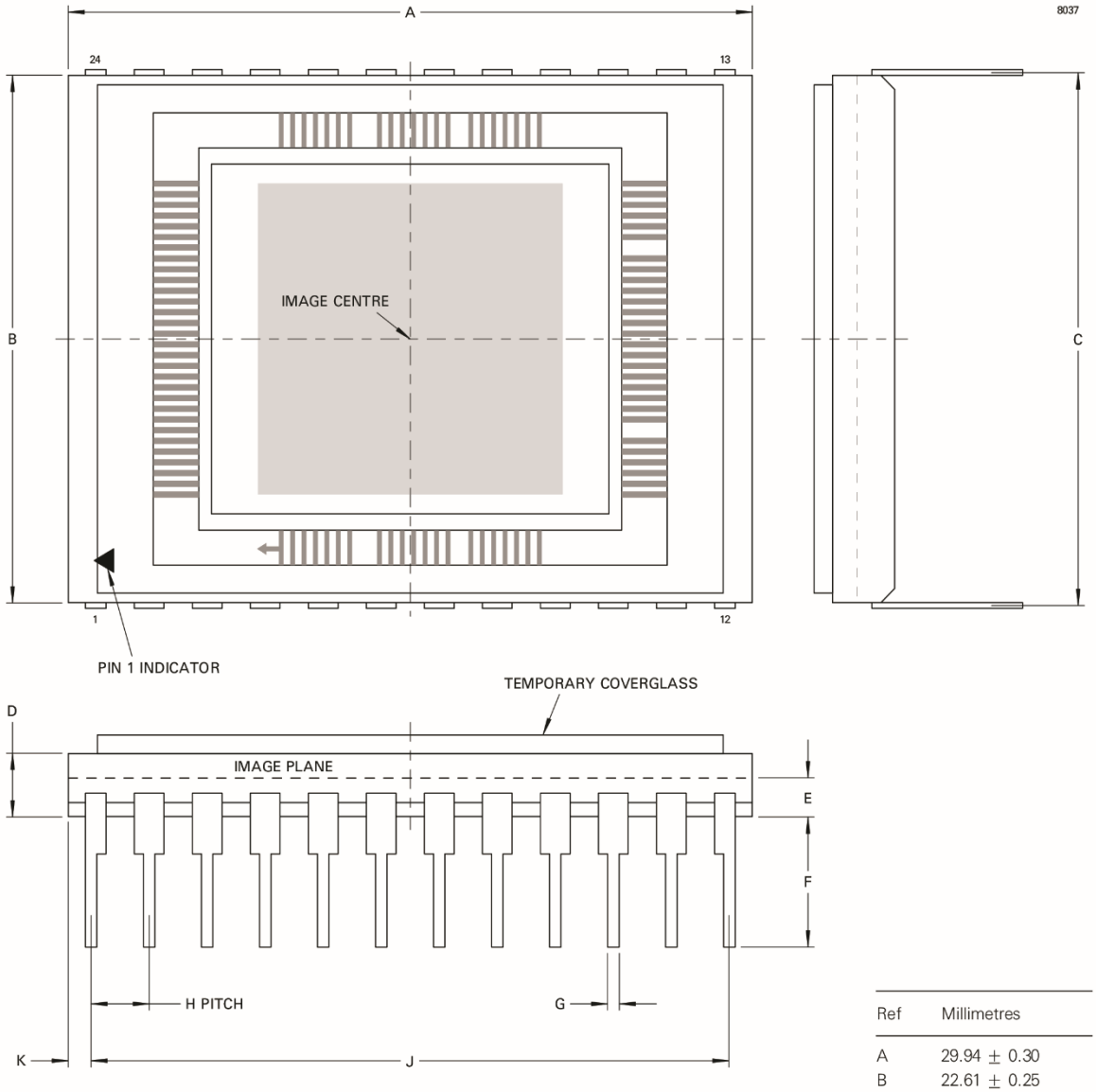
OUTPUT CIRCUIT



NOTE

14. SW is joined to Ø3 in the package

OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3

ORDERING INFORMATION

Options include:

- Temporary Glass Window
- Permanent Window; ask for details
- UV Coating
- X-ray Phosphor Coating

In common with other e2v technologies CCD sensors, a front illuminated CCD77-00 is available with a fibre-optic window or taper.
For further information on the performance of these and other options please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unanttended CCs should not be left out of their conducting foam or socket

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.
Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating	153	273	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.
Maximum device heating/cooling 5K/min