CCD275-42 NIMO Back Illuminated High Performance CCD Sensor

FEATURES

- Large image area
- 26µm square pixels
- Two phase image and store pixels with metallised electrodes
- Three phase bi-directional split register with gated dump drain
- Four output amplifiers
- Back illuminated for high quantum efficiency
- Non-Inverted Mode Operation (NIMO)
- Thin-gate low voltage process.
- Frame transfer operation

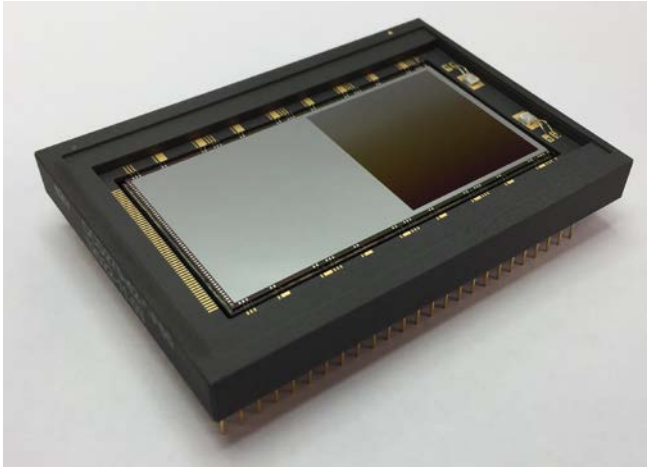
INTRODUCTION

The CCD275-42 is a frame transfer sensor with a large image area and split readout register. Back illumination technology, in combination with low noise output amplifiers, makes the device well suited to the most demanding applications, such as astronomy.

The device design allows operation at high readout rates with pixels optimised for fast line moves with high signal capacity.

The device is supplied in an Aluminium Nitride package with reverse side pins on a 0.1” pitch. The package has two PRT temperature sensors for real time temperature measurement.

Users are advised to consult Teledyne e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging or performance features.



TYPICAL PERFORMANCE

Pixel readout frequency	3 MHz
Output amplifier sensitivity	1.4 µV/e^-
Peak signal	700 ke^-/pixel
Readout noise @ 3 MHz	35 e^- rms

GENERAL DATA

Format

Silicon die size	29.7 x 55.6 mm
Active pixels	1024 (H) x 2050 (V)
Image pixels	1022 (H) x 954 (V)
Image area	26.57 mm (H) x 24.8mm (V)
Pixel size	26µm square
Number of output amplifiers	4 (+ 4 dummy)

Package

Package footprint	50 x 70 mm
Focal plane height	6 mm
Package type	Aluminium nitride ceramic with pins on a 0.1” (2.54mm) grid pitch.

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ELECTRO-OPTICAL PERFORMANCE (At 233K unless stated)

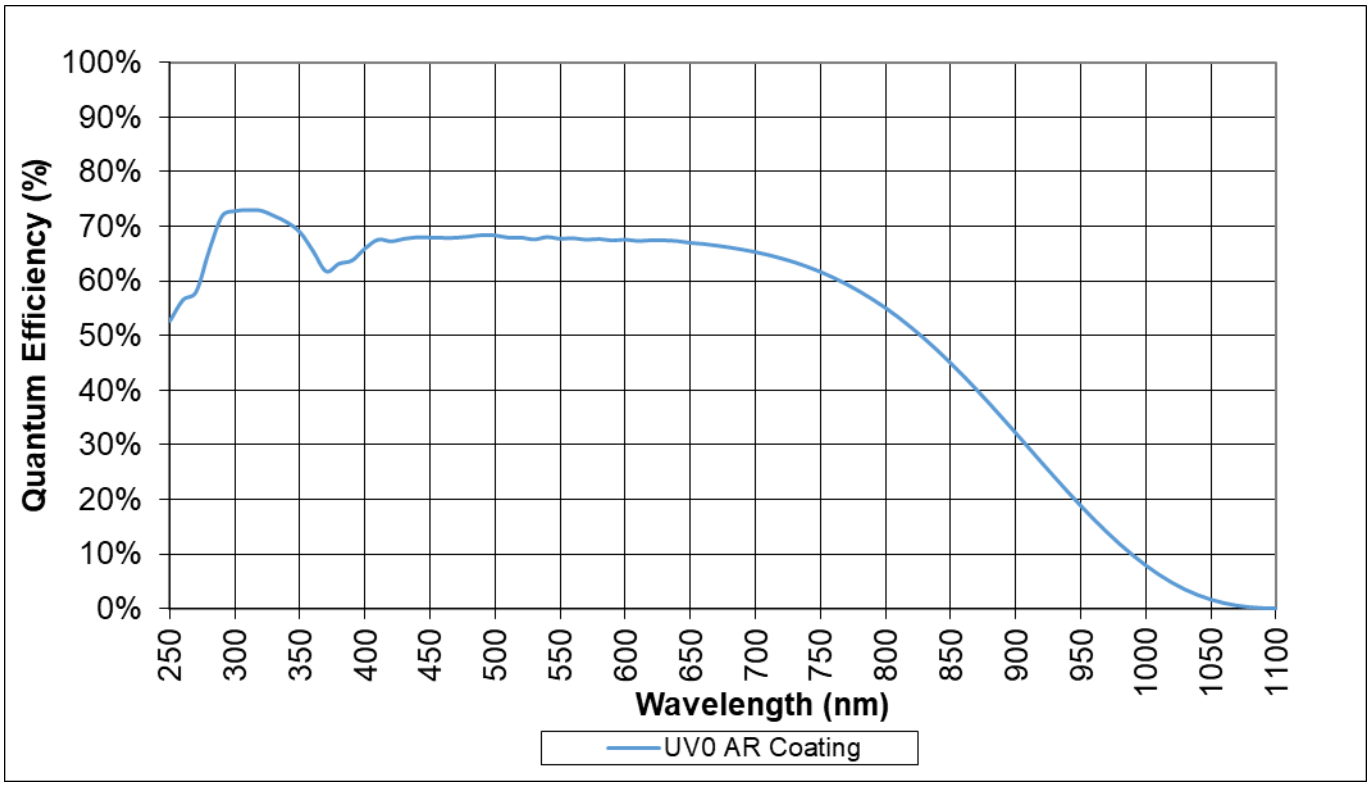
		Min	Typical	Max	Units	Note
Image peak charge storage		500,000	700,000	-	e^-/pixel	
Register peak charge storage		-	3,000,000	-	e^-/pixel	1
Output node capacity (Gain 1)			1,400,000		e-	1,2
Output amplifier responsivity (Gain 1)		-	1.4	-	µV/e^-	2
Readout noise (Gain 1)		-	35	45	rms e^-	2,3
Dark signal		-	160	220	e^-/pixel/s	4
Charge transfer efficiency	Parallel	99.999	99.9995	-	%	5
	Serial	99.998	99.9985	-	%	
Pixel readout frequency		-	3	5	MHz	1,6
Frame transfer period		0.8	1	-	ms	1,7

NOTES

1) Predicted values from design; not measured.
2) Typical values are for default Gain 1 high responsivity mode of operation. A switchable gain capability is provided, with Gain 2 mode providing typical values of 0.6 µV/e^- responsivity, 2 Me- node capacity and 70 e- noise. Only Gain 1 mode is factory tested.
3) Measured with digital correlated double sampling at 3MHz pixel rate, in darkness and reverse clocking the register clocks to exclude dark signal shot noise.
4) Dark signal at 233K. It is a strong function of temperature and the typical average (background) dark signal is taken as:
$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
where Q_{d0} is the dark current at 293 K. In some circumstances strong illumination may leave a low level of residual charge in the following image.
5) The CTE value is quoted for the complete clock cycle (i.e. not per phase).
6) All factory testing is performed at the typical 3MHz readout frequency. The maximum frequency of the output depends on the external load capacitance to be driven but is expected to be up to 5MHz, though this is not verified by test and performance cannot be guaranteed.
7) The maximum line move rate has a dependancy on the series resistance, comprising the on-chip, external and buffer components with < 15 Ohms assmued the fastest frame transfer. Minimum period is not verified by test .

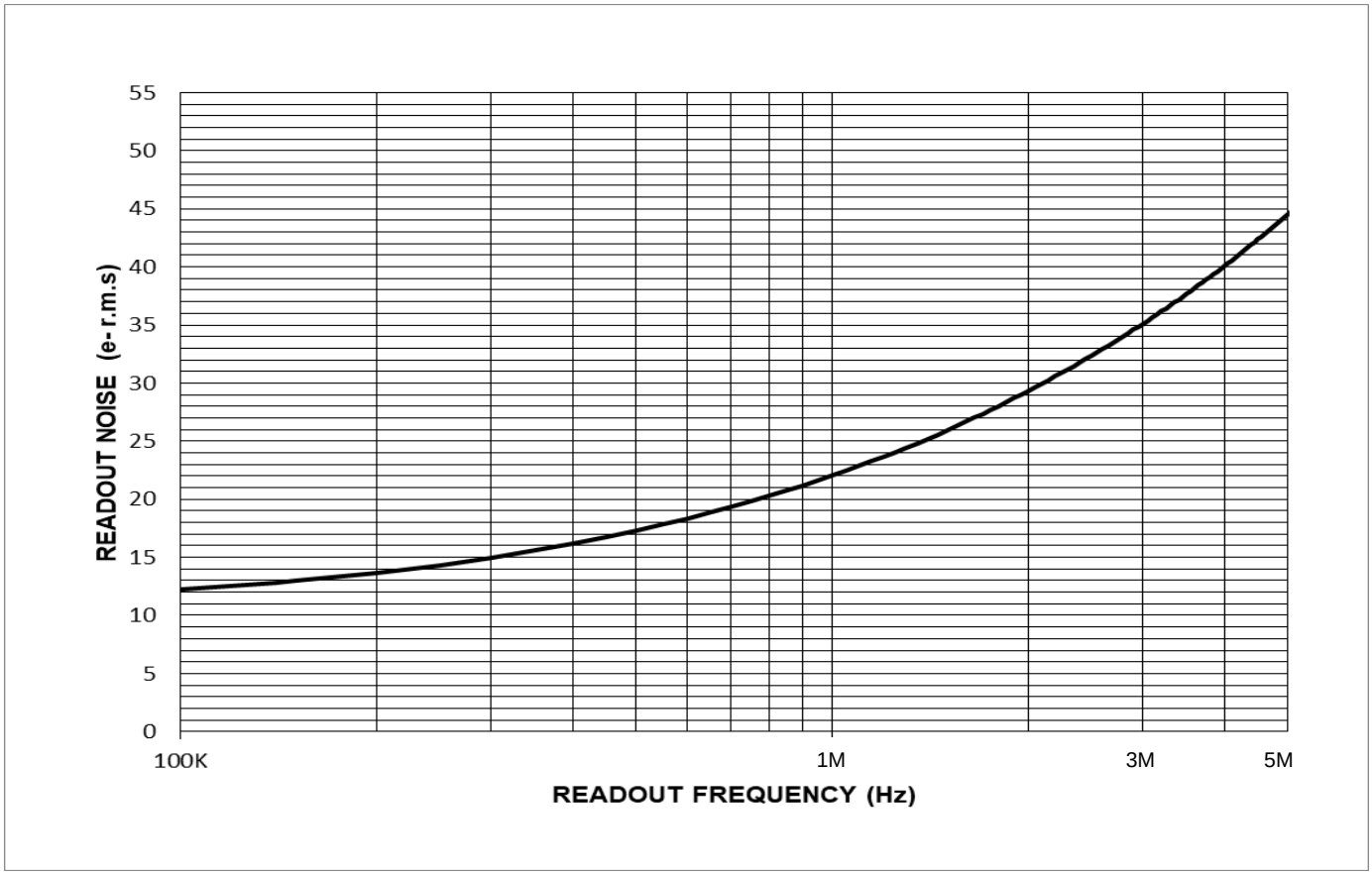
TYPICAL SPECTRAL RESPONSE CURVE AT 233K

For default UV0 coating



TYPICAL OUTPUT CIRCUIT NOISE

With correlated double sampling at a bandwidth of 2x readout frequency without dummy output operation.



COSMETIC SPECIFICATION

Maximum allowed defect levels are indicated below.

GRADE	1	2
Black Column defects	2	6
White Column defects	1	2
White spots	100	150
Black spots	200	550
Traps >200 e^-	5	12

Grade 5 devices are also available as electrical samples. These are confirmed to have working outputs and will nominally provide an image. Not all parameters are guaranteed to be tested or provided and the image quality may be worse than that of a grade 2.

Grade 6 devices are also available as mechanical samples. No electrical performance is provided and these should not be connected to electronics. The mechanical performance parameters will be measured but not guaranteed to be compliant to the maximum values above.

DEFINITIONS

White Column defects	A column is counted as a defect if it contains at least 15 white or dark single pixel defects.
Black Column defects	A column is counted as a defect if it contains at least 15 white or dark single pixel defects.
White spots	A defect is counted as a white spot if the dark generation rate is 10 times the specified maximum dark signal generation rate at 233K.
Black spots	A black spot defect is a pixel with less than 80% of the local mean at a signal level of approximately half full well.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e- at 233 K.

DEFINITIONS

Back-Thinning
A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal. The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required the dummy outputs may be powered down by not fitting the external load resistor, biases must remain connected.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration.
Dark signal is a strong function of temperature as described in note 4.

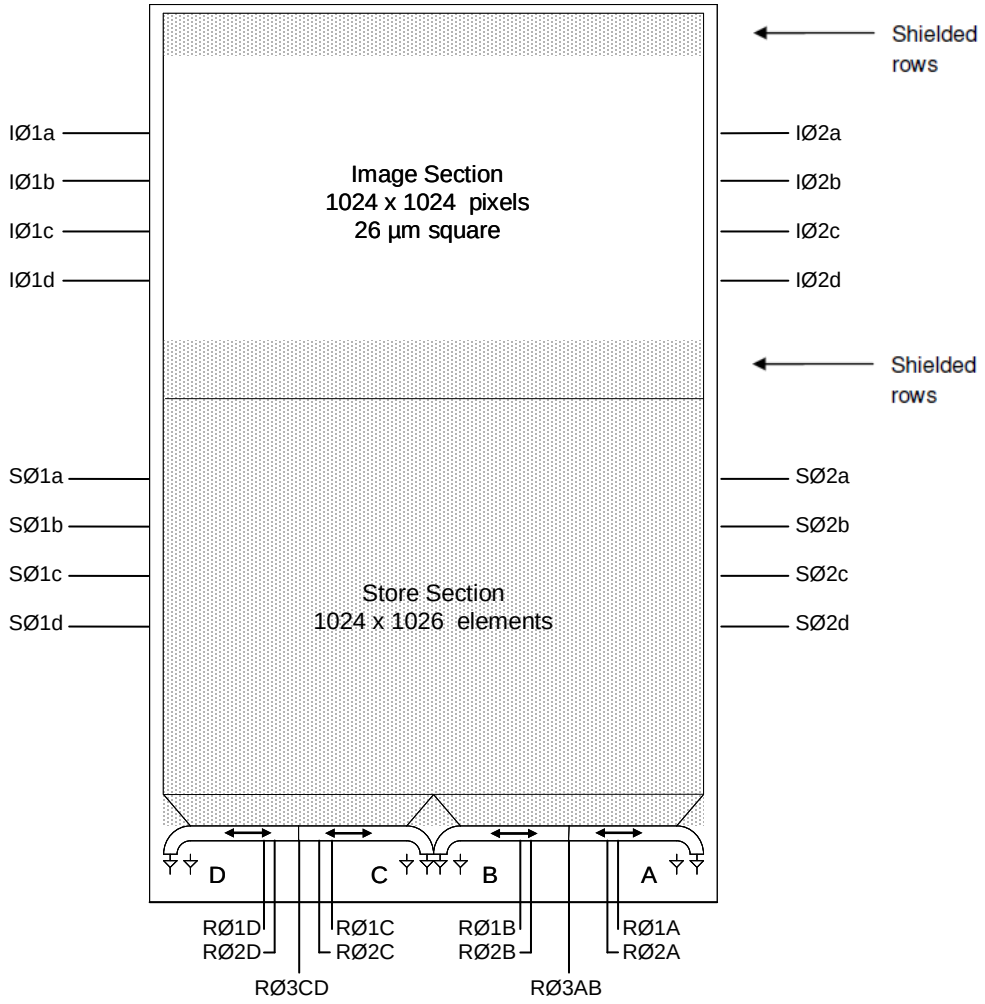
Correlated Double Sampling

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency

DEVICE SCHEMATIC



FRAME READOUT

To readout in the default mode of operation to through outputs A and D only, the following clocking needs to be applied to the register connections.

Clock Phase	RØ1	RØ2	RØ3
Register A charge towards OSA	RØ1A	RØ2A	RØ3AB
Register B charge towards OSA	RØ2B	RØ1B	RØ3AB
Register C charge towards OSD	RØ2C	RØ1C	RØ3CD
Register D charge towards OSD	RØ1D	RØ2D	RØ3AB

ELECTRICAL INTERFACE

PIN	REF	DESCRIPTION	Typical Bias (V)	Typical Clock Low (V)	Typical Clock High (V)	Max Rating With respect to Vss (V)
1	TS1A	Temperature sensor 1 +Ve	-	-	-	N/A
2	TS1B	Temperature sensor 1 -Ve	-	-	-	N/A
3	TD	Top Drain	24	-	-	-0.3 to 30
4	SS	Substrate	0	-	-	N/A
5	IØ1A	Image clock 1 A	-	0	7	±15
6	SS	Substrate	0	-	-	N/A
7	IØ1B	Image clock 1 B	-	0	7	±15
8	SS	Substrate	0	-	-	N/A
9	IØ1C	Image clock 1 C	-	0	7	±15
10	SS	Substrate	0	-	-	N/A
11	IØ1C	Image clock 1 D	-	0	7	±15
12	SS	Substrate	0	-	-	N/A
13	SØ1A	Store clock 1 A	-	0	7	±15
14	SS	Substrate	0	-	-	N/A
15	SØ1B	Store clock 1 B	-	0	7	±15
16	SS	Substrate	0	-	-	N/A
17	SØ1C	Store clock 1 C	-	0	7	±15
18	RESPD	Responsivity/Gain selection D (note 10)	0	-	-	±15
19	SØ1D	Store clock 1 D	-	0	7	±15
20	RESPC	Responsivity/Gain selection C (note 10)	0	-	-	±15
21	OSD	Output Source D	-	-	-	N/A
22	DOSD	Dummy Output Source D	-	-	-	N/A
23	OGD	Output Gate D	2	-	-	±15
24	DGCD	Dump Gate C/D	-	0	7	±15
25	SS	Substrate	0	-	-	N/A
26	ODD	Output Drain D	24	-	-	-0.3 to 30
27	DODD	Dummy Output Drain D	24	-	-	-0.3 to 30
28	RDD	Reset Drain D	15	-	-	-0.3 to 20
29	DCØC/D	DC Restore Output C/D	-	0	10	±15
30	SS	Substrate	0	-	-	N/A
31	RØ2D	Register D clock 2	-	1	7	±15
32	RØ3CD	Register C/D clock 3	-	1	7	±15
33	SS	Substrate	0	-	-	N/A
34	RØ2C	Register C clock 2	-	1	7	±15
35	RØ1D	Register D clock 1	-	1	7	±15
36	RØ1C	Register C clock 1	-	1	7	±15
37	ØRD	Reset Output D	-	0	10	±15
38	ØRC	Reset Output C	-	0	10	±15
39	OGC	Output Gate C	2	-	-	±15
40	RDC	Reset Drain C	15	-	-	-0.3 to 20
41	DODC	Dummy Output Drain C	24	-	-	-0.3 to 30
42	DOSC	Dummy Output Source C	-	-	-	N/A
43	ODC	Output Drain C	24	-	-	-0.3 to 30
44	OSC	Output Source C	-	-	-	N/A
45	DD	Dump Drain	24	-	-	-0.3 to 30

PIN	REF	DESCRIPTION	Typical Bias (V)	Typical Clock Low (V)	Typical Clock High (V)	Max Rating With respect to Vss (V)
46	SS	Substrate	0	-	-	N/A
47	ODB	Output Drain B	24	-	-	-0.3 to 30
48	OSB	Output Source B	-	-	-	N/A
49	DODB	Dummy Output Drain B	24	-	-	-0.3 to 30
50	DOSB	Dummy Output Source B	-	-	-	N/A
51	OGB	Output Gate B	2	-	-	±15
52	RDB	Reset Drain B	15	-	-	-0.3 to 20
53	ØRA	Reset Output A	-	0	10	±15
54	ØRB	Reset Output B	-	0	10	±15
55	RØ1A	Register A clock 1	-	1	7	±15
56	RØ1B	Register B clock 1	-	1	7	±15
57	SS	Substrate	0	-	-	N/A
58	RØ2B	Register B clock 2	-	1	7	±15
59	RØ2A	Register B clock 2	-	1	7	±15
60	RØ3AB	Register A/B clock 3	-	1	7	±15
61	ODA	Output Drain A	24	-	-	-0.3 to 30
62	DODA	Dummy Output Drain A	24	-	-	-0.3 to 30
63	RDA	Reset Drain A	15	-	-	-0.3 to 20
64	DCØA/B	DC Restore Output A/B	-	0	10	±15
65	SS	Substrate	0	-	-	N/A
66	TS2B	Temperature sensor 2 -Ve	-	-	-	N/A
67	TS2A	Temperature sensor 2 +Ve	-	-	-	N/A
68	TG	Top Gate	0	-	-	±15
69	SS	Substrate	0	-	-	N/A
70	IØ2A	Image clock 2 A	-	0	7	±15
71	SS	Substrate	0	-	-	N/A
72	IØ2B	Image clock 2 B	-	0	7	±15
73	SS	Substrate	0	-	-	N/A
74	IØ2C	Image clock 2 C	-	0	7	±15
75	SS	Substrate	0	-	-	N/A
76	IØ2D	Image clock 2 D	-	0	7	±15
77	SS	Substrate	0	-	-	N/A
78	SØ2A	Store clock 2 A	-	0	7	±15
79	SS	Substrate	0	-	-	N/A
80	SØ2B	Store clock 2 B	-	0	7	±15
81	SS	Substrate	0	-	-	N/A
82	SØ2C	Store clock 2 C	-	0	7	±15
83	RESPA	Responsivity/Gain selection A (note 10)	0	-	-	±15
84	SØ2D	Store clock 2 D	-	0	7	±15
85	RESPB	Responsivity/Gain selection B (note 10)	0	-	-	±15
86	OSA	Output Source A	-	-	-	N/A
87	DOSA	Dummy Output Source A	-	-	-	N/A
88	OGA	Output Gate A	2	-	-	±15
89	DGAB	Dump Gate A/B	-	0	7	±15
90	SS	Substrate	0	-	-	N/A

NOTES

8) If all voltages are set to the 'typical' values, operation at or close to typical performance should be obtained.

9) Maximum voltage between pairs of pins: OS to OD + 15 V. Maximum current through any source or drain pin: 10 mA.

10) Default high responsivity gain 1 mode is with RESP bias at 0 V. For Gain 2 mode RESP should be set to +10 V.

PIN CONNECTIONS (View facing pins of connector)

See package dimension drawings below for pin numbering.

TEMPERATURE SENSOR OPERATION

Two, 2 wire PT1000 PRT's are fitted to the device. These can be used during operation to monitor the device temperature. If they are not used it is recommended that they are grounded to minimise noise pickup.

POWER UP AND DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. This includes ensuring that reverse bias voltages cannot be momentarily applied.

It crucial that the power on order is followed; failure to observe this may result in irreparable damage to the device.

Power On: -

1) Drain biases e.g. OD, RD

2) Substrate

3) Gate biases eg. OG and clocks can be enabled

All biases must be settled at their operating level before commencing the power on sequence.

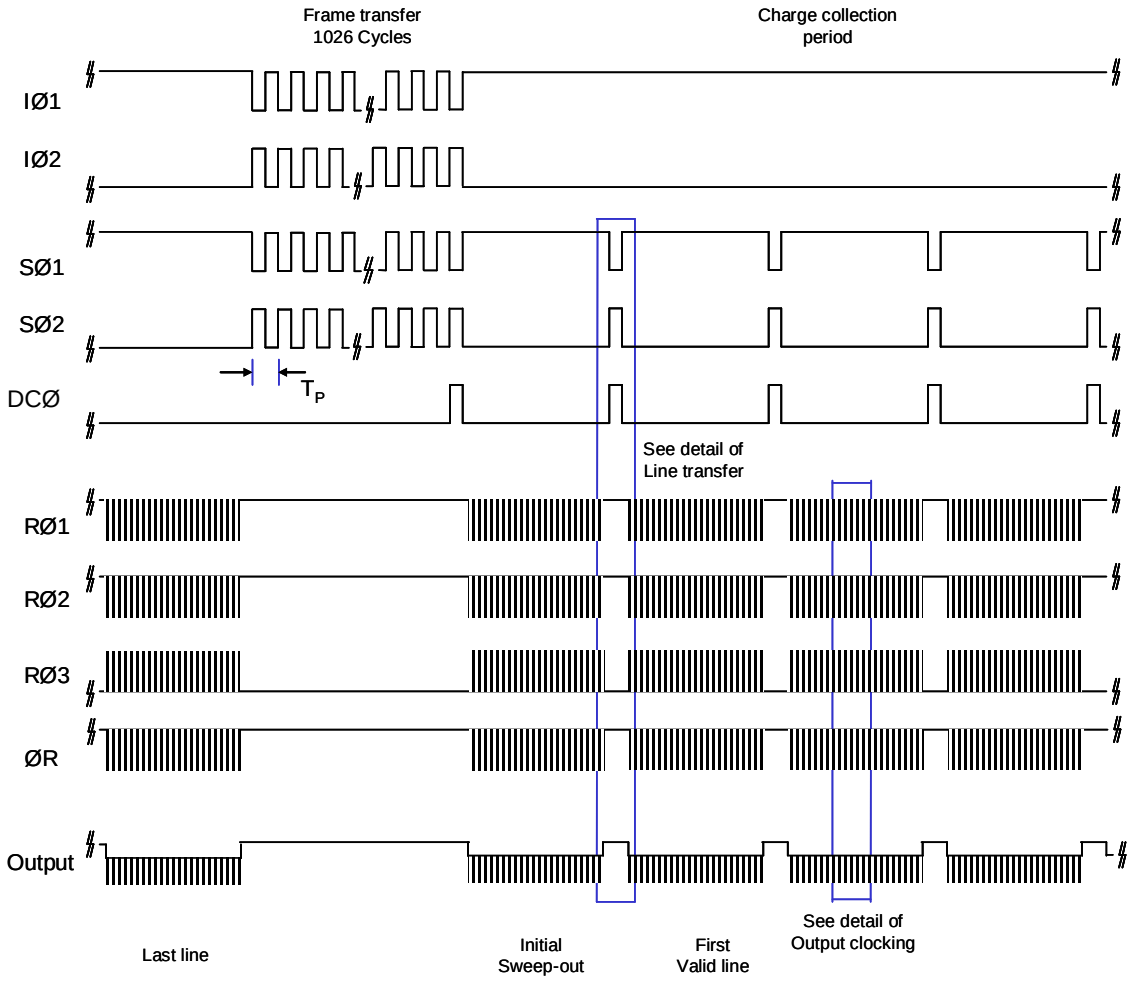
Power off: -

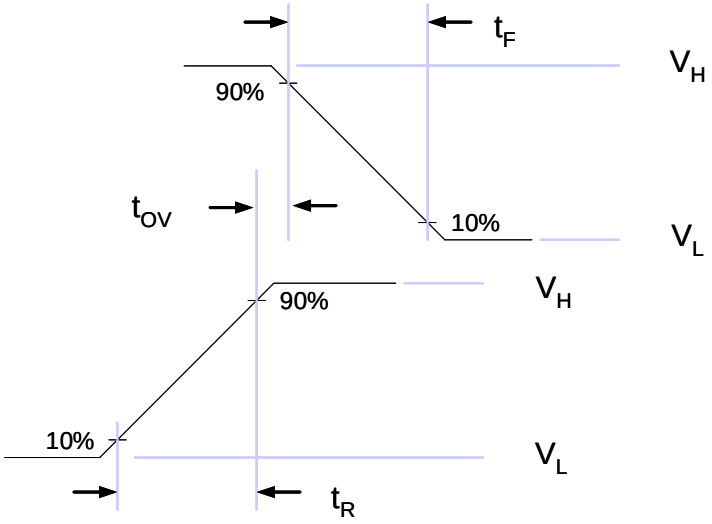
The reverse of the above.

It is also important to ensure that excess currents do not flow in the OS pins. Such currents could arise from rapid charging/discharging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier

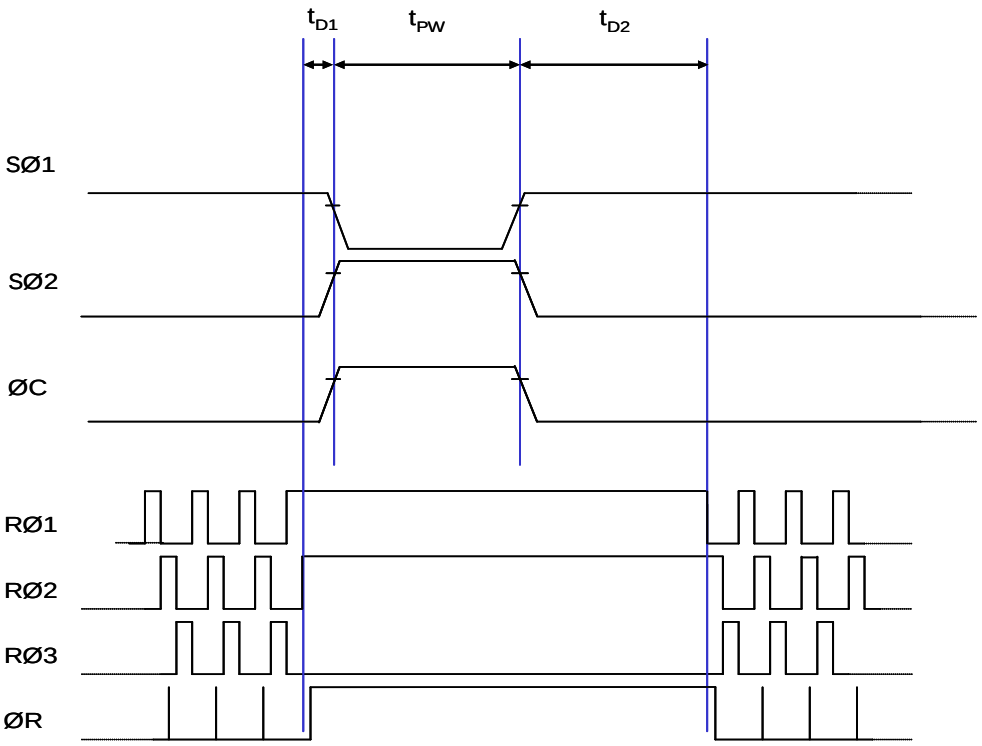
FRAME READOUT TIMING DIAGRAM

Detail of Frame Transfer

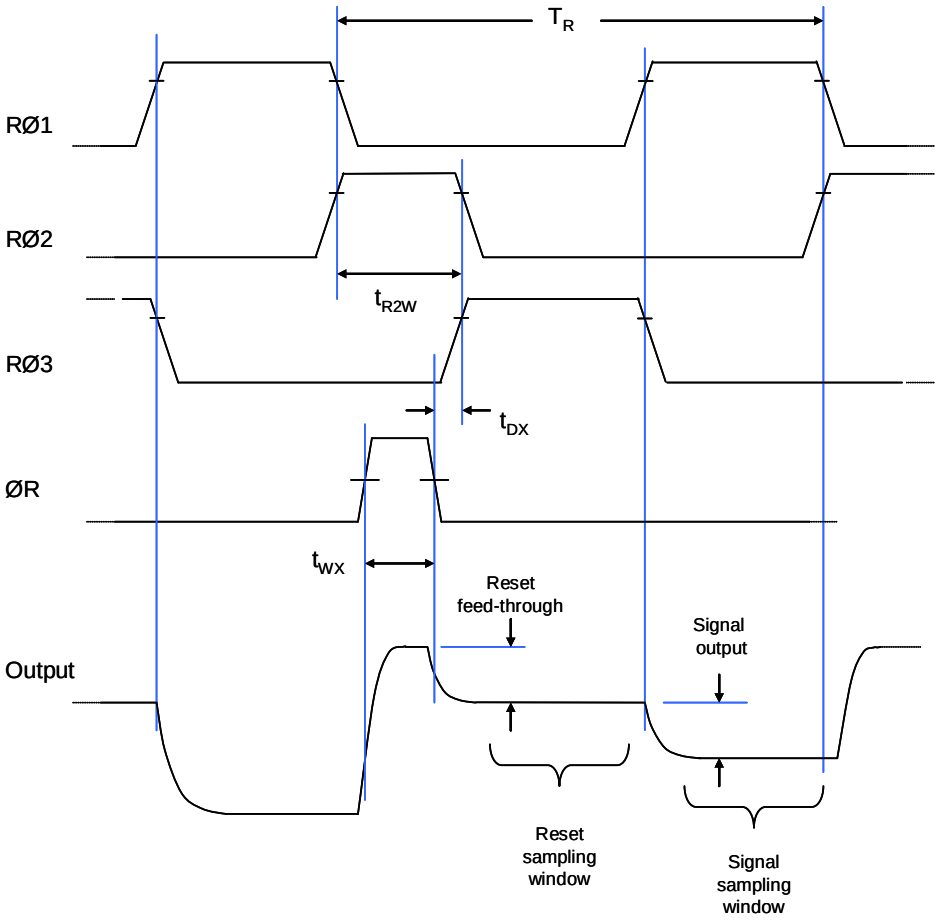




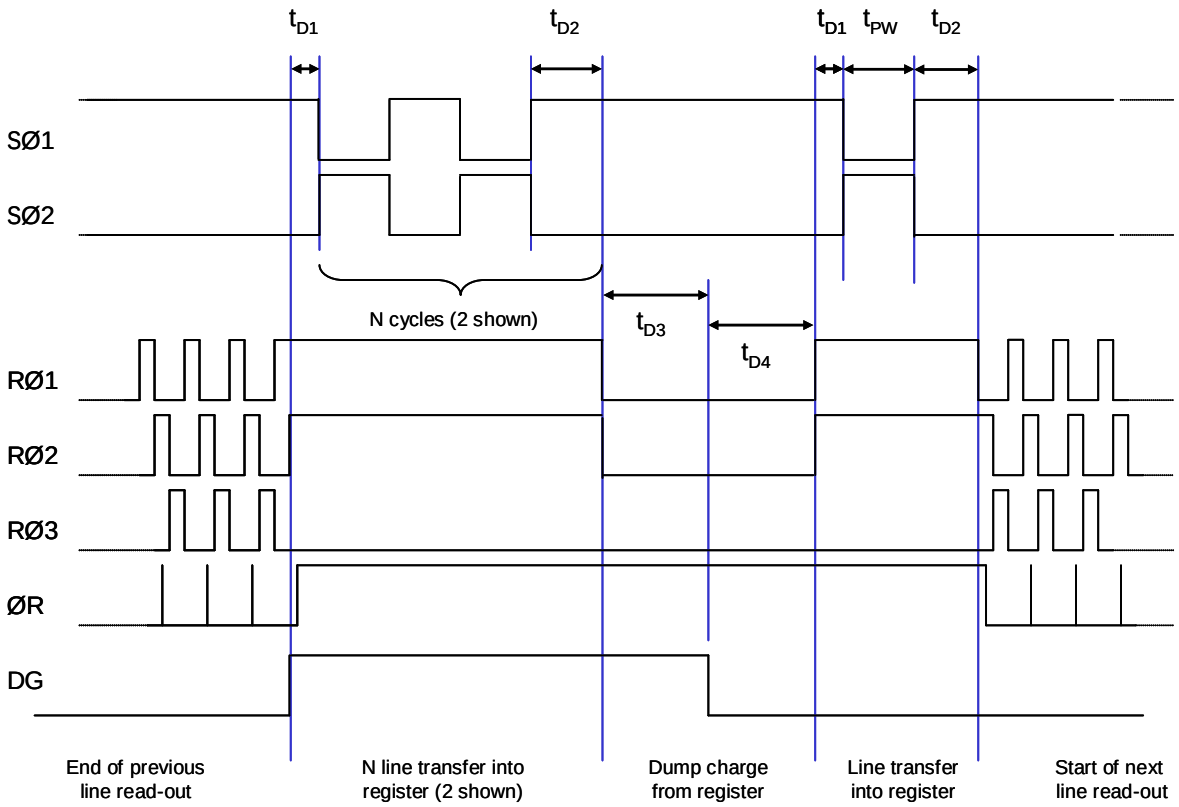
Detail of Line Transfer



Detail of Output clocking



Charge Dumping Sequence



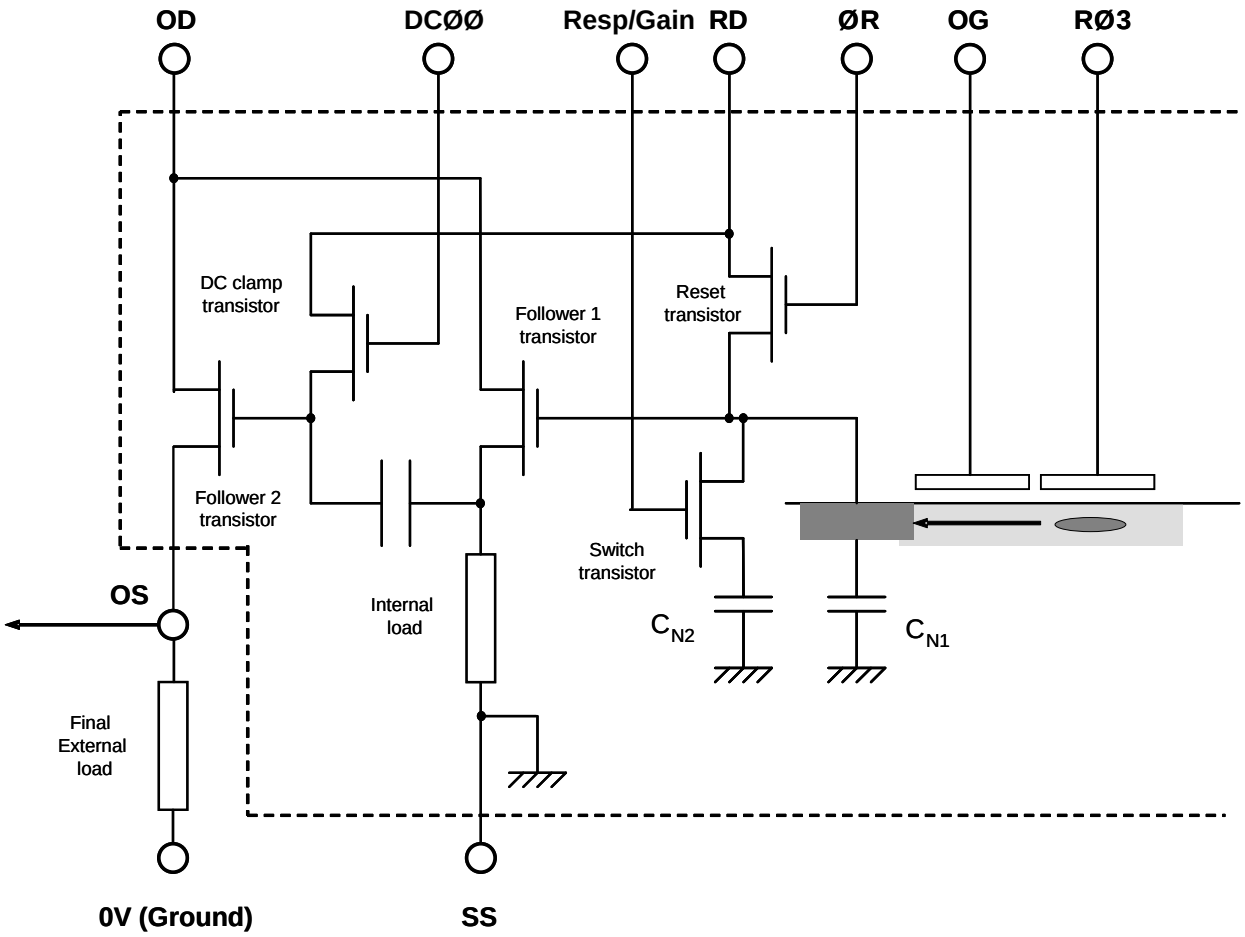
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typ	Max	Unit
	Line Move Period	800	1000	-	ns
t_{PR}	Image/Store section pulse ries time (10-90%)	45	50	-	ns
t_{PF}	Image/Store section pulse fall time (10-90%)	45	50	-	ns
t_R	Register clock period	-	334	-	ns
t_{RR}/t_{XR}	Register/Reset pulse rise time (10-90%)	5	10	15	ns
t_{RF}/t_{XF}	Register/Reset pulse fall time (10-90%)	5	10	15	ns
t_{WX}	Reset pulse width (at 50% levels)	20	25	-	ns

NOTES

11) Where no minimum or maximum is stated, the value is either not critical or is determined only by the readout timing necessary for the required chip operation in the specific application of the user.

OUTPUT CIRCUIT

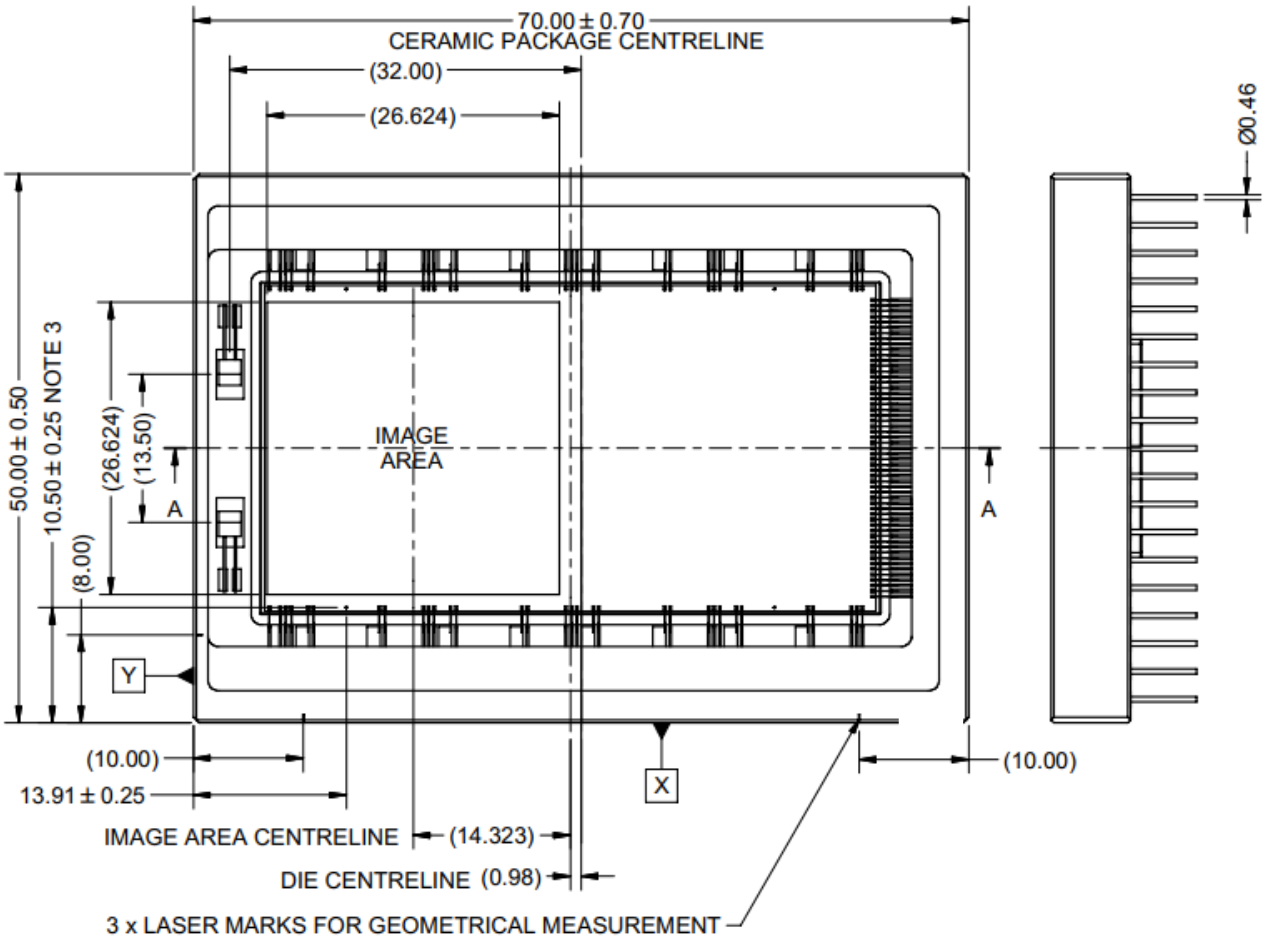


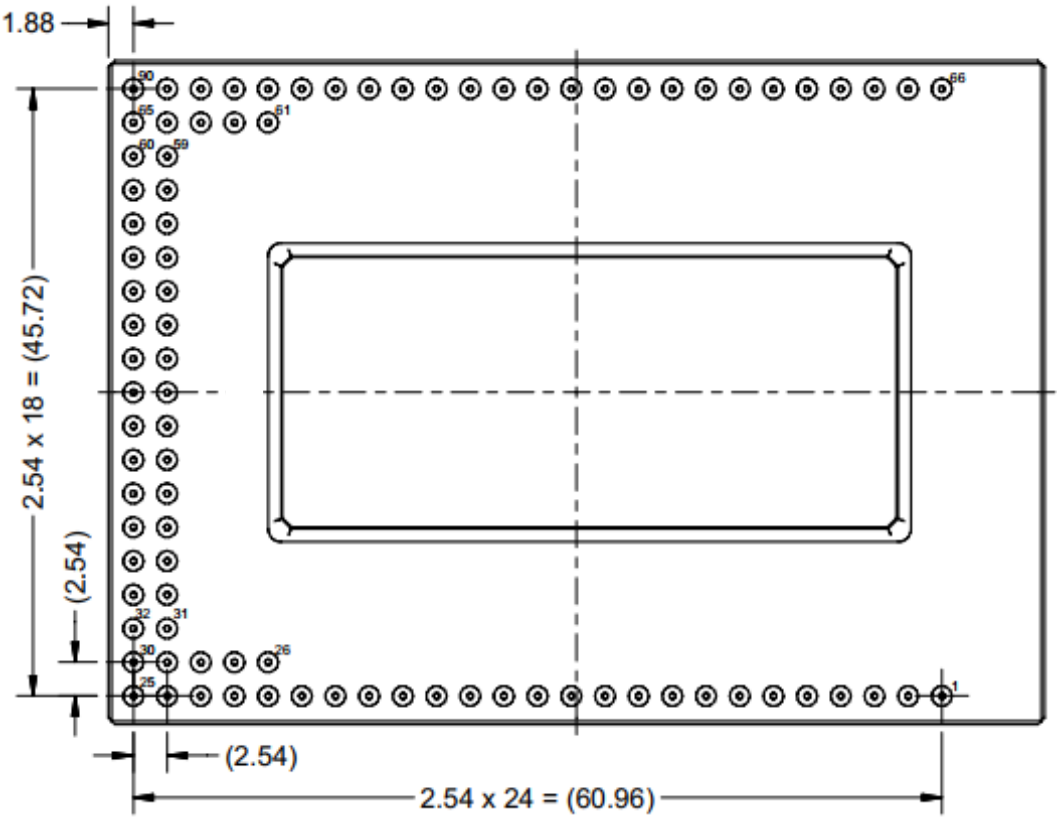
NOTES

12) The amplifier has a DC restoration circuit, which is activated internally whenever DCØ is pulsed high. This should be pulsed on every line in time with SØ2 as shown in the detail of frame transfer diagram.
13) The OS and DOS outputs both need to have external load resistors to operate. Output load nominally 2.7kΩ external load resistor or 7.5 mA constant current source.
14) Outputs B and C when not used (default mode) should have all biases connected but no externmal load connected to minimise power consumption.
15) Output impedance ~ 350 ohms.
16) Maximum total load ~ 20 pF (typically 10 pF maximum external).
17) On-chip power dissipation ~50 mW per single amplifier (195 mW total with load).

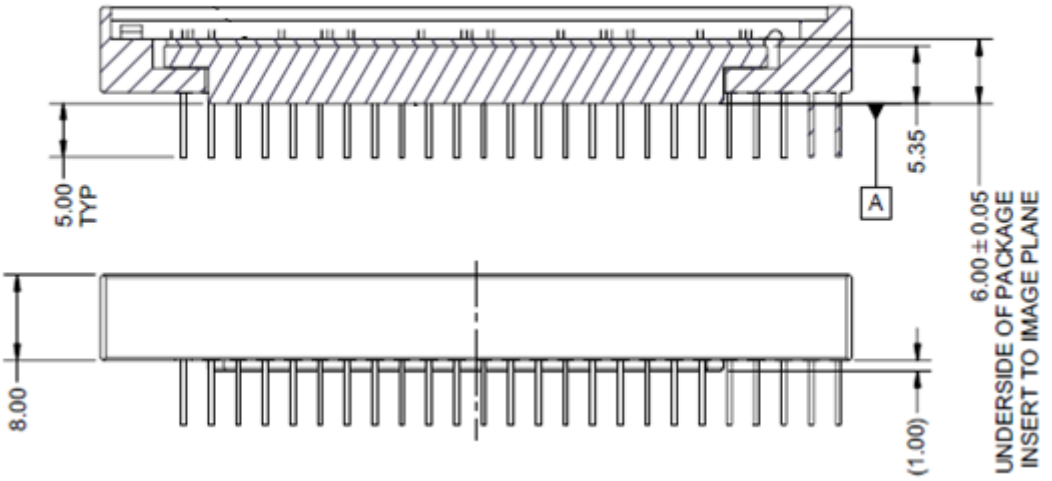
PACKAGE DIMENSIONS

(All dimensions without limits are nominal). Not all dimensions are verified by measurement.





A-A (2 : 1)


5.00
TYP
A
5.35
6.00 ± 0.05
UNDERSIDE OF PACKAGE
INSERT TO IMAGE PLANE
8.00
(1.00)

ORDERING INFORMATION

For further information on ordering and the performance of this device, please contact Teledyne e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- No voltage or charge differential between the device pins and receiving socket pins during installation.
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation. Users planning to operate CCDs in high radiation environments are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	148	-	373	K
Operating	148	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min