TECH BRIEF

Three ways to adjust power consumption and dissipation in your processing systems

March 2020

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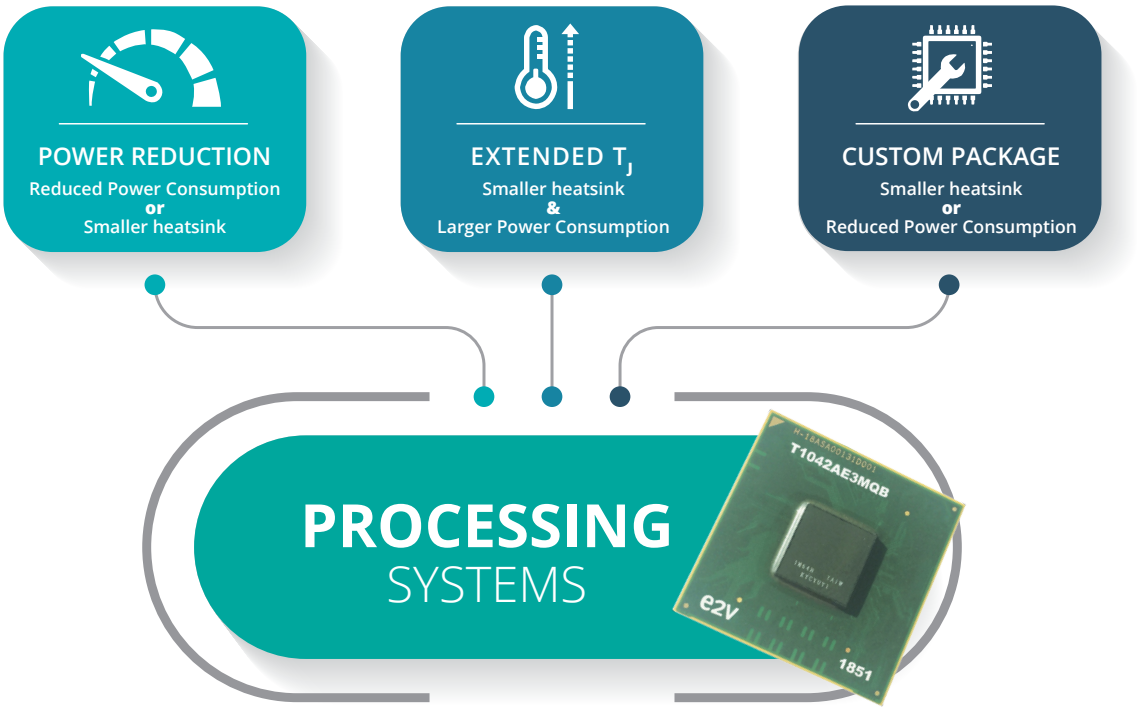

ABSTRACT

Despite the rising power efficiency of new processors, the **accelerating demand for computational power** often **outstrips the ability to cool the systems down** and/or to **provide them the right amount of current.** Furthermore, mechanical/thermal design usually happens late in the development cycle. Consequently, it is **likely to run up against thermal limits late in the design process.** Designers naturally want to optimize their systems and find acceptable tradeoffs.

Teledyne e2v, the **leading supplier of High Reliability microprocessors**, has developed over the years **a core competence to customize processors beyond their standard specifications;** this allows system designers to **increase** both **system's safety margins,** and get **additional SWaP benefits** (Size, Weight and Power).

This paper outlines **Teledyne e2v's tailored approach** proposed to system designers to **adjust power consumption and dissipation** in processing systems using High Reliability processors.

In many cases, selecting one or even a combination of **three degrees of customization** can deliver significant value to the design. The three degrees discussed include:

1. **Power consumption optimization** for a specific customer use case. This consists of **characterizing the processors** versus the **customer application**, prior to selecting those with the **lowest total power consumption.**

2. **Alternative custom package** selection for **thermal resistance optimization.** In most case, this brings as well circuit / die protection.

3. **Raised maximum junction temperature (T_J)** specification can extend operation. This requires **additional qualification work at elevated temperatures** combined with **careful consideration of operating life profile.** The key point is to quantify this, since elevated temperature operation affects device failures in time (FIT rates)

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Teledyne e2v High Reliability Microprocessors have been the workhorses across a broad range of defense, aerospace and other high-reliability markets for several decades now. Meanwhile, contemporary processor advancement is today driven by the demands of other future mass markets such as the extreme number crunching needs of autonomous driving. Thus, the changing economic focus of suppliers, like NXP, has deep consequences for high-reliability supply chains. Not least, that products are engineered with less stringent requirements for many applications.

Meanwhile SWaP (Size, Weight and Power) minimization persists and informs daily decision making of high-reliability system designers working with harsh environments, such as aerospace, defense, or even space. This paper focuses on the selection of processors targeting such roles. Afterall, processors are a strategic component choice representing a large contributor to the total power budget (the P of SWaP). Equally, thermal dissipation drives heatsinking, impacting upon system size and weight goals (the S & W of SWaP).

BACKGROUND ON PROCESSOR POWER CONSUMPTION

Processor power demands have been on the rise with every new generation. Diving into the electricals for a typical device can be a confusing experience except for those who are already pre-armed with an understanding of the system level design issues.

Consider the datasheet extract provided in Table 1, taken from the quad-core ARM® Cortex® A72 64-bit Layerscape® processor, the LS1046. This shows power characteristics for the standard component for two different processor clock frequencies (1.6 & 1.8 GHz) and three different junction temperatures (nominal 65, 85 & 105 °C). Furthermore, three different power modes are indicated: Typical, Thermal and Maximum. Across environmental conditions, it is clear there is practically a doubling in platform power quoted. This highlights that thermal management is going to be a major design topic regarding processor selection.

Furthermore, it is important given that datasheets warrant device performance, a manufacturer's standard specification includes guard-banding or margins to account for process lot variations. So for example, a customer forced by design to use the highest operating junction temperature specified, might on inspecting Table 1 easily conclude that this 'ideal' processor consumes too much power and thus, has to be rejected. However, as will be shown later, there were some power enhancements to be made resulting helpfully in a positive outcome.

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]
							V_{DD}	SV_{DD}[8]	
1800	700/800	2100	1.0	1.0	65	Typical	8.5	0.9	9.4
					85	Thermal	11.4	0.9	12.3
						Maximum	14.3	0.9	15.2
					105	Thermal	14.4	0.9	15.3
						Maximum	17.3	0.9	18.2
1600	700/800	2100	1.0	1.0	65	Typical	7.7	0.9	8.7
					85	Thermal	10.7	0.9	11.6
						Maximum	13.2	0.9	14.2
					105	Thermal	13.7	0.9	14.6
						Maximum	16.3	0.9	17.2

Table 1: NXP LS1046 Processor power consumption specifications.

REVIEWING THE THREE DEGREES OF FREEDOM

Approach 1: Power consumption optimization

This consists of evaluating a population of target components, taking test data and examining the power consumption spread. Ultimately the purpose is to select out only those devices exhibiting the best power consumption characteristics for a given application use case.

Power screening evidence suggests that for some applications when the use case is clearly defined, it is possible to operate a processor well within its operating envelope. However, this requires knowing with greater precision, how the device behaves within the target use case. There is no quick answer to this, but power screening provides the detailed analysis necessary to reach a definitive understanding. In one project, Teledyne e2v demonstrated its ability to source processors with power consumption 46% lower than the worst-case standard product scenario as illustrated in Figure 1, and this by combining characterization of

the cutomer's application and power screening. Here, a device initially believed unsuitable for the task due to assumed excess power consumption, could now be sourced and designed-in with confidence.

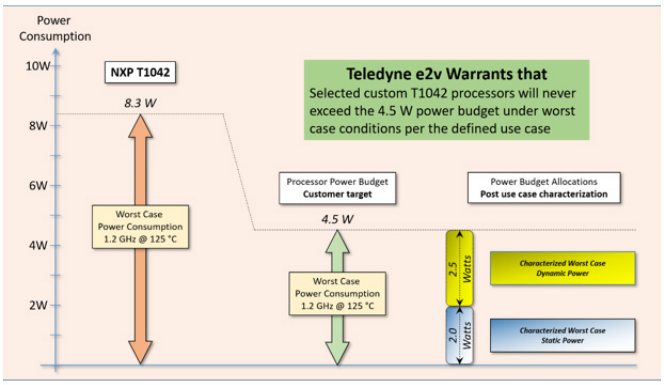

Figure 1: T1042 processor worst case power specification versus customer's target use case.

This will not always happen and to understand that, demands an understanding that power consumption within processors comprises two contributing factors namely:

- Static or quiescent power drain – the power demanded by the IC to supply all its internal peripherals irrespective of any number crunching or code execution taking place
- Dynamic power draw is essentially the computational power consumed. It can vary considerably in multi-core processors depending on the instantaneous computational load.

Unique power insights for Teledyne e2v

Teledyne e2v, with multiple decades of collaboration with NXP and Freescale before that, has built up an enviable knowledge of processor performance and has access to the same tools, product testers and test programs as the original manufacturer. This is the foundation that gives Teledyne e2v a credible and unique background to offer custom device power optimization through screening and characterization as its referred to at Teledyne e2v.
Processor characterisation work performed within Teledyne e2v's manufacturing system has shown that the following characteristics are not at all unusual of current processors:

- Static power demand can vary significantly, device to device
- Static power can be close to zero at cold, but can represent 40% or more of the total power budget at 125 °C (see Figure 2)
- Dynamic power is dictated by the customer's use case. That fortunately varies minimally device to device, over temperature or between process lots

Relationship between processor power consumed and ambient temperature

Figure 2 illustrates the typical relationship between junction temperature and static power consumption observed on a real processor; a higher junction temperature (T_j) leads to the non-linear power characteristic shown. In this example, a 45 °C temperature rise to 125 °C – the nominal maximum, yields a static power increase of ~3x, from ~4W to 14W. Conversely, a good way to reduce power consumption is by reducing junction temperature through enhanced cooling.

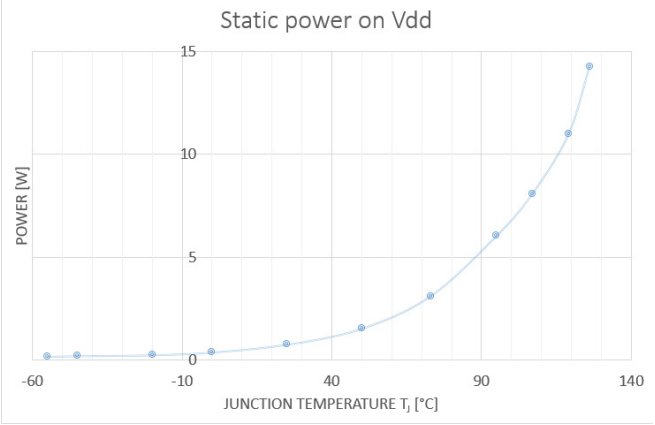

Figure 2: Typical evolution of static power consumption over junction temperature.

From this curve, it is not practical to maximize all processor SWaP elements simultaneously. The curve points to the fact that if power consumption is optimized, then junction temperature must be minimized. That often impacts size and weight since some form of cooling such as heatsinking may be necessary.

So, whilst SWaP is a key design element, sadly a tradeoff is always needed between:

- lowering the power consumed or
- reducing the thermal management system to gain size and weight benefit

Teledyne e2v is well placed to deliver power optimized microprocessor components

Thanks to access to both NXP original test programs, equivalent testers and the skills in-house to modify environmental conditions and develop enhanced product specifications, Teledyne e2v can work to guarantee a custom power specification. Furthermore, Teledyne e2v can perform a deep technical power analysis of a customer application noting especially its dynamic power requirements.

Outcome: Power consumption reduction

Figure 1 charts initial customer assumptions in respect to a T1042 quad-core processor under consideration for a low power design environment. The commercial specification indicated a worst-case power budget of 8.3 W (with 1.2 GHz clock and T_j = 125 °C). However, the customer had a hard power budget limit of 4.5 W. At the outset of their project it looked unlikely that they could confidently select the T1042.

Armed with enhanced product testing data and Teledyne e2v's analysis of the customer use case led to a conclusion that the company could guarantee the supply of specially selected devices consuming almost half the power originally anticipated.

Overall this approach can help reduce power consumption or simplify a project's thermal design.

Approach 2: Custom packaging

This consists in modifying or redesigning the existing standard product package to lower its thermal resistance from junction to board, or junction to package top:

- Can be used to reduce the junction temperature, thus lowering power consumption (assuming the same heatsink remains in place). Alternatively, reduces the cooling system (size/weight) since the package thermal resistance (R_{th}) is lower, that of the heatsink can be larger.

- An alternative package can enhance vibration protection for the component and/or simplify and improve the thermal interface between the cooling system and the processor.

- To deploy a lid or not to further impact thermal performance.

A lid is the cover that is found on most processors which acts as a heat spreader and protection for the component's die. However, depending on the application, some designers might want a lid to help integrate a heatsink more easily. Others prefer a lidless design because they can't accept the extra thermal resistance of the lid. Also, note that a lid dramatically reduces the junction to board thermal resistance, a clear benefit if it is desired to conduct more heat through the printed circuit board (PCB).

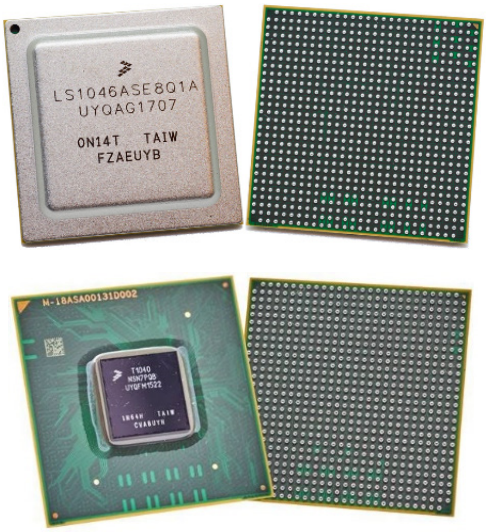

Figure 3: LS1046 lidded design [Top], T1040 lidless design [Bottom].

Some components are delivered with lids (e.g. LS1046), others come without (e.g. T1040), see Figure 3. Usually the designer doesn't have a choice because with 'commercial off the shelf' (COTS) components, both versions are rarely available. That's where Teledyne e2v has the flexibility to help, by proposing to add or remove a lid.

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Teledyne e2v is well placed to deliver custom packaging

Teledyne e2v has specific knowledge and experience repackaging semiconductor components. This includes but is not limited to specific package development projects, for example a package developed especially for the Teledyne e2v EV12AQ600 Analog to digital converter. Moreover, Teledyne e2v has in-house expertise to handle the re-balling of packages to allow for solder formulation changes to suit the tin-lead alloy free needs of some space customers (e.g. to protect against tin whiskers forming in space).

Outcome: Custom packaging

A feasibility study was recently performed to add a lid to the NXP T1040 processor. A mechanical proposal for the optional lid was made (see Figure 4), and revised thermal specifications were estimated. Thanks to the lid, the junction to board thermal resistance is expected to roughly halve to 4.66 °C/W with the lid, down from 9 °C/W for the standard device. In that case, the junction to top thermal resistance increases due to the addition of the lid, from less than 0.1°C/W to 0.85°C.

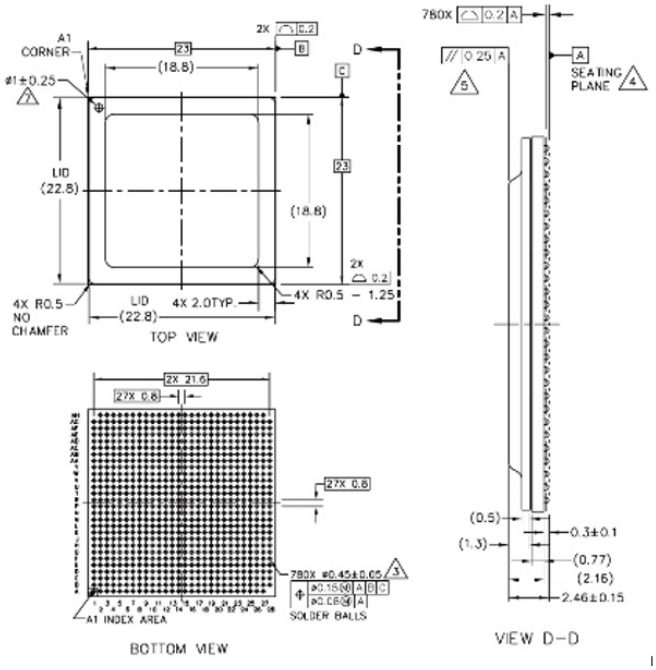

Figure 4: Proposal of optional cover (lid) for T1040.

Further thoughts on package improvements

The ideal thermal design is operable without a heatsink where all heat is conducted just through the PCB. Though unrealistic in many cases, it is still possible to consider alternatives to the commercial standard package in some applications to get a marginal gain. Modifying the package to reduce the thermal resistance from junction to PCB might be enough given that multi-layer PCBs offer a low thermal resistance, a fair portion of the heat can be conducted through the PCB, relieving the constraints on heatsink design, or reducing the power consumption with the same heatsink (through lowering the junction temperature). One example of what is possible at Teledyne e2v is the PC8548 (on ceramic substrate). This is equivalent to the MPC8548 (plastic substrate) available from NXP. Though looking similar and identical in size, they differ substantially with respect to thermal performance. Thanks to the ceramic substrate of the PC8548 the thermal resistance from junction to board is 60% lower (@ 3°C/W) than the plastic version (@ 5°C/W).

Although both these examples focus on lowering the junction to board thermal performance, a similar approach can be taken to reduce the junction to package top thermal resistance.

Approach 3: Extended (i.e. > 125 °C) junction temperature

This optimization considers the viability of operating silicon beyond conventional thermal limits of commercial, standard products. Certainly, silicon is not physically limited to operate only up to 125 °C, several elevated temperature applications exist and are already served. The benefit of higher junction temperature operation is the extra thermal headroom on offer. But, as seen earlier, elevated temperatures have an implied penalty namely significantly raised power dissipation (see Figure 2). Where a higher junction temperature can pay off is in applications with an operating profile requiring short bursts of increased dynamic power, yet it is critical these bursts can be handled within the thermal capacity of the design.

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Teledyne e2v is well placed to deliver extended temperature

Thanks to in-depth product knowledge and testing experience, combined with product qualification infrastructure, Teledyne e2v can explore in detail with customers the likely operating life impact of choosing extended temperature operation. It's an existing capability served by the company, given that Teledyne e2v already supplies NXP processors guaranteed up to 125 °C - an advance over the commercial device's 105 °C limit.

Outcome: Extended temperature

Following a positive viability evaluation, Teledyne e2v can supply a custom IC specification at elevated operating junction temperature levels. This specification will be delivered in a manner that comprehends careful consideration of the following four operating factors.

Four factors of extended junction temperature operation

To increase operating junction temperature four important topics need be evaluated:

- **Functional performance:** At higher temperature, a processor might not meet all its electrical requirements. Teledyne e2v characterization shows that maximum clock frequency may need to be reduced to comply with datasheet electricals (see Figure 5). Thus, some specifications might need to be scaled back compared to the standard component if it is to be successfully used over the extended temperature range.

- **Reliability:** Reliability for silicon components decreases rapidly and non-linearly as temperatures rise. This is defined in literature by a modified Arrhenius 'reliability' equation. Figure 6 shows typical FITs (Failures-In-Time) from NXP processors operating up to +105 °C. Extrapolating these out to +150 °C, reliability drops by a factor ten compared to +105 °C FITs. Such a drop in reliability has to be acceptable in the target application.

- **Power consumption:** As shown in the Figure 2, power consumption increases exponentially with temperature, which means that operating in the extended temperature zone implies the acceptance of considerably higher power consumption.

- **Packaging ability** to sustain high temperature operation needs to be verified. Plastic epoxy packages in particular, start to deteriorate beyond about 160 °C. Repackaging with high temperature epoxies would be a mitigation strategy here.

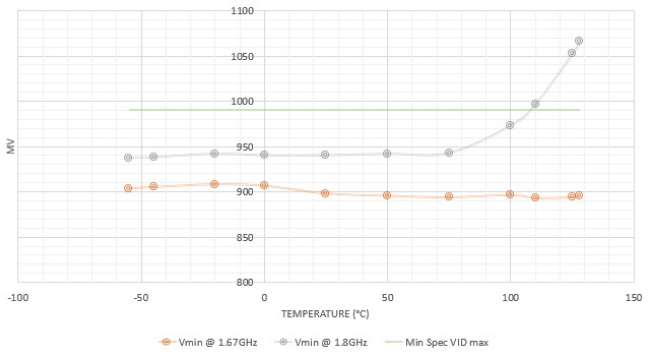

Figure 5: Example of 1.8 GHz clock frequency limitation at high temperature (>100°C).

Qualifying the above four factors can precede a positive decision to extend the upper thermal limit on a device in a specific application, making appropriate changes to the guaranteed electricals, and packaging materials. The ability for Teledyne e2v to support custom requests is highly dependent on the customer's understanding of their mission and operating lifetime profile. Knowledge of how long the extended temperature condition should persist; whether for some applications the high temperature conditions are merely transient or represent a steady-state condition will make or break this as a viable option. Irrespective of these factors, Teledyne e2v is well placed to provide advice.

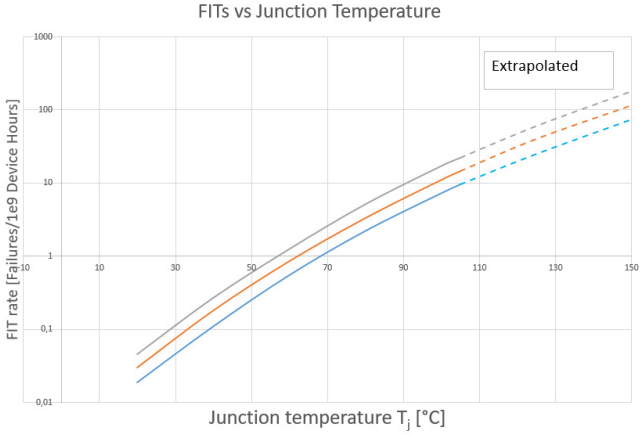

Figure 6: Typical FIT rates versus temperature extrapolated out to 150 °C.

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THREE DEGREES OF FREEDOM AID SOURCING POWER OPTIMIZED PROCESSORS

This paper has discussed how Teledyne e2v, building on its long-term strategic relationship with NXP is uniquely positioned as a trusted supplier of customized processor options. Customization is possible based on either the power architecture (e.g. T series processors such as the T1042) or ARM architecture (e.g. Layerscape LS1046). Outlined here were three degrees of freedom to power optimize and customize processors for harsh applications. These three options are:

- Definitive power screening for optimal, use case specific power consumption
- Alternative custom package selection for enhanced thermal handling capability.
- Raised maximum junction temperature (T_J) to support raised dynamic power demands

Owning independent test and qualification infrastructure and having access to skilled product engineers combined with a preferential, long term supply agreement with NXP gives Teledyne e2v an edge when offering specialized, high-reliability, power optimized processor solutions for specific customer use cases in complex applications.

If you remain unsure whether a bespoke processor solution is the right choice, we encourage you to connect with Teledyne e2v to discuss the specifics of your current challenge. You just might be surprised by the value customization brings to your design.

LEARN MORE:

> Teledyne e2v helps reduce power consumption in commercial processors.
> Teledyne e2v Hi Reliability Differentiators for Microprocessors.
> Teledyne e2v is introducing Quad ARM® Cortex® A72 for Space applications.
> Qormino packaged processing solutions will operate in a 100% Aerospace product application environment.
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