

# A Novel Sensor for High Resolution Earth Observation

## TDI CMOS Imaging Sensor: CIS125

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A new image sensor based on ground-breaking technology to deliver a high resolution (0.5m) and improved performance Earth Observation (EO) satellite.

A TDI CMOS image sensor offers a number of significant performance advantages over the existing CCD based solutions:

### Smaller pixel size

Pixel size can be down to 5µm or even lower enabling large numbers of pixels to be included in a single sensor (up to 24,000 wide).

### More spectral data

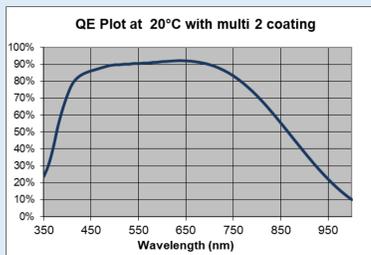
The number of spectral lines can be increased to up to 8 giving 2x the spectral data available from any existing CCD based detector.

### Increased line rates

As the digitisation can be operated at very high speeds, line rates of over 40kHz can be achieved, to give very high resolution images.

### And with no reduction in QE

The backthinned TDI CMOS being developed by Teledyne Imaging will have a quantum efficiency almost identical to the equivalent CCD based system.



These image sensor advantages lead to critical improvements in the overall system:

### Lower power consumption

In addition to the reduction in power consumption obtained in the image sensor the fact that the output is already digitised significantly reduces the power dissipated on the platform.

### Reduced weight

One TDI CMOS image sensor replaced two of the CCD sensors making a smaller focal plane. The reduced power consumption and much simpler electronics also significantly reduces the total weight. The smaller pixel size available also allows smaller focal planes to be used.

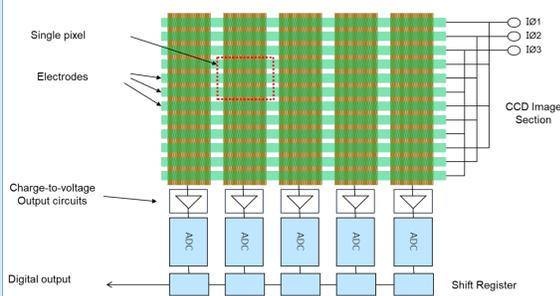
### Ease of integration

The TDI CMOS sensor requires only 1.8V and 3V supplies with no large currents and voltage. The digital output also removes one of the most complex parts of the electronics as well as simplifying the optics.

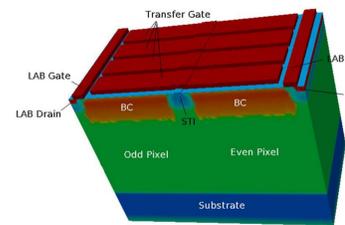
The payload development described here is a collaboration between Teledyne e2v, Surrey Satellite Technology Ltd (SSTL) and the Centre for Electronic Imaging (CEI – The Open University).

## How TDI CMOS Works

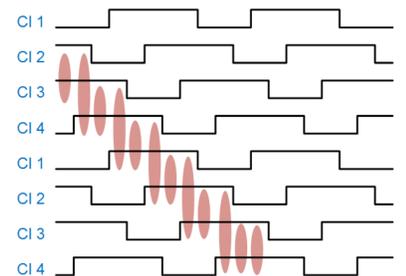
A CMOS TDI detector consists on a image area that is essentially a CCD made using a CMOS process with CMOS readout electronics including the analogue to digital conversion on each column



The challenge has been to establish a process using standard CMOS technology that can achieve very high charge transfer efficiency and peak signals with the reduced voltages available in CMOS technology. Teledyne have developed a pixel design where charge transfer efficiency between pixels is comparable to CCDs and a high full well capacity is achieved.



These can be clocked in a similar manner to a CCD.



For these detectors, an output and ADC exists on each column to convert the charge to a digital signal

## High Resolution Colour

EO TDI devices are typically constructed from a number of different arrays:

PAN arrays are used to provide maximum spatial resolution with smaller pixels using broadband illumination to improve the SNR.

Multispectral (MS) arrays have larger pixels which provide lower spatial resolution, but use narrower bandwidth illumination to define colour.

The images from these arrays can be combined to provide high-resolution, colour images.

## Architecture

The chip designed within the CEOI project uses:

- Four 5µm Panchromatic (PAN) staggered in column and row directions to increase spatial resolution by a factor two
- Eight MS channels of 10µm pixels for up to 8 different colour channels
- Analogue to Digital Converter (ADC) on each column to provide fast, digital conversion and assist high-speed read-out
- 16k columns to give a large swath width (9km)
- Selectable row length from 1 to 64 in PAN and 1 to 32 in MS to avoid saturation
- Up to 12 bit digital resolution for contrast detail
- Backthinned and AR coated at Te2v for high quantum efficiency and improved Signal-to-Noise Ratio (SNR) across the spectrum of interest
- Low reflection light shield to prevent ghost images
- Anti-blooming to prevent charge spilling in high contrast images



## Heritage - A prototype test achieved the following results.

| Feature             | Unit      | Target           | Measured         |
|---------------------|-----------|------------------|------------------|
| Pixel pitch         | µm        | 5 & 10           | 5 & 10           |
| Vertical resolution | Pixels    | 256              | 256              |
| Bi-directionality   |           | Required         | Demonstrated     |
| CTE / gate          |           | > 0.99998        | > 0.99999        |
| FWC - 5 µm pixel    | electrons | > 20 K (Non-AB)  | > 30 k (AB)      |
| Noise Floor         | electrons | < 15             | 12               |
| Max line rate       | kHz       | > 300            | 270 confirmed    |
| Dark Current @ 25°C | nA/cm²    | < 10             | 3.7              |
| Non-linearity       | %         | < 2              | < 2              |
| ADC                 | bit       | 12               | 12               |
| Read-out rate       |           | 8 ports 3.6 Gb/s | 8 ports 3.6 Gb/s |

## Radiation Results

The limiting factor to a device's usable lifetime in space is radiation damage which causes an increase in dark current (a noise contributor), defect pixels and a degradation in Charge Transfer Efficiency (CTE); as such it is vital that a device is radiation tolerant.

The test chip has been exposed to gamma and proton radiation to represent a space environment and has achieved the following results:

