High Resolution Charge Domain TDI-CMOS Image Sensor for Earth Observation

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ABSTRACT

Earth observation (EO) is a rapidly expanding area of space science and technology, fueled by the demands for timely, comprehensive and informative data for an increasing number of applications. With the increased affordability of satellites EO is becoming accessible to a larger pool of commercial developers and users.
Presently there does not exist in the market a low cost payload with the performance required to meet the growing demands of the commercial 'New Space' EO market (very high resolution, good quality image, low mass and low recurrent cost).
The presentation will discuss the characterization results of a novel TDI-CMOS silicon prototype as well as a description of the current flight model design currently being developed under the CEOI EO technology and Instrumentation program funded by the UK Space Agency. This sensor will be a key enabling technology for the high resolution new space payload.

Keywords: EO, Earth Observation, New space, charge domain TDI, qTDI, CMOS, Back illumination, PAN, MS, focal plane.

1. INTRODUCTION

Teledyne e2v, a Teledyne Technologies company, in partnership with Surrey Satellite Technology Ltd (SSTL), and the Centre for Electronic Imaging (CEI) at The Open University (OU), has been awarded a contract to develop technology building blocks of a low power and high resolution CMOS image sensor tailored to address the small satellite Earth Observation (EO) market.
Under the contract (awarded by the UK Space Agency via the Centre for Earth Observation Instrumentation), Teledyne e2v, in collaboration with other organizations within Teledyne's Imaging Group, will lead the development of new technology which will simplify EO satellite system design using CMOS Time Delay and Integration (TDI) image sensors.
Teledyne's CMOS TDI modular platform brings small pixels, high line rates, and on-chip functionality, including digital outputs, to enable cost-effective small satellite optical payloads. The technology will support many emerging EO applications such as land use mapping, urban infrastructure, agriculture, national resource management, disaster management, maritime, security, and surveillance – applications which are not well served with traditional sensor solutions. This latest development will contribute key building blocks to the industry-leading technology that Teledyne Imaging can offer to the global space market.
In conjunction with SSTL's world-leading experience in building very high-resolution small satellite imagers and the OU's capabilities in sensor characterization and testing, Teledyne e2v will deliver an EO imaging system that demonstrates a more affordable space asset cost for customers looking at 0.5 meter systems and applications.
Although traditional Charge Coupled Device (CCD) technology continues to deliver the very highest performance for many demanding applications, some key benefits of CMOS TDI image sensors are:

- Reduced power consumption
- Increased on-chip integration and functionality
- Reduced size, volume, and cost of the complete sensor and front-end electronics

By leveraging these benefits, larger constellations can be launched to achieve higher temporal resolution.

2. AN OVERVIEW OF THE SENSOR AND ITS TECHNOLOGY

CIS125 is the Teledyne qTDI (charge domain TDI) sensor being designed in CMOS technology as part of the CEOI EO technology and Instrumentation program funded by the UK Space Agency. The architecture developed is reported in Figure 1. This qTDI detector is composed of 4 panchromatic (PAN) bands and 8 multi-spectral (MS) bands. The configuration reported here is optimised for the CEOI program and each PAN and MS are composed of sub-TDI bands (A&B) that to enhance the full well by adding digital summation to the charge domain performance. The PAN and MS number of TDI lines were carefully chosen to optimise application needs versus silicon area. Each sub-TDI needs to be read out separately and therefore needs its own conversion. This is the equivalent of reading out 16 independent bands. This implies that each quarter of line is dedicated to the conversion of a 1 PAN and 1 MS as shown Table 2 and Figure 3.

The pixel, Figure 2, is a CCD structure, with gated anti-blooming (AB). This sensor is a stitched device of 16k columns for the PAN and 8k columns for the MS. The pixel is 5µm and 10µm for the PAN and MS respectively, see Table 1. To speed up the frame rate the sensor uses high speed ADC per column allowing 12 bits conversion in $0.9\mu s^3$. This is an ADC single slope architecture with a counter generating ten Gray codes and four phase-shifted unary codes providing 12 bits output in total at very high line rates. The column readout path is illustrated Figure 4. A single read path is shared between all bands enabling to implement a maximum number of bands without the need of 2D stitching technology and optimising power consumption. The data resulting of the image conversion is then sent to a gigabit transmitter (GTX) composed of a serialiser working in double data rate mode (DDR) at 3.6GHz operation and CML (2.8Gb/s) data driver. The high speed CML output driver standard has been selected to minimize the number of output reducing the complexity of the front end electronics. Input signals such as clock, integration control and SPI interface are using LVDS format.

The number of TDI stages per bands is select-able as follow:

- Each sub-TDI PAN array can be programed in the following steps: 1, 4, 8, 16, 24, 32, 48 and 64.
- Each MS array can be programed (independently for each MS) in the following steps: 1, 2, 4, 8, 12, 16, 24 and 32.
- For the secondary, shorter sub-TDI sections (PANBs with 32 and MSBs with 16), will mirror the options of the primary ones, for the available number of lines.

This sensor will be made with a 0.18µm Imaging CMOS process using thick and high resistivity epitaxial silicon. The device is back-illuminated to improve fill factor and it will be thinned (using Teledyne-e2v process) to optimise QE versus MTF. To enhance further it performance an Anti-reflection coating will be deposited as well as black-coating between channels to avoid straight light effects.

CIS125 is designed as a modular platform to enable to adapt to a wide range of configuration with lower risk associated to new development.

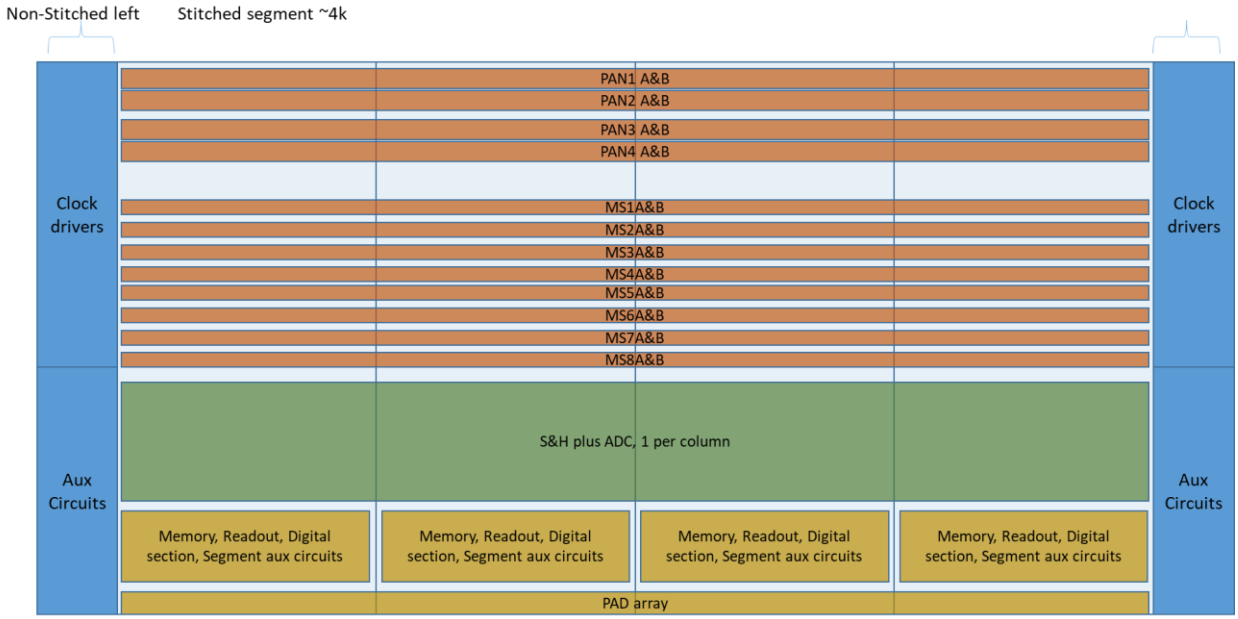

Figure 1 Sensor Architecture

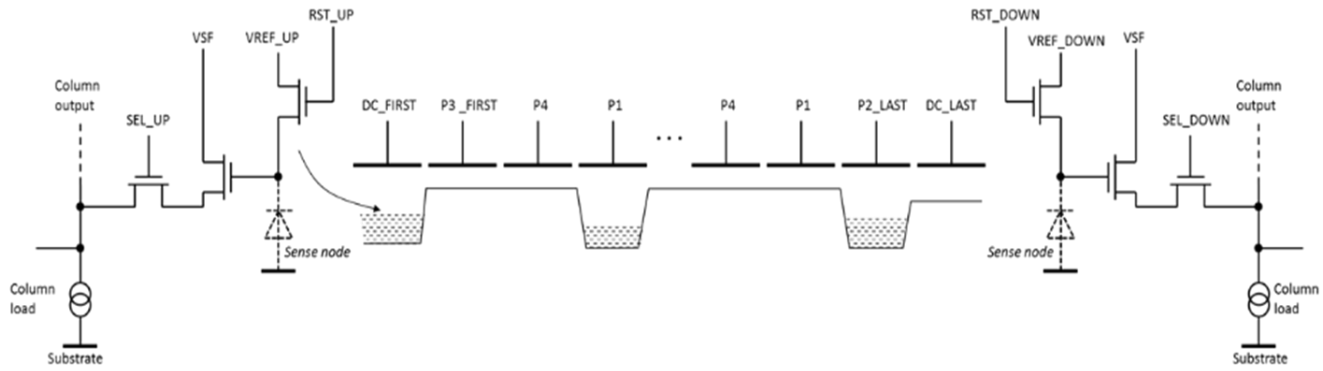

Figure 2 Pixel schematic.

Pixel count		Pixel size (µm)		Line rate (kHz)		Prototype
PAN	MS	PAN	MS	PAN	MS	
16k	8k	5	10	14	7	2019

Table 1 Configuration for CIS125.

1/4LT			1/4LT			1/4LT			1/4LT			1/4LT			1/4LT			1/4LT			1/4LT		
P1A	P1B	MS1A	P2A	P2B	MS1B	P3A	P3B	MS2A	P4A	P4B	MS2B	P1A	P1A	MS3A	P2A	P2B	MS3B	P3A	P3B	MS4A	P4A	P4B	MS5B

Table 2 PAN and MS readout timing organisation.

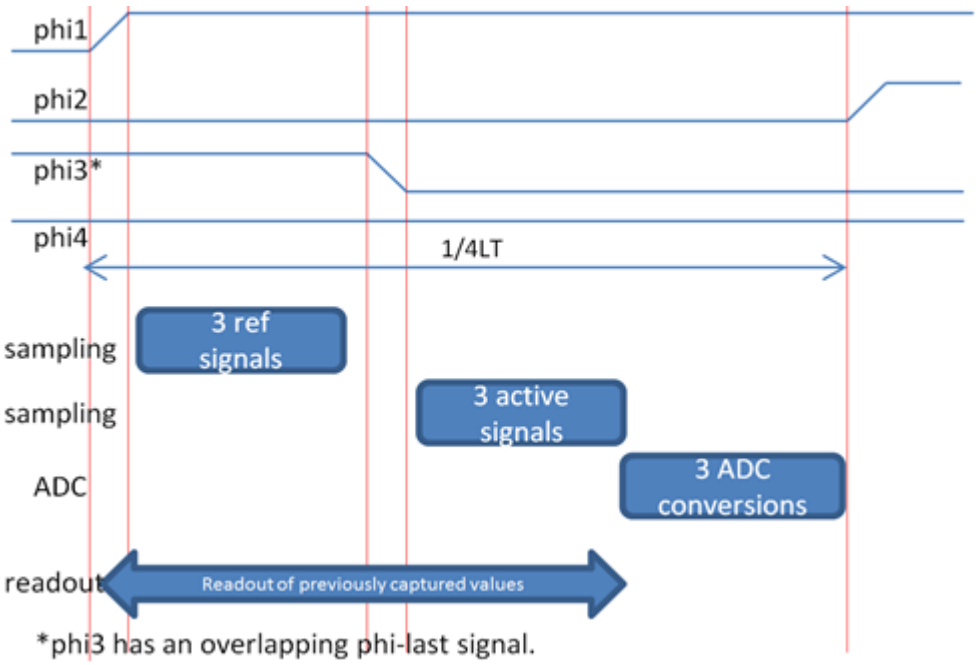

Figure 3 Example of timing access to the sensor CIS125.

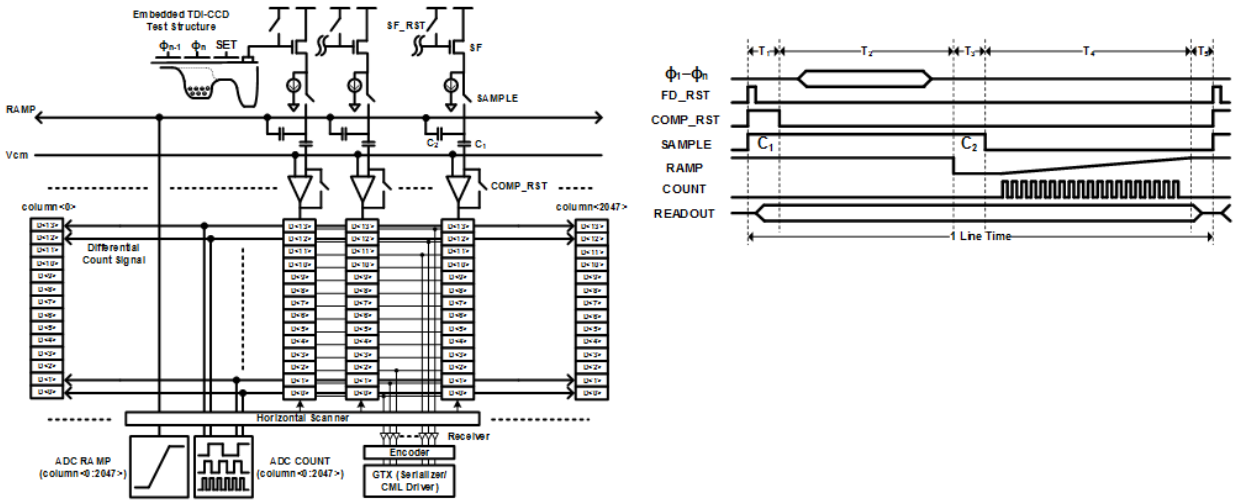

Figure 4 High speed ADC readout diagram and timing.

The pixel architecture is represented Figure 2. It is a 4 phase CCD structure with minimum poly-poly gap (0.25µm). The pixel is bi-directional with two identical output ports at either end of the CCD structure. This structure is based on a buried channel implentation to achieve good charge transfer efficiency (CTE) and to minimise post radiation degradation as seen with surface channel approach.
The clocking of the CCD phases are overlapping as shown Figure 5. The green rectangle represents the movement of charges. The transfer of direction can simply be achieved by swapping two of the clocks. This feature is accessible via an SPI interface. Gate voltage and clock slew rate are optimised for best full well capacity and CTE trade-off.

The clock generator and drivers are embedded in the chip making greatly simplifying the integration of this detector. Note that carefull lay out technics are used to obtain correct clock slew rate and avoid IR drops due to current demand during switching activity.

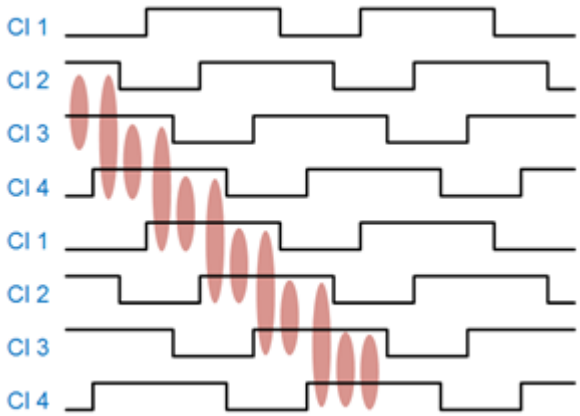

Figure 5: CCD structure phase clocking.

Parameter	Performance
Pixel size: PAN/MS	5µm/10µm
No. of Pixels PAN/MS	16,384/8,192
PAN FWC	60,000
No of PAN channels	4
MS FWC	~106, 000
No. of MS channels	8
PAN TDI Steps	64
MS TDI Steps	32
RMS Noise (PAN)	<30e (with digital summation)
Line rate	baseline ~14k
Dark signal at 14kHz (PAN) at 20°C	~70e (64 rows)
MTF	55%
QE	Teledyne-e2v standard backthinned
Dynamic Range (dB)	72
Outputs	CML (up to 2.8Gb/s)
Power	< 10 W
High frequency clock generator	On-chip
ADC	On-chip/Column ADC
Column ADC	At least 12 bits
Encoding	On-chip
Internal summation in case of multi PAN	No
Radiation	Latch-up immune up to at least 80MeV.cm^2/mgSEU immune up to 40MeV.cm^2/mg for data storage SEU immune up to 80MeV.cm^2/mg for configuration and state machine
Pin/PAD count	< 500
Backthinning	Yes
Inter-band black-coating	Yes

Table 3 Performance target.

3. PROTOTYPE DEVICE EXPERIMENTAL RESULTS

3.1 Electro-optical performance

The implementation of good CCD structure in CMOS represents several challenges of which the two mains ones are obtaining good CTE and high enough full well. In that respect and compared to CCD the limitations of CMOS technology to be overcome are non-overlapping poly gates and lower supply voltages. The former affects the CTE and the later the FWC. In addition and similar to CCD technology a surface channel CCD structure although giving higher full well will suffer from high CTE degradation end of life (EOL) worsening drastically MTF performance. This is because trap generated at the silicon surface will trap and release electron at different clock phases. Hence all the CCD structure pixels uses buried channel despite the loss of Full Well. In order to overcome the lower supply voltage of CMOS technology negative supplies used to increase the potential across each pixel. More importantly it helps reducing the dark current. It can be noted that summing in the digital domain two of the CCD structure, also called sub-TDI array earlier in this document, is recommended to increase the signal noise ratio. This is because while the total charge is added in a linear fashion the noise is added in root square fashion only.

A summary of the main results are proposed below and can be found in more details in reference below[1]. On a 5µm pitch CCD structure with anti-blooming a FWC of 30ke- was measured with a CTE better than 0.99999. The signal linearity achieved is with 2% while dark current performance 3.7 nA/cm2 with a temperature doubling factor of 9.5^{o}C. The Arrhenius plot indicates a activation energy (E_a) of 0.6eV. This corresponds to half the silicon mid-band gap confirming that the dark current source is the conventional Shockley-Read-Hall (SRH) mechanism. The charge conversion efficiency graph shows a pixel conversion gain of 35µV/e-. This gain is designed to optimise noise floor versus full well hence dynamic range.

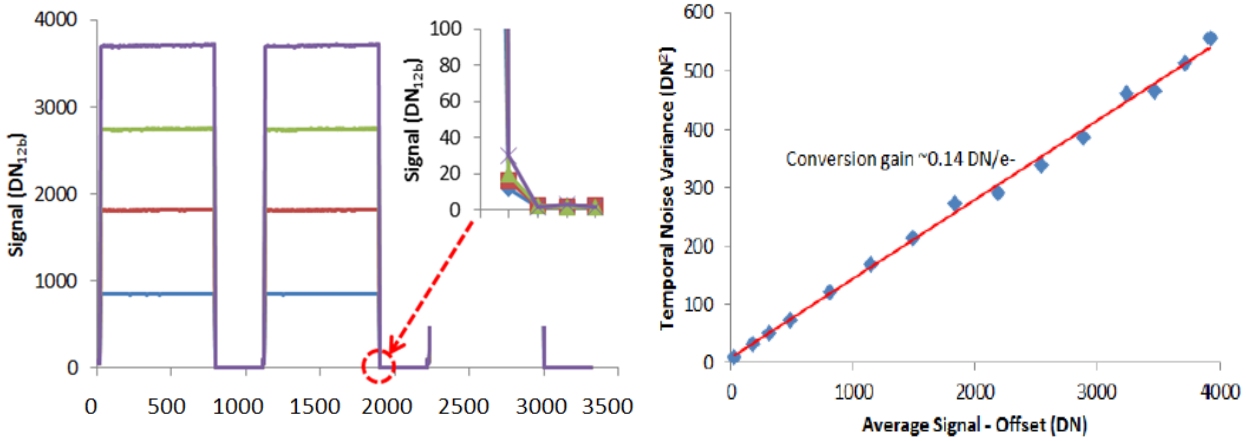

Figure 6 Left CTE measurements and right PTC.

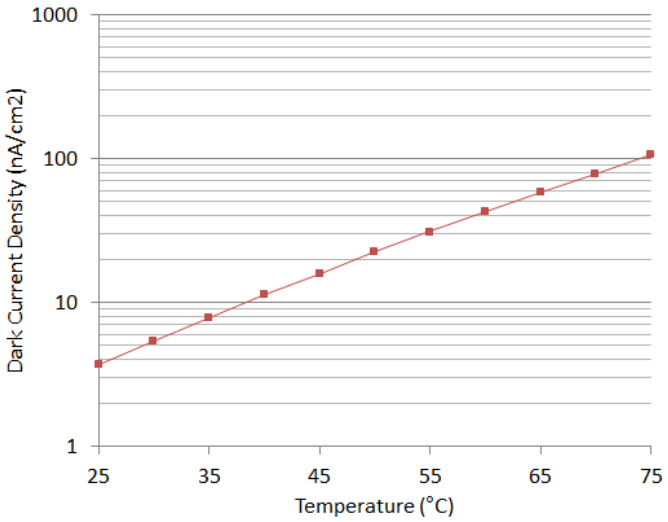

Figure 7 Dark current.

3.2 Radiation

The radiation immunity or degradation model is a key aspect of validation of a new technology. In the context of the qTDI detector two aspects matters: the CCD structure behaviour with Gamma and Proton and the readout periphery immunity to Heavy Ion. Below shows results obtained on these two aspects.

CCD structure

For the CCD structure the concerns are mainly around two parameters dark current (including bright pixel) and CTE performance degradation when subject to Gamma and proton radiation. The results[4] below show a good behaviour with acceptable results for a flight mission.

The Gamma radiation increased the dark signal of the Non-Anti-bloomed (AB) split by a factor 2 at 30krad while the AB split dark signal triple. This could be explained by the fact that AB split has less STI and less active area but has more gate edges and poly gaps (Non-continuous poly gates). A similar observation is made after the proton irradiation, see table for details. The higher increase for the AB splits is also explained by the higher level of gate edges.

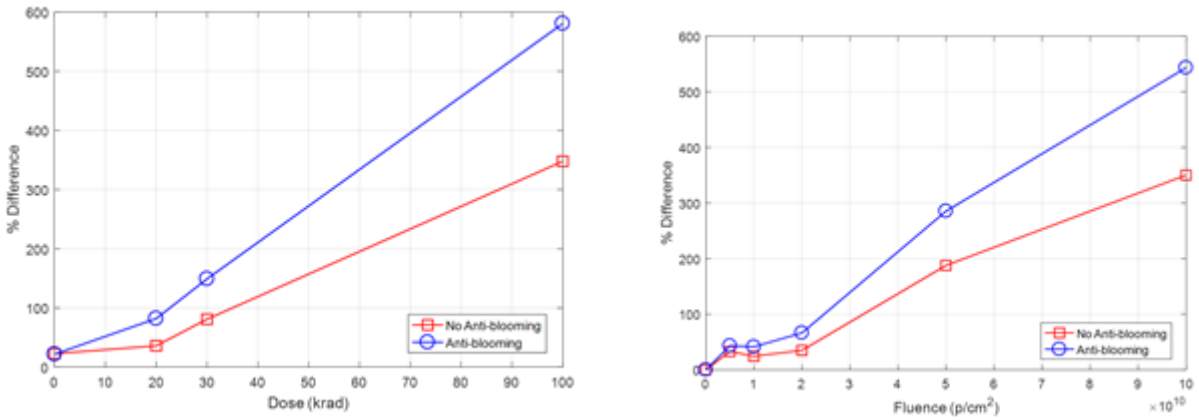

Figure 8 Post radiation dark current: Left is post Gamma and 7 days rest; right is post Proton and 14 days rest.

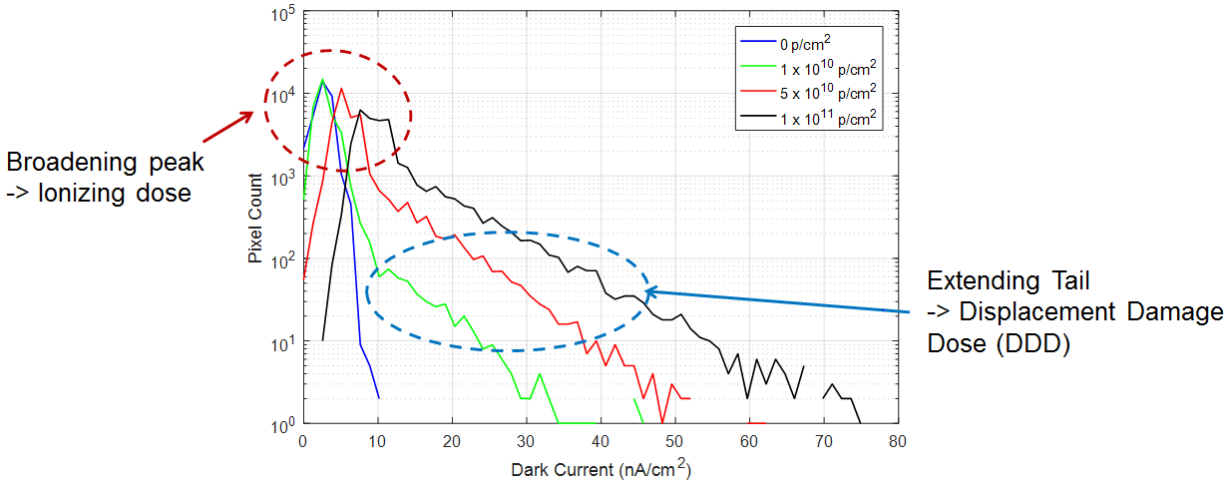

Figure 9 Bright pixel post proton and 14 days rest.

	Pre-radiation	Post Gamma 30krad	Post proton - 5x1010 p/cm2
Without AB	3-4nA/cm^2	< x2	<x3
With AB	3-4nA/cm^2	~x2.5	<x4

Table 4 Dark current summary at 30krad and 5x1010 p/cm2 Proton exposure.

The results below show a very small and similar CTE degradation of both the AB and non-AB versions of the prototype device with Gamma and proton up to doses that would be expected in typical space based applications. Note that the "version 2" is a variant of the baseline "version 1" to improve CTE.

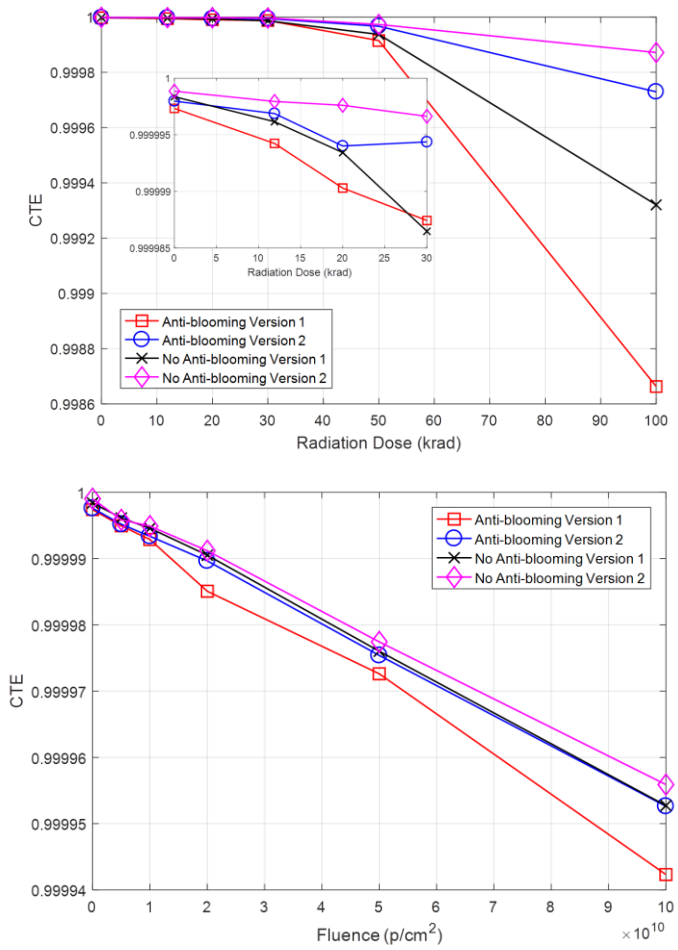

Figure 10 CTE versus at the top Gamma and at the bottom Proton.

Single Event Effect (SEE)

Usually, the SEE is categorized in:

- Non-destructive
  - Single event upset (SEU) – change of logic state in memory element.
  - Single event transient (SET) – transients in circuit that lead to erroneous data being captured.
  - Single event functional interrupt (SEFI) – temporary loss of device functionality (for an imager of this simplicity, this is caused by bus contention).
- Potentially Destructive
  - Single event latch-up (SEL) – a parasitic thyristor causes circuit lockup or catastrophic failure.

Teledyne has developed design rules and layout rules that have secured several projects such as MTG or METImage giving high immunity to heavy ion. These results have been reported in details at the ICSO conference 2016[5]. Below is given the summary table.

	LETth ($MeVcm^2mg^{-1}$)	Mission rate (day^{-1})	Reliability over 8.5 years (%)	Comments
SEL	> 67.7	< $2x10^{-6}$	99.2	This worst case as no latch-up was actually observed
SEU rad-hard register	65	< $4x10^{-12}$	99.9999	Sequencer, timing and readout control
SEU low power register	19	< $1x10^{-8}$	99.996	Serial programmable interface

Table 5 MTG-FCI results[5].

4. SUMMARY

The CIS125 qTDI CMOS image sensor for high resolution earth observation has been presented:

- Large number of bands PAN and MS.
- High conversion rate allowing high line rate with single row of ADC maximising the number of bands on silicon.
- Highly integrated simplifying the front electronic and reducing size and power consumption at system level.

In this paper has also presented the performance of the CCD structure used and demonstrated high TRL level:

- CTE of 0.9999 and Full Well of $30ke^-$ for 5µm pixel pitch and high line rate.
- Other performance such as dark current or linearity been within expectation.
- Post radiation Gamma and Proton performance and especially CTE and dark current having a reasonable degradation and therefore acceptable for flight model.

5. ACKNOWLEDGEMENT

We gratefully acknowledge support from the UK Space Agency via the Centre for Earth Observation Instrumentation.

6. REFERENCES

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