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INTRODUCTION

e2v technologies L3Vision® CCD sensors use a novel charge multiplication technique to facilitate gain in the charge domain and enable performance with an equivalent output noise of less than 1 e⁻ at pixel rates of over 11 MHz. Thus the sensors are excellently suited for scientific imaging where the illumination is limited, or for TV applications at very low light levels.

This technical note discusses how the CCD operating conditions can be optimised, maximising device performance.

CLOCK WAVEFORMS AND TIMINGS

Suggested clocking schemes and clock rise and fall times are shown in the product data sheets, and the phase relationships of the register clocks are illustrated in Figs. 1 and 2.

When implementing the clocking schemes, the following points should be noted:

- For operation at readout frequencies in excess of 1 MHz, it is more straightforward to employ a sinusoidal R∅2HV than a square wave clock pulse. Implementation of a resonant sinusoidal clocking scheme will also reduce power dissipation.

- The R∅2HV voltage level at the time of charge transfer is critical for obtaining stable multiplication gain. For example, for operation with a gain of 1000, a stability of ± 30 mV is required to maintain the gain within $\pm 5\%$.

- If sinusoidal R∅2HV clocking is implemented, care is required to optimise the register clock timings. The peak of the R∅2HV sine wave should correspond to the falling edge of the R∅1 clock pulse. Incorrect timing of R∅2HV may result in reduced gain, poor charge transfer efficiency and impaired signal linearity performance.

- If square wave R∅2HV clocking is implemented, the requirement for maximised multiplication gain and optimum charge transfer is that R∅2HV is stable at the clock high level when R∅1 falls and the charge transfers.

- For operation in inverted mode/2-phase mode, the image and store clocks should overlap at a level not less than 90% of the clock amplitudes. For operation in non-inverted mode, image and store clock overlaps should be at not less than 50% of the clock amplitudes. Overlaps of the conventional register clocks R∅1, R∅2 and R∅3 should be at not less than 50% of the clock amplitudes.
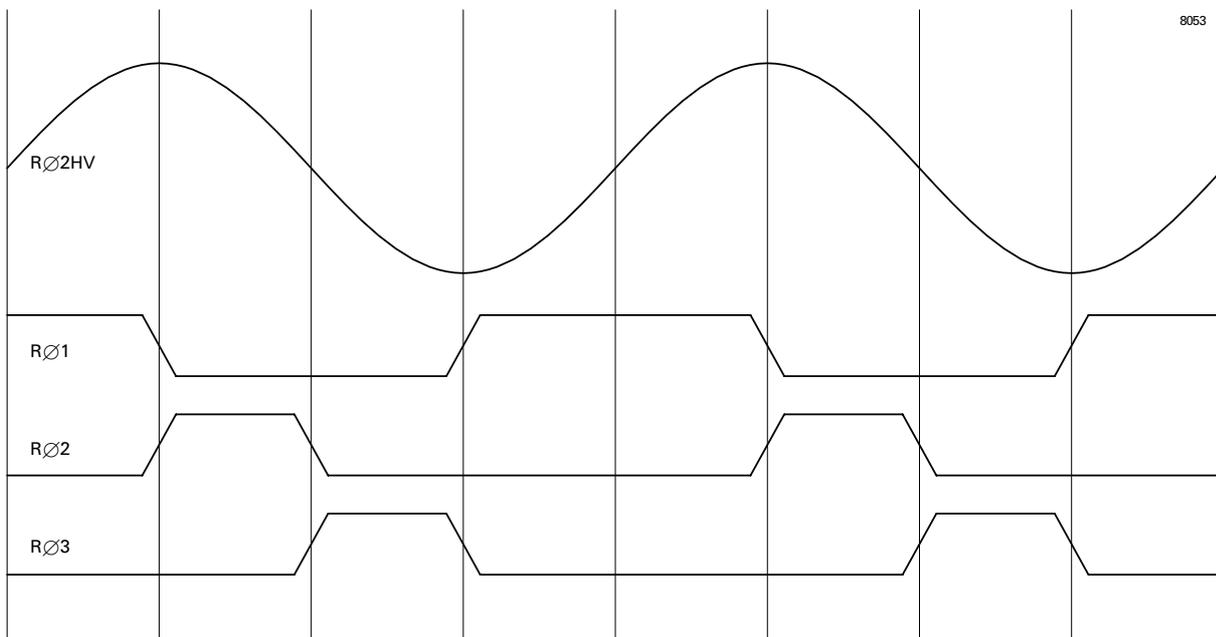

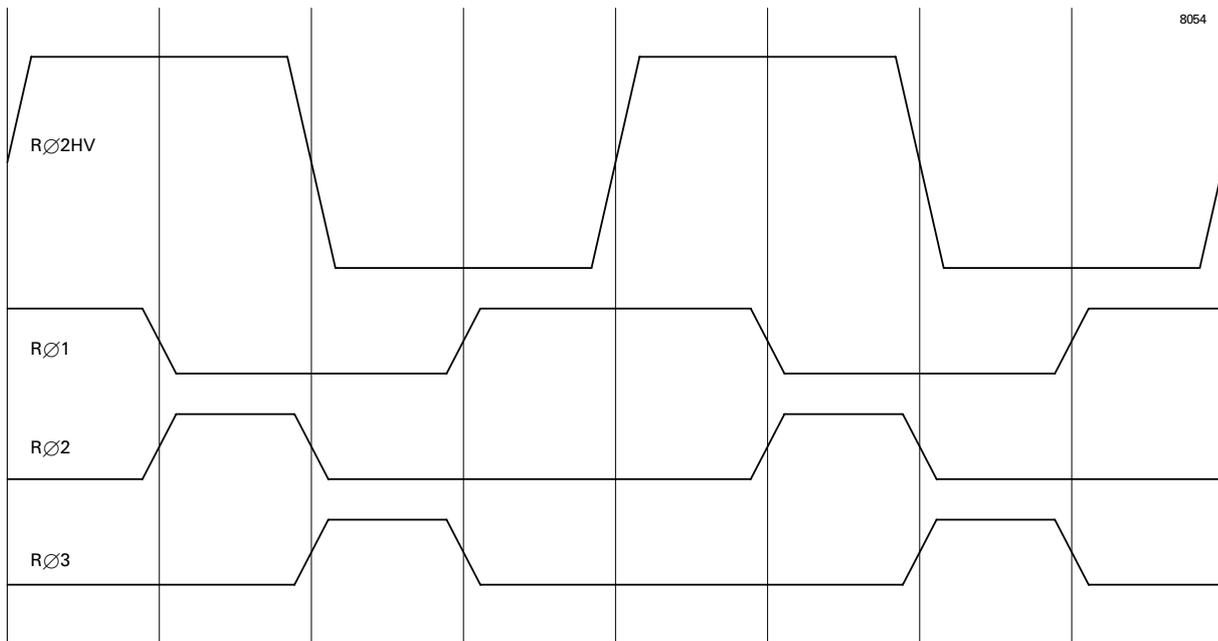**Fig. 1.   Register Clocking Scheme Implementing Sinusoidal R∅2HV Clocking**

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Fig. 2.   Register Clocking Scheme Implementing Square Wave R$\oslash$2HV Clocking

OPERATING VOLTAGE LEVELS

Typical operating voltages are given in the product data sheets. Generally, the applied biases are those used for most conventional e2v technologies CCDs, although the following points should be noted:

● It is necessary to offset the register clock low level to typically 5 V positive of the image and store clock low level when the device is operating in inverted/2-phase mode. This is to avoid generation of excess dark signal.

● Optimum register capacity (and thus maximum dynamic range) is achieved by offsetting the low level of R$\oslash$2HV to typically +4 V relative to the other register clock low levels.

Devices will operate using the stated typical values. However, some adjustment may be required between the stated maximum and minimum in order to optimise performance.

A typical procedure to set optimum operating biases for inverted mode operation is outlined below:

1. Set all voltages to the nominal values given in the product data sheet, with $V_{R\oslash2HV}$ (high) = 20 V (no multiplication gain).

2. Using a suitable lens, image a test chart with a light level corresponding to a detected signal of approximately half the image full well capacity.

3. Make small adjustments to V_{OG} and $V_{R\oslash DC}$ as necessary to optimise charge transfer.

4. Gradually increase the $V_{R\oslash2HV}$ (high) level until the output signal level starts to increase. Continue increasing $V_{R\oslash2HV}$ until a multiplication gain of approximately 10 is achieved. If using sinusoidal R$\oslash$2HV clocking, adjust the phase of the R$\oslash$2HV sine wave as necessary to achieve maximum multiplication gain.

5. Reduce the light level to give a signal of 100 e$^-$/pixel. Increase the multiplication gain until the output signal is roughly 100 ke$^-$/pixel, i.e. a gain of roughly 1000.

6. Put the device in darkness and adjust V_{SS} to find the point where the dark signal just starts to increase rapidly with reduced V_{SS}. This corresponds to the pinning potential of the image and store sections. Set V_{SS} to a value that is approximately 0.5 V above the pinning potential, so that the device is operating in inverted mode with surface dark signal suppressed.

7. Image a suitable test chart and adjust the clock amplitudes $V_{I\oslash}$ and $V_{S\oslash}$ to a value approximately 1 V above the minimum required for correct vertical charge transfer.

8. Make further small adjustments to $V_{R\oslash DC}$ as necessary to optimise horizontal charge transfer.

9. (Anti-Bloomed device only). Set the multiplication gain to unity and image a suitable test chart containing a bright highlight. Adjust V_{ABD} to a value where correct anti-blooming is achieved, between the regimes of image section blooming (vertical spill of charge) and charge avalanching from the anti-blooming drain (resulting in corruption of the image). Confirm correct anti-blooming across the full area of the image.

10. If the device has a GD connection (e.g. the CCD65), turn on the multiplication gain and image a suitable test chart containing a bright highlight. Adjust V_{GD} to its correct value, between the regimes of readout register blooming (horizontal spill of charge) and charge avalanching from V_{GD}.

Other applied biases should not normally require any adjustment for optimisation.

DEVICE OPERATING TEMPERATURE AND DARK SIGNAL REDUCTION

With a sufficiently high multiplication gain applied, the output amplifier noise is effectively eliminated so that the dark signal now becomes the major source of noise. The dark signal is a strong function of temperature, roughly doubling with a 6 °C increase in temperature. Low noise performance, very close to the theoretical limit, can be achieved by sufficient cooling of the device.

FURTHER INFORMATION

For further information and technical support, please contact e2v technologies.