e2v technologies

CCD Sensors Technical Note
Glossary of Terms

Active Thickness:

The thickness of the silicon in which electrons are photo-generated and collected as signal. In back-illuminated devices this is the actual thickness of the device silicon, but in front-illuminated devices it is generally the thickness of a lightly doped 'epitaxial' layer deposited on much thicker material (or substrate) which is highly doped (p+) to cause almost immediate recombination of any charge photo-generated within it.

Advanced Inverted Mode Operation (AIMO) Device:

An improved inverted mode device structure developed by e2v technologies to achieve peak signal levels higher than available with the basic IMO device. See also Inverted Mode Operation device and Multi-Phase Pinned.

Amplifier (On-chip):

A single or multiple transistor structure fabricated with and forming an integral part of the CCD. It is designed to convert the accumulated charge into a voltage signal usable by external circuitry. See also Output Node.

Amplifier Responsivity:

See Output Responsivity.

Anti-blooming Drain:

The drain structure used to remove excess overload-generated charge from the pixels of an image section, usually located in the column isolation region. See also Blooming, Fixed anti-blooming, Gated anti-blooming.

Back-Illuminated (Back-Thinned):

A CCD fabricated on one surface of silicon material which is subsequently processed for illumination from the reverse side, thereby avoiding transmission loss in the electrode layer (particularly significant at short wavelengths or with low energy X-rays). This requires the silicon to be reduced to a thin layer, which is usually achieved with chemical etching, together with surface passivation and an optional anti-reflection coating.

Bias:

The electrical voltage supplies necessary for the operation of a semiconductor device.

Binning:

The addition of signal charge from more than one pixel into a given location. Binning may be performed in either horizontal (row) or vertical (column) directions by performing the summation onto the output node, into a summing well or into the readout register.

Binning Capacity:

The storage capacity of the readout register and/or summing well relative to that of the pixel.

Bloomed:

An optical surface provided with an anti-reflection coating.

Blooming:

When the illumination level is sufficient to generate more charge than can be stored in a pixel, the spread of excess charge to adjacent pixels is known as blooming.

Bulk Silicon (Device):

Silicon of uniform doping concentration throughout the normal total thickness of a front illuminated device.

Channel:

A region of semiconductor defined by implantation for charge transport or conduction. In an image sensor this might be immediately below the surface of the electrode structure, hence 'surface channel', or deeper within the material, 'buried channel'.

Charge Coupled Device (CCD):

A semiconductor in which generated electronic charge is accumulated and transferred by the application of electrical potentials to insulated electrodes or gates. In an imaging CCD the charge is generated by received photons, either optical or X-ray.

Charge Detection:

The charge-to-voltage conversion that takes place in the on-chip amplifier to give an output signal.

Charge Dumping:

The operation of removing unwanted charge from a CCD performed either using a specific dump-gate and drain structure or using gated anti-blooming.

Charge Packet:

An isolated quantity of charge (electrons), typically consisting of the integrated photo-generated charge from a single pixel of the image, which is stored and transported as signal in a CCD.

Charge Sloshing:

An alternative term for dither clocking.

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Charge Transfer Efficiency (CTE):

A measure of the ability of the CCD to transfer correctly a charge packet from the point of generation to the device output. It is defined as the fraction of the charge initially stored in a CCD element which is transferred to an adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states, and may subsequently transfer to the next element (and beyond) with later clock cycles. The value for CTE is not constant but varies with signal size, temperature and clock frequency. Note that in some definitions the value is per electrode-to-electrode transfer, rather than element-to-element.

Charge Transfer Inefficiency (CTI):

Mathematically (1 - CTE).

Clamp-and-Sample:

A practical circuit technique for implementing correlated double sampling.

Clamping:

The action of setting a signal voltage to a pre-determined reference level prior to the subsequent excursion of useful signal as a voltage difference.

Clock Cycle:

The basic increment in the set of clock pulses necessary to transfer charge from one element to the next.

Clock Electrode:

The part of the basic CCD structure, usually fabricated from polysilicon, which, by means of the clock pulses applied to it and its neighbours, effectively controls the storage and movement of signal charge in the silicon beneath it.

Clock Frequency:

The clock cycle repetition rate in Hz, effectively equal to the number of elements a charge packet would pass through per second.

Clock Phase:

A term used to identify: i) the different clock pulses, in the set of similar but time shifted pulses, used to operate a section of a device; ii) the terminal of the device to which these pulses are applied and iii) the electrodes connected to this terminal. A clock phase is usually designated by the Greek symbol ϕ, followed by a number which generally indicates sequence (both in time for the pulses and spatially for the electrodes) and preceded by a letter to indicate the device section to which it applies.

Clock Pick-up:

Attenuated clock pulse waveforms present in the output of the device and therefore superimposed on any signal, but not considered to be noise because of the constant repetitive nature. It is a result of coupling through parasitic capacitance in the CCD or its external connections.

Clock Pulse(s):

The pulsed voltage waveform (of which several are generally required) applied to the device for operation.

Clocking:

A term used to describe operation of the device by applying clock pulses to achieve collection, transfer and detection of signal charge.

Column:

A line of CCD elements in the direction perpendicular to the readout register and generally transferring charge to one particular element in the readout register.

Column Isolation:

The region between two adjacent CCD columns necessary to separate the signal charge in the pixels of each.

Contrast Transfer Function (CTF):

Another term for Modulation Transfer Function (MTF), sometimes used to describe performance with a square-wave input.

Correlated Double Sampling (CDS):

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second taken with charge present.

Dark Reference Pixels:

Pixels of a CCD active area which are made insensitive to illumination (e.g. with an aluminium shield) specifically for the purpose of dark signal compensation. See also Overscanning (virtual pixels).

Dark Signal:

The output signal of an image sensor with zero illumination. This is typically thermally generated electrons within the semiconductor material which are accumulated in each element of the device and transferred to the output during readout.

Dark Signal Non-Uniformity (DSNU):

The spatial variation of the dark signal within an image sensor.

Deep Depletion Device:

A device with the active thickness increased from normal and with a corresponding increase in the depth of depletion (i.e. to minimise the depth of the remaining field-free region).

Defects (Cosmetic):

Pixels of an image sensor which show performance not representative of the average for the device. Defects present with no illumination (white spots or columns) are pixels with greater than a defined limit above the average thermal charge generation, while dark defects (black spots or columns) in an illuminated image are pixels with photo-response less than a defined limit below the local average for the device. Test specifications and data sheets define particular limits or thresholds for the discrimination and counting of defects.

Depletion Region:

The depth of silicon below the surface which is normally devoid of carriers and in which there is an electric field normal to the surface to direct photo-generated charge to the nearest pixel.

Detector Quantum Efficiency (DQE X-rays):

The efficiency of signal charge generation in an X-ray CCD detector (including any scintillator conversion coating) is expressed as the ratio of the square of the signal to noise ratio of the combined detector, to the square of the signal to noise ratio of the X-ray source (see also Quantum Efficiency). This definition takes account of the statistical nature of the X-ray photon generation process, the probability of such photons being absorbed by and generating useful charge in the CCD and the absorption and re-emission from any intervening materials of the detector package.

Dither Clocking:

A method of dark signal reduction where the electrode used for charge storage in an element is periodically switched between the different phases.

Drain:

An n-type region in the device structure to which a positive bias is applied to extract electrons. See also Anti-blooming drain, Dump drain, Reset drain and Output drain.

Dual Slope Integrator:

A practical circuit technique for implementing correlated double sampling.

Dump Gate/Drain:

A device structure, normally alongside the readout register, for the removal of unwanted signal charge. Application to the dump gate of an electrical potential above a threshold enables the fast transfer of charge to a drain.

Element:

The basic unit cell of a CCD able to store an isolated quantity or 'packet' of charge.

Field-free Region:

The depth of active p-type silicon below the depletion region in which electrons (as minority carriers) can diffuse laterally away from the point of photo-generation before being attracted by the depletion region of a pixel and then collected as signal.

Fixed Anti-blooming:

An anti-blooming drain designed to remove any excess charge above a pre-set maximum signal level. See also Gated anti-blooming.

Frame Transfer CCD:

A CCD designed with the active area separately clocked in two sections; one for image acquisition and one for temporary storage and subsequent transfer to a readout register. In some CCDs a shield (see Store shield) is incorporated to make the storage region insensitive to illumination. Frame transfer devices are typically used for TV applications. Integration of a subsequent frame may take place simultaneously with readout.

Frame Transfer Time:

The time period in which a complete CCD image can be clocked from the imaging region to the storage area.

Front Face Illuminated:

The conventional mode of imaging CCD operation where the incident radiation is transmitted to the charge generating silicon via polysilicon clock electrodes. See also Back-illuminated.

Full Frame CCD:

A mode of CCD operation where all active elements are used for imaging.

Full Well Capacity:

An alternative term for storage capacity.

Gate:

A general term for the control electrode in any MOS structure, e.g. transistor, CCD etc.

Gate Protection:

Voltage-limiting components integrated on-chip in the gate connections of the device to reduce its susceptibility to damage from electrostatic discharge (ESD).

Gated Anti-blooming:

An anti-blooming drain designed with a gate electrode to control (via the applied voltage) the maximum signal level at which anti-blooming occurs; it can also be used for charge dumping purposes. See also Fixed anti-blooming and Dump gate/drain.

Guard Ring/Drain:

A drain structure sometimes used in the peripheral regions of a CCD to collect photo-generated charge which would otherwise diffuse into the active regions of the device as spurious signal.

Image Smear (Frame Shift Smear):

The generation of charge in other than the correct pixels during the time that charge signals are being transferred through an illuminated section of the device e.g. for readout. The effect can be minimised by reducing the ratio of transfer to integration times and eliminated by using a shutter to block the illumination during transfer.

Integration:

The accumulation of photo-generated charge within the pixels of a CCD image sensor.

Integration Time:

The time or proportion of the operating cycle of the CCD in which charge is accumulated.

Inverted:

A mode of operation where the electrode voltage is held sufficiently negative of the substrate bias that holes are attracted to the silicon surface, thereby locally inverting the n-type buried channel to p-type and also suppressing the surface component of dark signal.

Inverted Mode Operation (IMO) Device:

A conventional device structure fabricated with additional implants to allow integration with all clock phases at zero and the whole surface inverted, thereby achieving very low levels of dark signal. See also Inverted, Pinned, Multi-Phase Pinned.

Line Readout Section:

An alternative name for the readout register.

Modulation Transfer Function (MTF):

A term traditionally used to define the resolution performance of any optical component. It is the ratio of the depth of output signal modulation to that present in a sinusoidal bar-pattern input of a given spatial frequency. The use of this parameter with pixellated image sensors such as the CCD should be treated with caution as alias effects arising from mismatch between the pixel size/spacing and the intensity distribution of the image may cause some ambiguity in the measurement. Quoted values are usually for the maximum in-phase conditions, where the maxima and minima of the distribution are each coincident with a pixel aperture.

Multi-Phase Pinned (MPP):

Alternative description of IMO devices, used particularly in the USA.

Noise:

The random variations of output signal present effectively superimposed upon the known signals. Such noise arises from the statistical variations of both thermally and photon generated signal and inherently in electron conduction through resistive materials.

Normal Mode (Device):

Conventional device operation i.e. non-IMO.

Notch:

Another term for supplementary channel, particularly in the USA.

Open Electrode Structure:

In the normal operation of a Front Face Illuminated CCD the incident light is transmitted to the silicon via the electrode structure. To minimise the inherent absorption of these layers, particularly at short wavelengths, CCDs may be fabricated with patterned electrodes where a part of each pixel is left unobscured and therefore 'open' to direct illumination.

Output Drain(s):

Drain connection of the amplifier transistor(s).

Output Gate(s):

Final electrode(s) in the readout register, generally held at fixed bias to screen the output node from the pulsed electrodes, and thereby minimise clock pick-up.

Output Node:

The on-chip circuit point whose capacitance to substrate is used to convert the accumulated and transferred charge to a voltage which is subsequently buffered by an amplifier to give an output signal. The node may be formed by the fabrication of a diode structure within the silicon.

Output Register:

An alternative name for the readout register.

Output Responsivity (Charge Conversion Factor):

A measure of the transfer characteristic of the CCD output node and on-chip amplifier of a CCD. This is normally expressed in units of μV per electron of detected charge.

Output Source:

Source connection of the final amplifier transistor, generally used for signal output.

Overscanning (Virtual Pixels):

The action of clocking a readout register by more cycles than the number of register elements. This is sometimes performed to provide blank or zero charge readouts to use for output offset compensation in the electronic processing chain.

Parallel Transfer:

Transfer of the rows of charges towards the readout register.

Peak Signal:

The maximum signal which can be stored, transferred and read out with specified performance. The value quoted may be determined by either saturation or by some parameter reaching a specified limit e.g. non-linearity. Separate values may be quoted for the pixel, the readout register and the output amplifier.

Phosphor (Scintillator):

A chemical compound with the ability to photo-luminesce, when irradiated by optical or X-ray photons. The emitted wavelength is usually visible light and, if appropriately selected, such compounds may be used to effectively wavelength-shift incident radiation to a region of enhanced CCD response.

Photo-Response Non-Uniformity (PRNU):

The spatial variation of the photon-induced signal generating process within an image sensor.

Pinned:

Another term for 'inverted' as the accumulated holes also 'pin' the surface potential to that of the substrate.

Pixel:

'Picture Element': an element in the image section of a CCD in which photo-generated charge is collected as signal.

Potential Well:

A term used to describe the charge storage region (of an element) derived from the shape of the potential distribution in the underlying silicon.

Quantum Efficiency (QE) (Optical):

A measure of the sensitivity of an image sensor to input illumination. It is defined as the proportion of the incident photons which generate signal charge, and is normally expressed as a percentage. It is wavelength dependent. See also Responsivity or Detector Quantum Efficiency (DQE X-rays).

Radiation Hard:

Able to withstand a higher-than-normal dose of ionising radiation within specified limits of performance degradation.

Readout Rate:

The clock frequency of the readout register, divided by the horizontal binning factor if appropriate.

Readout Register:

A CCD analogue shift register fabricated adjacent to the column structure of the device, used for serial readout of each row of charge signals. Also sometimes referred to as the Serial register.

Reset Drain:

Drain connection of the output reset transistor.

Reset Gate:

The gate connection of the output reset transistor.

Reset Pulse:

The clock pulse, usually designated ϕR, applied to the reset gate to reset the potential of the output node prior to the detection of a charge signal.

Responsivity:

An absolute measure of the sensitivity of an image sensor to input illumination. This is normally a function of the wavelength of the incident radiation and is typically expressed in units of mA/W.

Row:

A line of CCD pixels in the direction parallel to the readout register.

Run-in or Run-out Pixels:

Some CCDs are provided with a greater number of register elements than pixels in the imaging row to provide stability of readout clocking and improved integrity of the signal pixels or for system offset compensation (e.g. line by line clamping).

Saturation:

The absolute maximum signal level possible in the device, usually determined by factors such as the onset of clipping, (e.g. with anti-blooming), charge spreading (e.g. in non-anti-bloomed devices), or gross non-uniformity.

Scientific Sensor:

A high performance CCD not generally compatible with standard TV formats and typically operated at reduced temperatures to achieve a wide dynamic range.

Serial Transfer:

Transfer along the readout register to the output.

Spectral Response:

The variation of responsivity with optical wavelength.

Spectroscopic Sensor:

A CCD designed for use in applications where the input illumination is spectrally dispersed in one dimension and imaged or binned in the orthogonal direction.

Storage Capacity:

A measure of the peak signal capability of the device, generally expressed as the number of electrons per pixel.

Store Shield:

An opaque layer (typically aluminium) fabricated on a frame transfer CCD to make the storage region insensitive to illumination. It may also be extended to cover the output amplifier and elements of the image section to give dark reference pixels (e.g. edge columns and/or rows at top and bottom of the image section).

Stitching:

A photo-lithographic technique used to define large area CCDs where a projected mask image of limited area is stepped and repeated.

Substrate:

The underlying p-type body of the semi-conductor material, usually held at fixed applied bias (V_{SS}), also the term used to describe the highly doped base material on which an epitaxial layer is deposited.

Summing Well (Electrode):

A separately connected electrode at the end of the readout register before the output gate which may be used to accumulate several charge packets prior to output and thus facilitate horizontal binning.

Supplementary Channel:

The provision of an additional narrow channel region in the element structure to minimise the number of bulk traps (especially those radiation-induced) experienced by a small sized charge signal on transfer through a device, thereby achieving higher CTE.

Time Delay and Integration (TDI):

A method of CCD operation where the image illumination is scanned across the CCD synchronously with the clocking of the active area electrodes. Each pixel in any column of the CCD therefore acquires a temporally integrated intensity from a point of the image. These may be binned into the register or separately read out as appropriate.

Transition Region/Elements:

One or more columns/rows that form the boundary between the dark reference pixels and the useable imaging pixels. The signal level in these elements is undefined and therefore should not be used.

Trap (Trapping State):

Another name for the generation-recombination centre in a semi-conductor which, in large numbers, is generally the cause of dark signal and charge transfer inefficiency in a device. The term trap is also used to describe a type of image defect resulting from a certain localised imperfection in the channel. This operates by capturing a fixed quantity of charge from a charge packet (or the whole charge packet if less than this quantity) as it is clocked past the defect site, and then slowly releasing the charge to be collected by the following potential wells as they are clocked past the same site.

'Wedge' Dark Signal:

In frame transfer sensors the dark signal component from the store section increases from row to row in direct proportion to the time taken to transfer a row to the readout register, thereby giving a wedge profile to the overall dark signal distribution. Neither the image section component nor that of a full frame sensor will show a wedge profile as an inverse wedge is generated and stored in the array during readout of a previous frame and this normally adds (unless charge dumping is used) to the equal-and-opposite readout wedge to give a uniform dark signal.