

# Charge-Coupled Devices for the ESA PLATO M-class Mission

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## ABSTRACT

PLATO is a candidate mission for an European Space Agency M-class launch opportunity. The project aims to detect exo-planets from their transits across host stars and to characterise those stars by studying their oscillations, hence the name PLATO for, PLANetary Transits and Oscillations of stars. In order to achieve this aim the mission proposes to fly a satellite with a focal plane of up to 34 mini-telescopes, each containing 4 large area back illuminated Charge-Coupled Devices (CCDs) to provide ultra high precision photometry. If successful, the satellite will have nearly 0.9 m<sup>2</sup> of image sensors and will be by far the largest composite detector focal plane ever flown. To meet the mission requirements e2v have developed the CCD270 which has 4510 by 4510 pixels, each pixel is 18 μm by 18 μm, in a development funded by the European Space Agency. This large area (81 mm x 81 mm) full frame image sensor is intended for precision photometry with a dynamic range in excess of 30,000. The CCD270 has been manufactured with a thinner gate dielectric and a higher buried channel dose than standard devices to increase the full well capacity in the image area. The additional advantages of the thinner gate are lower power dissipation, smaller clock voltage swing for standard channel doses and higher tolerance to ionising radiation. This paper describes the imager sensor in detail and focuses on the novel aspects of the device, package and interface.

**Keywords:** Si CCDs, advancements in detector design and fabrication, novel detector designs

## 1. INTRODUCTION

PLATO is a proposed space borne mission which aims to discover planets outside of our solar system by detecting the transits of planets across their parent stars. The prime objectives of the PLATO sensor are: to be capable of detecting down to Earth sized exo-planets orbiting sun-like stars, to measure oscillations of stars with planetary systems, and to measure oscillations of classical pulsators<sup>1</sup>.

In order to achieve these goals the definition and design of the focal plane was a key activity. The outcome of the instrument studies was a concept of an array of individual telescopes each comprising 4 CCDs in a 2 x 2 focal plane. The format of the telescopes and the CCDs was carefully chosen through a trade-off study to best comply with the mission requirements. The trade-off involved taking into account the existing performance parameters and capabilities in detector design and packaging to come up with a unique custom sensor for PLATO. This activity preceded a CCD development activity at e2v and enabled a number of novel features to be incorporated in both the detector and the package.

This paper describes the image sensor in detail, highlighting the novel aspects of the detector, package and interface.

## 2. PLATO CCD270 DESIGN DETAILS

The mission requires a high photometric precision with a minimum resolution. It is these requirements that drove the specification for a pixel size of 18μm square with a Full Well Capacity (FWC) of at least 900ke-, with a target of 1000ke-. This quantity of signal charge can be achieved at e2v without any changes in operating conditions by using a variant of the standard manufacturing process having a thinner dielectric and an increased buried channel dose.

The baseline requirement for the PLATO sensor was to have a full frame device consisting of 4510 x 4510 pixels. The image area was split into top and bottom halves to enable a frame transfer variant to be made for the small number of fast telescopes for satellite pointing. Figure 1 shows a schematic of the CCD270. The bottom half of the image area is

referred to as the store section even though for the majority of devices it would be used for imaging. Along the top of the device a drain and injection gate are included to facilitate a crude control of charge injection should the mission require a means to fill traps generated by radiation damage. Alternatively, the gated drain enables a fast clear of the image area. In this scenario, the top half of the device, the image section, would be reverse clocked to dump charge into the injection drain. The bottom half of device, the store section, would be forward clocked into the register where the signal could be dumped into the adjacent drain when the register dump gate is high. The register dump drain and dump gate are not shown in Figure 1.

The image and store pixels are comprised of four electrodes. This arrangement maximizes charge storage area in the pixel during integration for optimum FWC. The bottom of the store section is separated from the register by a transfer gate which enables the critical transfer into the register to be independently controlled.

The images are read out through 2 ports, one at each end of the split register at the bottom of the device. The register consists of three phase pixels, which is the standard approach for the majority of e2v's devices. The register channel width allows a linear signal handling capability of up to at least 150% of that of the pixel FWC.

Each output port consists of a pair of read out amplifier circuits. The "real" circuit is used to read out the signal from the CCD, and the "dummy" circuit is used to suppress common mode noise. Inputting these channels to an off-chip differential amplifier suppresses correlated noise but increases uncorrelated noise by  $\sqrt{2}$ . Should the dummy amplifiers not be required, they can be powered down through separate Output Drain supplies.

The output circuit of the device was designed to target a Charge to Voltage conversion Factor of  $2.2\mu\text{V}/\text{e}^-$  on a back illuminated device. This allows a  $900\text{ke}^-$  signal to be handled within the linear range of the amplifier performance whilst achieving a noise of  $20\text{ e}^-$  rms at 4MHz.

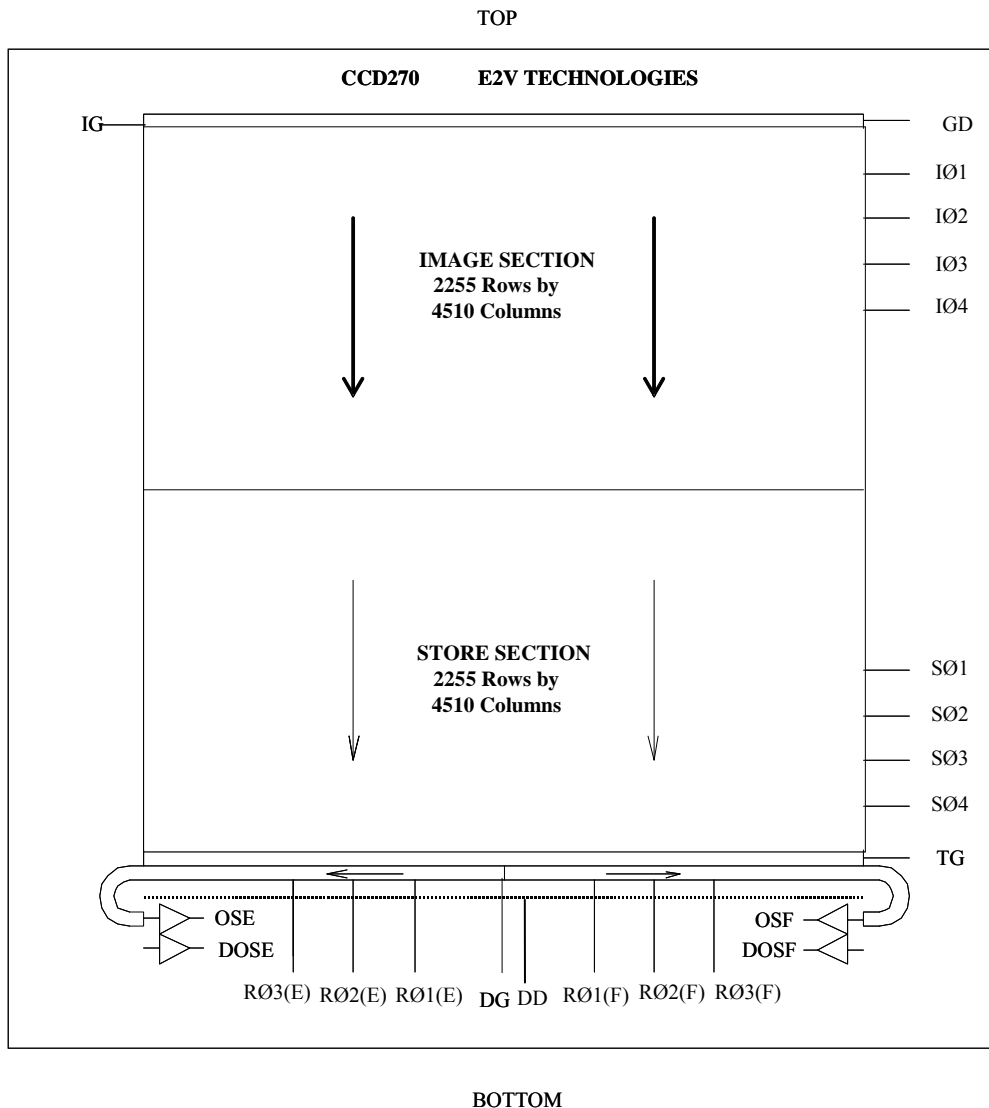


Figure 1 shows a schematic of the CCD270.

The novel aspects of the PLATO CCD design were the use of the thinner gate dielectric in conjunction with an increased buried channel dose and the large area device for a Space application. The thinner gate dielectric and the increased buried channel dose have been demonstrated on previous devices independently. The thinner gate dielectric was used on the CCD203-82s flown on NASA's Solar Dynamics Observatory in 2010 and the higher channel implant has been used on a number of internally run development projects for potential applications. The predicted performance for the PLATO CCD270 was determined from rigorous device modeling, supported by compensated comparisons with existing measurements. This left the large area of the device as the only concern.

e2v have been manufacturing large area devices for a number of years. The CCD230/231 family of devices has been used to make 4k x 4k devices with 15  $\mu\text{m}^2$  pixels and a 6k x 6k variant. More recently e2v has been manufacturing 9k x 9k devices with 10  $\mu\text{m}^2$  pixels for ground based astronomy applications. The 6k x 6k, 9k x 9k and the PLATO CCD270 devices are all full wafer devices that inherently have a low yield; the incidence of fatal defects scale with device size. To quantify the risk and uncertainty associated with the manufacture of a large quantity of devices for the 144 Flight Models and Flight Model spares that are required for PLATO; e2v manufactured more than 6 batches of wafers during the PLATO CCD development contract funded by the European Space Agency. From this data and our experience on the

Gaia programme, where e2v delivered 44 Engineering Models, and 130 Flight Models and spares, a realistic prediction of the manufacturing plan could be made for the delivery of Flight Models.

### 3. PLATO PACKAGE DESIGN

The PLATO CCD had to be assembled on to a package that would fulfill the thermal and mechanical interface requirements of the focal plane cameras. Each focal plane camera consists of a 2 x 2 array of devices maintained at an operating temperature of  $-70^{\circ}\text{C}$  to suppress dark signal. Each device is cooled by a thermal strap on the back of the package, which was design to be close butted on two sides. The flexible cable between the CCD and the warm Front End Electronics provided a thermal break and the electrical interface. Figure 2 shows the interfaces for the Focal Plane Array and Front End Electronics.

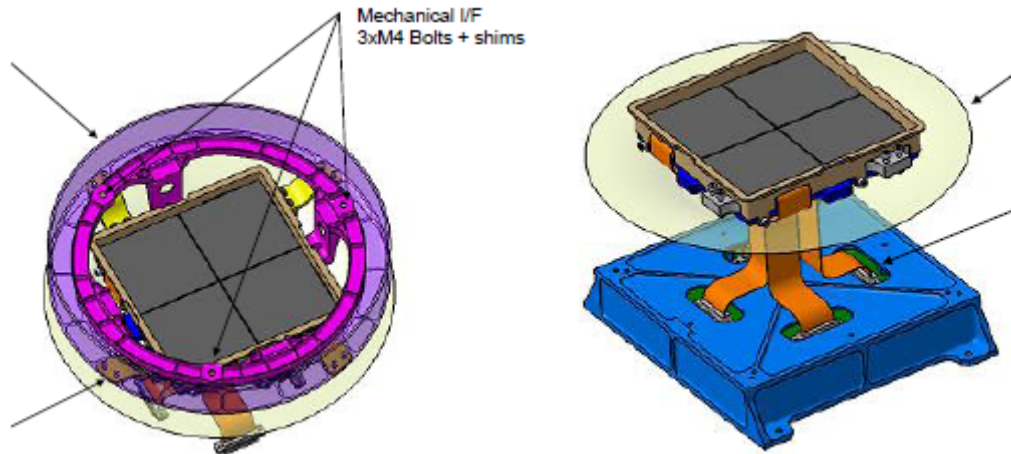


Figure 2 shows the interfaces for the Focal Plane Array and Front End Electronics from the Assessment Phase PLATO Payload Consortium Study<sup>2</sup>. This design has since been heavily revised, but it illustrates the camera focal plane and electronics clearly.

The PLATO CCD package is manufactured from Silicon Carbide (SiC) and provides positions for mounting the flexi connector, and various undercut holes to fit threaded inserts that provide the different mechanical interfaces. Silicon carbide is a desirable material for CCD packages as it has a close thermal expansion match to silicon and a high thermal conductivity.

Figure 3 shows top surface (sky facing) and bottom surface (FEE facing) views of the whole device assembly. The assembly consists of the die, a flexible cable with a micro-D connector, two flexi clamps, a Platinum Resistance Thermistor (PRT), threaded inserts for handling rods, threaded inserts for fixing the camera thermal strap, flexi clamp fixing screws and three studs with shims attached to inserts in the package.

The studs and shims provide the mechanical interface to the camera. The shims are clamped to undercut holes in the SiC package by the stud, and are the thermal interface for cooling the package. The studs enable the packages to be secured to the camera structure, and the combination of the studs and shims enable e2v to specify a precise package height tolerance and image area flatness.

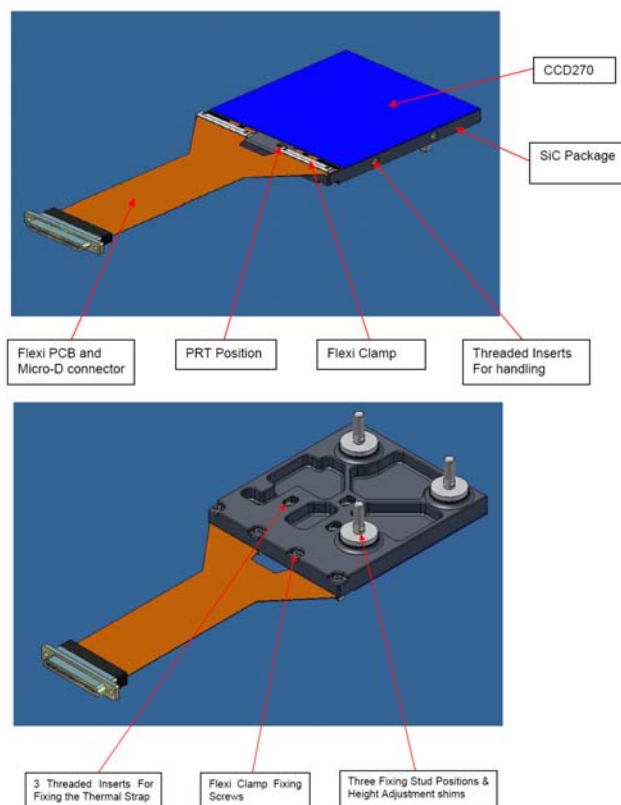


Figure 3 shows top surface (sky facing) and bottom surface (FEE facing) views of the whole device assembly.

In order to accommodate the instrument mechanical and thermal design, the position of the third stud on the underside of the package had to be shifted away from the center line of the package. In moving this stud it increased the distance over which the package edge could act as a cantilever. To retire the risk, e2v carried out simulations of the shock loads on the package for 1500g 0.5ms and 500g 1.0ms conditions.

The initial simulation for a 1500g shock perpendicular to the plane of the CCD determined that the stress in the package around the threaded inserts in the undercut holes in the SiC exceeded the material yield point. The material yield point in the Invar studs was also exceeded.

The simulation was repeated for a reduced shock specification, MIL-STD-883, Method 2002.5, Condition A (500g, 1ms), in the vertical direction. In this case, the outcome was positive, although the yield safety factor for the Invar studs was only 10% in the positive vertical direction.

Further simulations of the shock in the plane of the CCD indicated that the package should survive the Condition A levels. The uncertainty arises from the estimation of the friction between the studs and the shims within the model. Practical tests will be required in the future to address this issue.

#### 4. PLATO FLEXI DESIGN

Flexi circuits provide minimum footprint size and an acceptably low heat transfer path away from the cryogenically cooled package. They are light in weight, are compatible with low temperatures and exhibit low out-gassing characteristics. They have been proven to be suitable for space applications and have been qualified previously as part of the CCD91-72 device for Gaia.

The design of a flexi is a trade-off between optimising the length, layout and tracks for electrical or thermal requirements. A short flexi with a ground plane will favour the electrical performance; whilst a longer flexi with minimal copper tracks will favour the thermal requirements and establishing a break between the cold detector and the warm electronics.

The challenge for the PLATO CCD was optimising the trade-off for the 4MHz output signal (OS) frequency whilst maintaining a thermal difference of 90°C, 120°C maximum, between the detectors and the electronics. In order to minimise the electrical cross-talk the output signals and biases were grouped towards the ends of the connector, with the clocks at the centre. The substrate connections were situated between the groups in order to screen the “quiet” signals from cross-talk due to the fast clock edges. Otherwise, the order of the CCD pads was transferred to the micro-D pins directly one-to-one in order to minimise cross-over of tracks in the flexi.

The OS and dummy OS pairs were assigned to adjacent pins to optimise common-mode noise rejection when used as a differential output. The two temperature sensor pads were also tracked to adjacent pins, so that any pickup on one wire should also be present on the other, and therefore not affect the resistance measurement. Where possible, connections to the two halves of the device were positioned symmetrically to avoid any delays / imbalances between the two outputs.

The thermal conductance of the flexi was calculated from the layout of the tracks and a knowledge of the material properties. The total conductance calculated was 1.28mW.K<sup>-1</sup>. For a maximum temperature difference during operation of 120K (+40°C / -80°C) between the SiC package and the FEE interface, this equated to a 154mW rate of heat transfer through the flexi. This is roughly equivalent to the power dissipated by the register clocks averaged over a frame period, yielding a local rise in temperature of ~0.1K. Thermal conduction through the flexi cable was therefore not expected to have a significant effect on the operating temperature of the CCD.

## 5. KEY SPECIFICATIONS OF THE PLATO CCD

The following table outlines the key performance parameters of the PLATO CCD at the specified characterization temperature.

Table 1 outlines the key performance parameters of the PLATO CCD.

| Parameter                              | Specification | Target |
|--|---------------|--------|
| CCD characterisation temperature, °C   | -70 ± 3°C     | -      |
| Pixel Size, µm x µm                    | 18.0          | -      |
| Number of Pixels, Full Frame           | 4510 x 4510   | -      |
| Number of Pixels, Frame Transfer       | 4510 x 2255   | -      |
| Image Area Peak-to-Valley Flatness, µm | 40            | -      |
| Package Height Tolerance, µm           | ± 15          | -      |
| Quantum Efficiency, %                  |               |        |
| 500 nm                                 | 87            | -      |
| 600 nm                                 | 91            | -      |
| 700 nm                                 | 83            | -      |
| 800 nm                                 | 62            | -      |
| 900 nm                                 | 31            | -      |
| 950 nm                                 | 15            | -      |
| Full Well Capacity, ke-                | 900           | 1000   |
| Dark Signal, e-/pixel/s                | 0.8           | 0.4    |
| Dark Signal Non-Uniformity, e-/pixel/s | 0.08          | -      |
| Photo Response Non-Uniformity, %       |               |        |
| < 700 nm                               | 3.0           | -      |

|   |      |       |
|---|------|-------|
| > 700 nm  | 5.0  | -     |
| Noise at 4Mpixels/s, e- rms                             | 28.0 | 20.0  |
| Output Amplifier Responsivity, $\mu\text{V}/\text{e}^-$ | 2.0  | > 2.0 |
| Linearity, %  | 4.0  | 3.0   |
| Power Dissipation, mW                                   |      |       |
| Static - total value per amplifier                      | 200  | 180   |
| Dynamic – total clock and static power per frame        | 1400 | 1300  |
| Mass, g   | -    | 220   |

The amplifier responsivity was specified as  $2.0 \mu\text{V}/\text{e}^-$  with the note that higher responsivity would be desirable provided that the linearity specification could be achieved. The designed value was  $2.2 \mu\text{V}/\text{e}^-$  which met the minimum image FWC specification, the linearity specification, and targeted the lowest possible noise.

The calculated average dynamic power dissipation for a full frame CCD270 operated with PLATO specific line transfer, read out and frame rates is approximately 270mW where roughly 120mW will be dissipated on the device. The value for a frame transfer version of the CCD270 is approximately 570mW where 240mW will be dissipated on the device.

## 6. CONCLUSIONS

This paper has described the PLATO CCD270 device design details, including the novel features required to achieve a high charge handling capacity in the image area pixels. The package assembly has been introduced and the main challenges associated with accommodating the camera focal plane interface have been highlighted including the impact on the package shock test survivability. The trade-offs associated with the design of flexible ribbon cables for detectors run at low temperatures have been introduced and some of the features of the design have been explained. Finally, an outline of the key device performance specifications has been summarised.

## REFERENCES

- [1] PLATO Science Requirements Document ESA and PLATO Science Study Teams, SCI-PA/2008-020/PLATO/SciRD, 28<sup>th</sup> May 2010, Issue 4.
- [2] Assessment Phase PPLC Design Report, CNRS Laboratoire d'Astrophysique de Marseille, PLATO.LAM.INS.REP.1044, Issue 1, Rev. 1, 2<sup>nd</sup> July 2009.