First Measurements of True Charge Transfer TDI (Time Delay Integration) Using a Standard CMOS Technology

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***Abstract*— This work focus on an innovative noiseless charge transfer TDI pixel fabricated with a one poly standard Imaging CMOS technology. Parallel column charge to voltage conversion decreases drastically the number of needed charge transfers while keeping high motion/dynamic MTF (multi phase approach), high QE (photodiode based architecture) and low noise (no noise summation).**

Keywords: TDI (time delay integration), charge transfer, CMOS, photodiode, motion MTF.

I. INTRODUCTION

In the past years, the improved CMOS image sensors have started to take over from CCD technology. However, TDI applications are still a challenge for CMOS APS due to its intrinsic operating mode: charges are directly converted into voltage at the output of each pixel. In order to overcome this limitation, the standard approach consists of moving to digital summation: voltages are converted into digital words which are summed up as the scene is moving through the TDI array. However, the main drawbacks are the summation noise and the ADC performances (high operation speed is required). A first attempt to emulate CCD operation with CMOS technology has been done by [1]. However the Quantum Efficiency (QE) in the blue is poor due to the use of a large polysilicon gate area. This paper presents the first measurements of an innovative TDI CMOS pixel allowing true noisefree charge transfer and high QE based on a standard CMOS technology.

In the first part, we are going to describe and explain the push broom operation of the TDI pixel thanks to TCAD simulations. The second part focuses on the test chip and the pixel array which are manufactured using a standard Imaging CMOS technology. The last part of the paper is dedicated to electro-optical measurements and analysis. Future work and pixel optimization is also discussed.

II. CHARGE TRANSFER OPERATION

To overcome the technological limitation and allow a true noiseless charge transfer, we propose a new pixel architecture which is described in Figure 1 (in the case of a 2 phase architecture but the principle can be extended to 3 or 4 phases). Each phase of the pixel is composed of a pinned photodiode used for carrier storage, a pinching gate and a transfer gate. The purpose of the pinching gate is to exhibit a higher threshold voltage compared to the transfer gate leading to a potential step, as illustrated in the TCAD simulation in Figure 2 showing the maximum potential across the device (the cutplane runs through the middle of the structure). This effect is achieved by the P implantation located on both sides of the pinching gate. This implant also prevent the carriers moving directly from the photodiode to the transfer gate: thus electrons have to pass through the pinching gate. Thanks to the potential steps, the transfer is directional leading to a true charge transfer operation.

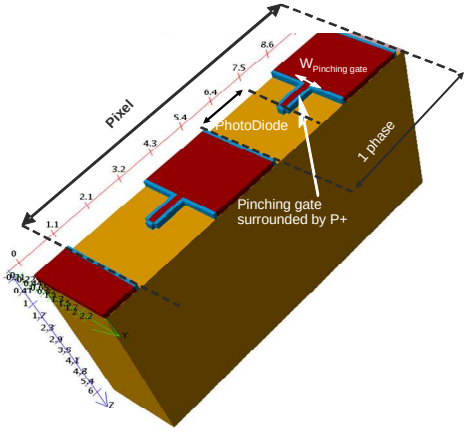

Figure 1. Innovative pixel architecture for charge transfer (shown here for 2 phases per pixel).

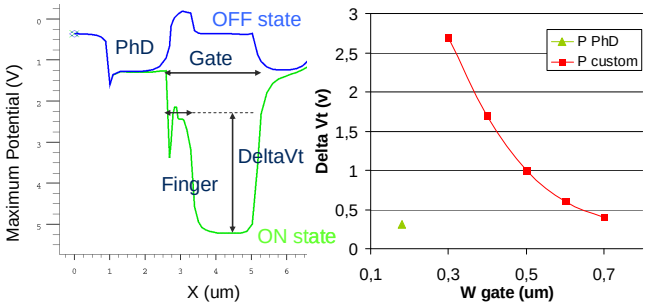

Figure 2. (Left) Maximum Potential simulated thanks to 3D TCAD along the pixel (extracted from a cutplane through the middle of the device). (right) Delta Vt as a fucntion of the pinching gate width.

The full well capacity (Qsat) is defined by the geometry of the phase and is limited either by the storage under the gate or in the photodiode. The storage of the photodiode is mainly defined by the pinned voltage. On the other hand, the storage under the gate is limited by the DeltaVt defined in Figure 2. This value strongly depends on the pinching implantation and the width of the pinching gate. Figure 2 shows the pinching effect as a function of the width of the polysilicon finger for two pinching implantations: the P used for the photodiode (P PhD) and a custom implantation (P custom). In the first case, the advantage is to have a fully auto-aligned implantation, but as it is very shallow the pinching effect is too small. With the second case, the pinching ranges from 0.5 to 3V and is appropriate for a correct device operation.

The device can operate with 2 timings (see Figure 3). For timing A, the phases are overlapping and the carriers are stored under the gates. The advantage is a large full well capacity (surface storage) but at the cost of a low transfer inefficiency. Now considering timing B, the gates are pulsed only for transfer and the carriers are stored in the photodiode. The full well capacity is reduced but as the carriers are stored in volume, the transfer inefficiency is improved. The later timing (B) will be used in this work.

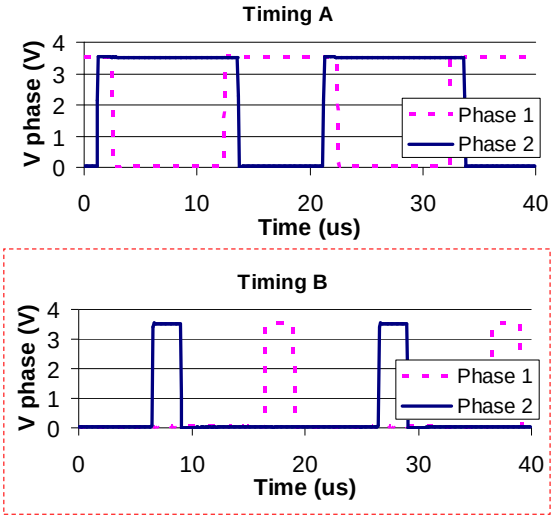

Figure 3. Measurement at the oscilloscope of the 2 phases for 2 timings.

The operation principle considering a structure with 2 phases using timing B is described in Figure 4. For the sake of simplicity, we consider here that the moving object is composed of strips of dark and white generating respectively “filled black electrons” and “empty white electrons”. In the first part of the timing, the electrons are accumulated in the photodiode and then the all gates named “phase 2” are switched ON. The carriers located on both sides of the gates drift under the gate. When the gate is turned OFF, all the carriers are directed to the photodiode located on the right thanks to the pinching effect described earlier. Then the second part of the integration is performed and all the gates named “phase 1” are switched ON, repeating the same operation than before. This way charges are moved forwards along the TDI structures.

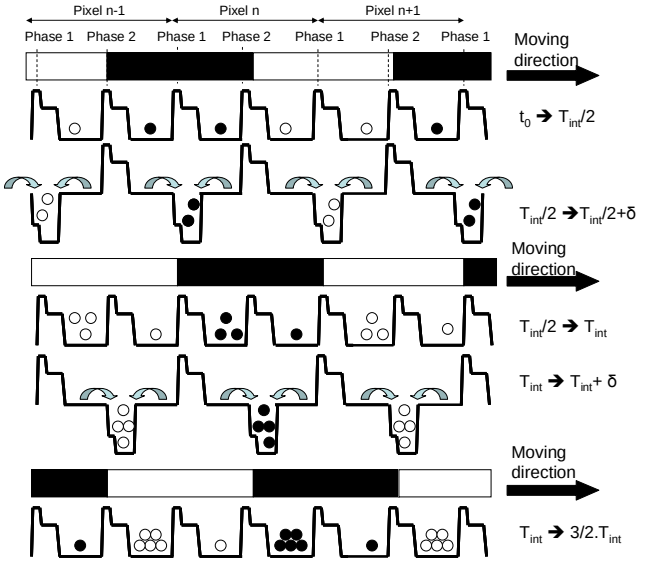

Figure 4. Operation principle of the structure with 2 phase per pixel and using timing B.

III. TEST CHIP DEFINITION

The silicon test chip has been manufactured using a standard Imaging CMOS technology. Due to a mistake, 1.5ohm.cm bulk wafers were used instead of epitaxial wafers. This kind of wafers is known to have many defects affecting both the dark current and the charge transfer efficiency.

The aim of this demonstrator is to characterize the pixel operation only, thus the circuit is fully analogue (no ADC onboard). The circuit architecture is given on Figure 5.

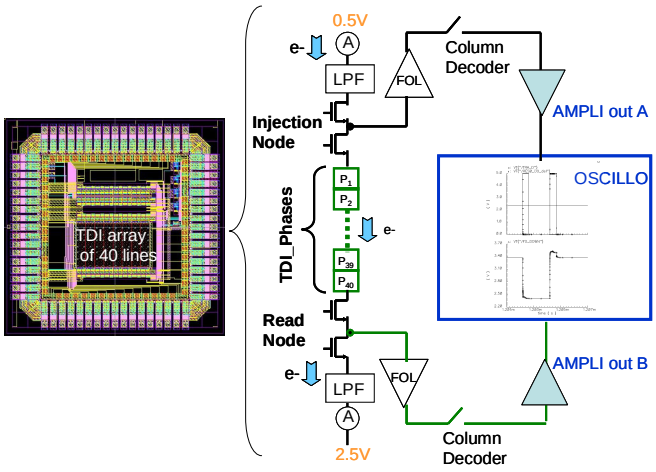

Figure 5. (Left) Circuit architecture. (Right) Circuit diagram: LPF stands for Low Pass Filter and FOL for follower architecture.

The pixel array is composed of 40 lines and 64 columns. Charge injection can be performed either optically by illumination or electrically though the injection stage. Currents are monitored though picoammeters located off chip whereas

the potential of the input and output node can be displayed on an oscilloscope through an amplifier.

In the following, we will present a CMOS TDI pixel with two pixel pitches: 7um and 13um with 2 phases per pixel. Each phase has 3 pinching gate for the 7um and 4 for the 13um structure and each pinching gate width is 0.3um. This multiple phases approach allows high motion/dynamic modulation transfer function (MTF) values especially compared to digital summation TDI CMOS solutions. At the bottom of each column, a charge to voltage conversion is performed using a differential pair and then directly read out. A typical measurement of the output signal is given on Figure 6 for an electrical injection corresponding of 10 lines. The signal is similar to a classical CCD signal with RST level followed by the reset gate coupling when it is switched off and finally the signal level.

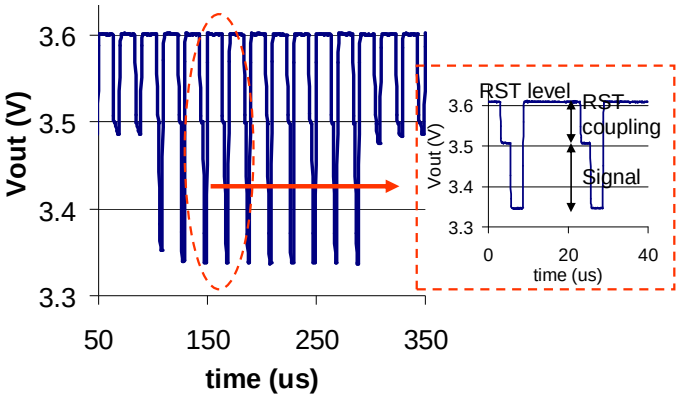

Figure 6. Measurement of the output signal after an electrical injection corresponding to 10 lines.

Analogue to digital converter (ADC) operating at line rate speed will be implemented in a later stage. This approach allows bypassing the greatest limitation of numerical based solutions which are limited by the speed of the ADCs and their area. Such an approach combines advantage of charges transfer TDI (CCD) and CMOS integration.

IV. ELECTRO-OPTICAL MEASUREMENTS

A. *CVF*

The charge-to-voltage conversion factor (CVF) is obtained by measuring the mean current and the output voltage from the TDI: 12.5 uV/e- and 7.5 uV/e- respectively for the 7um and the 13um pixels. These values can be tuned independently from other parameters.

B. *Dark Current*

The dark current is measured by increasing the integration time and plotting the output voltage as a function of time (see Figure 7). The ON time of the gates is kept constant (2.5us). The slope of this curve grants access to the dark current expressed in ke-/s/pixel. For the 7 and the 13um structure, 40ke-/s and 70ke-/s respectively are measured.

The dark current should not be expressed in nA/cm2 as it originates from the gates and the photodiodes, unlike CCD where only the gates generate carriers. However, for the purpose of comparison a standard CCD exhibits a current around 1nA/cm^2 which gives ~10ke-/s/pixel for a 13um pixel and ~3ke-/s/pixel for a 7um pixel.

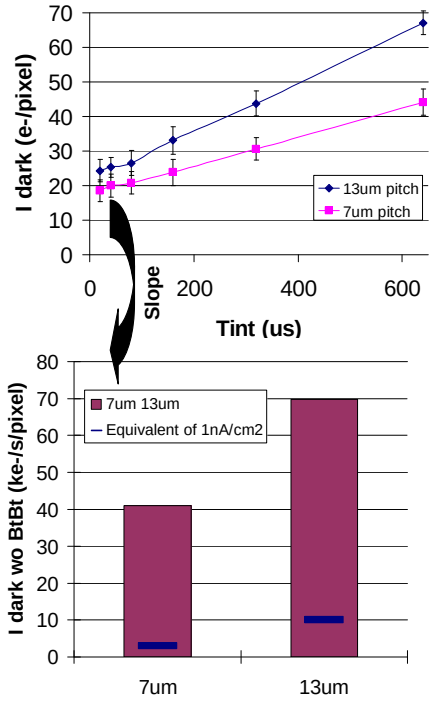

Figure 7. (Up) Measurement of the dark signal as a function of time for the 7 and 13um. (Down) Extraction of the dark current for each case without the BtBt offset.

It should be mentioned that the dark current in Figure 7 does not reach 0 when the integration time tends to 0s, indicating a dark current source independent of the integration time.

Due to the strong P+ pinching implantation located near the gate, the current could originate from Band to Band Tunneling (BtBt). In order to verify this assumption, the dark current is measured as a function of the ON time of the transfer gates (Tr): see Figure 8. This time a straight line passing through (0;0) is obtained. Furthermore, the current is measured with respect to the gate voltage (Vphase) for the 7 and 13um device and normalized by the gate width. The curves behave exponentially and both curves merge indicating that this current scales with the length of P+ in contact with the gates. Both results are in accordance with the BtBt hypothesis.

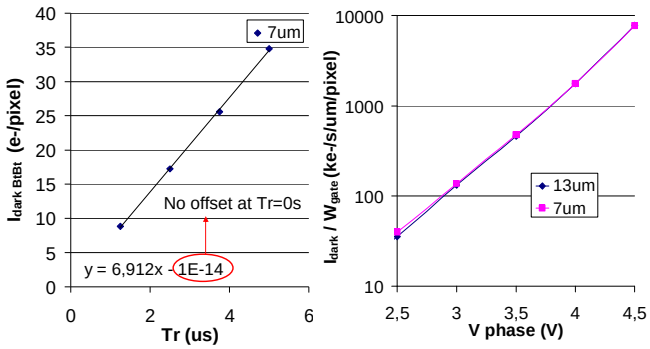

Figure 8. (Left) Measurement of the dark current offset as a function of the ON time of the transfer gates (Tr) for the 7um device. (Right) The dark current offset is measured as a function of the phase bias normalized with repect to the gate width for 7um and 13um (Tint=14us).

To further validate the BtBt origin and to find a way to mitigate the effect, TCAD simulations based on process data were carried out. The simulated structure is shown on Figure 9: it represents a cutplane perpendicular to the carrier direction through the pinching finger.

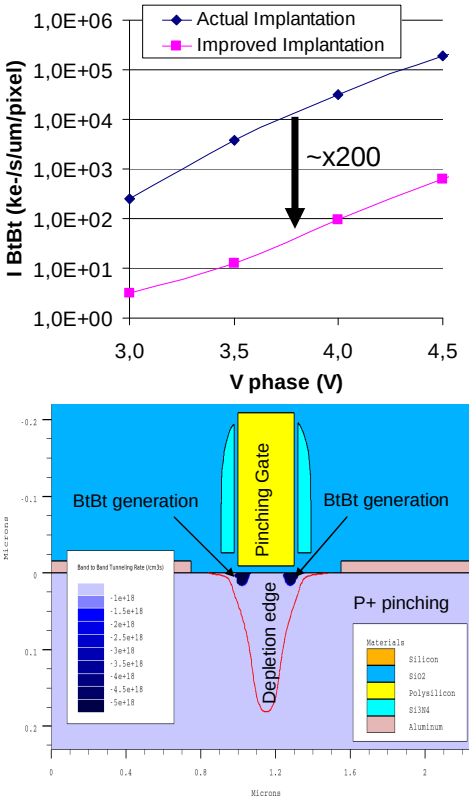

Figure 9. (Left) TCAD simulation of the BtBt dark current offset due to the P+ pinching implantation (Tr=2.5us, 7um structure). (Right) Output structure for V_{phase}=5V showing the localisation of the BtBt generation.

The simulations shows that the BtBt is located at the gate edges as supposed and that the simulated levels of current are compatible with the measurements (the observed discrepancy ~x10 can be explained by the difficulty to model correctly this phenomenon). By decreasing the dose and increasing the energy, the BtBt current can be divided by ~200. Looking at the pinching effect, the finger has to be decreased in order to keep the same pinching effect with the optimized implantation, as can be seen on Figure 10 showing the maximum potential under the pinching gate from a cross section taken perpendicularly to the carrier transfer direction.

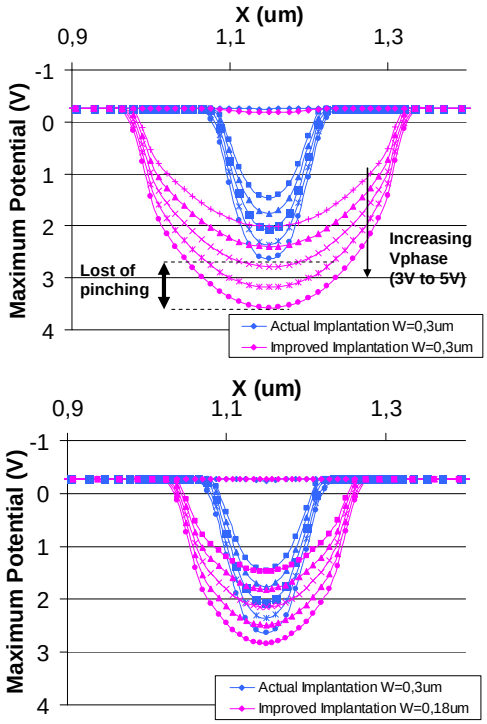

Figure 10. TCAD simulation of the maximum potential under the finger from a cross section perpendacularly to the carrier trnsfer direction for the actual pinching implantation and the optimized one and for Vphases ranging from 3V to 5V by 0.5V steps. (Up) Wfinger=0.3um for both cases. (Down) Wfinger=0.3um for the actual implant and W=0.18um for the optimized one.

To conclude this section, the "expected" dark current due to the volume generation and diffusion in the photodiode and the surface generation under the gates have been measured. This value can be optimized by increasing the ratio between the photodiode surface and the gate surface. Pinning the gates during the OFF state like in CCD can also be a way of improvement (but a negative voltage is required). A further decrease can be achieved using standard epitaxial wafers.

The dark current offset has been identified as BtBt, but TCAD simulations show how to mitigate this effect by changing the pinching implantation. But due to this high dark current, the biasing of the phases has been kept at 3.5V for the rest of the measurements.

C. Charge Transfer Efficiency (CTE) and Full Well Capacity (Qsat)

The most important point for charge transfer TDI is the charge transfer efficiency (CTE): it defines the percentage of

carriers contributing to the image. Its counterpart is the Charge Transfer Inefficiency (CTI): it defines the percentages of carriers left behind (thus that are not transferred). Both can be defined as:

$$CTE = (1-\varepsilon)^{Nb_{stages}} \quad \& \quad CTI = 1-CTE \qquad (1)\ \&\ (2)$$

Where ε is the CTI per pixel and Nb_{stages} is the number of TDI lines. Leaving carriers behind also leads to a degradation of the Modulation Transfer Function (MTF). The contribution of the transfer inefficiency to the global MTF can be calculated as [2]:

$$MTF_{transferInefficiency}(f_{Nyquist}) = \frac{1-\exp(-2.\varepsilon.Nb_{stages})}{2.\varepsilon.Nb_{stages}} \qquad (3)$$

The dependences of the MTF contribution and the CTE are plotted on Figure 11 as a function of the number of TDI stages and for various ε values.

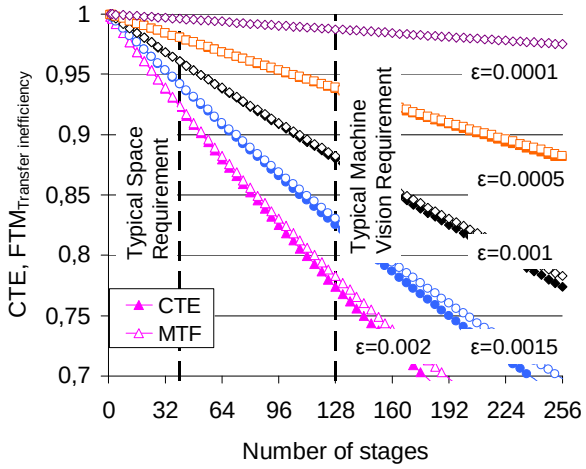

Figure 11. Calculation of the total CTE and the FTM at Nyquist due to the transfer inefficiency as a fuction of the number of TDI stages and the CTI. Open marks stand for the MTF and the filled marks stands for the CTE.

The CTE/CTI of our structures has been measured in dark conditions by electrically injecting charges in the TDI equivalent of 40 lines with a signal level of V_{signal} and then looking at the residual signal V_{empty} of the next "empty" lines (without injections). The ε (CTI per pixel) is then calculated for various signal levels by:

$$\varepsilon = \frac{\sum V_{empty}^{residual}}{Nb_{stages}.V_{signal}} \qquad (4)$$

The CTE measurements are shown in Figure 12 as a function of the number of carriers injected (Q0) for the 13um and the 7um device. The CTE values of both structures are equivalent for injection levels above 30% of Qsat to a CCD with 10000 column and register output with $\varepsilon \sim 5.5.10^{-6}$. At low level, the CTE is strongly degraded. However if comparison is done at fixed number of carriers (for example at ~3000e-), the CTE of the 7um is much better compared to the 13um benefitting from the reduced gate area (leading to a smaller amount of trapped carriers). Thus by correct tuning of the device parameters it is possible to transfer a small number of carriers.

Three parameters are involved in the CTE degradation: the gate area, the pinching gate width and the number of pinching fingers. The main parameter is the photodiode to gate area ratio: increasing it will increase the CTE while improving the Qsat and the QE. Decreasing the finger width is compatible as seen before with the new pinching implantation. Then the number of pinching fingers should be optimized in order to keep a good transfer while increasing the CTE.

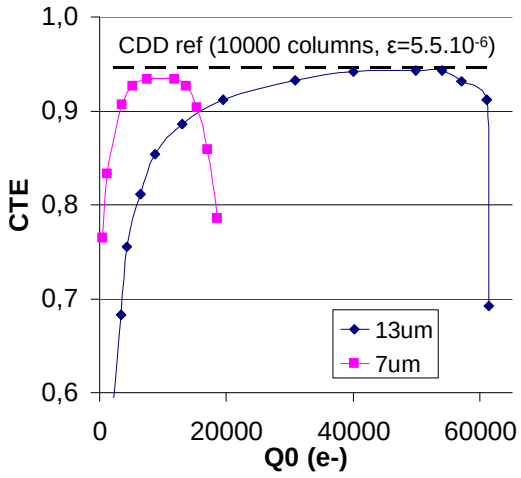

Figure 12. Measurement of the CTE of our TDI array (40 lines with column readout) as a function of the number of injected charges (Q0) for the 13um and 7um structure. A equivalent CCD performance with register readout is also added.

The full well capacity (Q_{sat}) can be defined as the value of carriers at which the CTE starts to decrease and can then be extracted from the measurement of Figure 11: Qsat(7um/13um) =16/52ke-. The Qsat depends on the photodiode area and the number of phases per pixel. It should be noted that due to the potential shape of the pixel (see Figure 2); it is possible that some of the carriers may be stored under the gate at high signal level.

D. Optical Measurement: QE and MTF

One of the benefits of this structure over classical front side illuminated CCD is the high Quantum Efficiency (QE) coming from the use of a photodiode. The measurement is shown on Figure 13: the QE peaks higher than 50% over the visible range without micro lenses. Calculations are in good agreement with the measurements. The lost in the 400-500nm range is due to the absorption in the polysilicon gates. Increasing the photodiode to gate area ratio drastically increases the QE in this range.

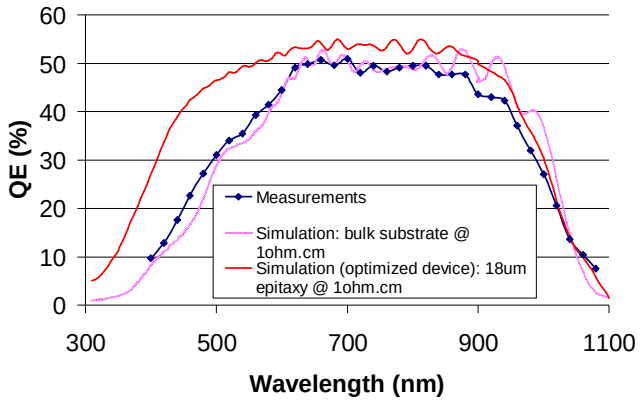

Figure 13. Measurement of the QE of the 13um device as a function of the wavelength. Simulations are also plotted especially with an optimized photodiode to gate surface ratio.

The static Modulation Transfer Function (MTF) has been measured along and across the track at Nyquist frequency for the 13um device: see Table 1.

TABLE I. MTF MEASUREMENT AND SIMULATIONS

Static MTF	**500nm**	**650nm**	**870nm**
Simulation across the track, standard epi, Fill Factor=0.9	*69*	*60*	*42*
Simulation across the track, bulk equivalent, Fill Factor=0.9	*69*	*54*	*25*
Measurement across the track	65	51	22
Measurement along the track	53	43	21

The measured values across the track are similar to the ones simulated with a bulk equivalent. The low QE figures at 870nm are due to the high thickness: when moving to a standard thickness, the MTF doubles. The MTF along the track is 10 points lower at 500nm and 650nm than across the track but becomes equal at high wavelength (870nm). Across the track, the isolation is done by STI encapsulated by Pwell whereas along the track, it is done only by the gates. Thus the isolation is worse along than across. However at large wavelength as the carriers are generated deeper, the difference becomes minor leading to a similar MTF.

V. CONCLUSION

TDI structures of 7um and 13um operating with a true charge transfer have been designed and manufactured on a standard Imaging CMOS technology. The main electro-optical performances have been measured and analyzed thanks to TCAD simulations. Compared to classical CCD, the advantages of this structure are a high QE (use of photodiodes) and a high speed (since parallel processing of voltages issued from each column is enabled by CMOS technology, conversion is done at TDI line rate). High values of CVF are achievable and help decreasing the noise. Compared to the digital summation based TDI solution, the advantages are a lower noise (charge transfer is noiseless), a higher motion MTF (multiple phases per pixel) and a reduced area/complexity.

The main drawback of this structure (high dark current) has been analyzed and ways of mitigation have been outlined thanks to TCAD simulations. The CTE has been measured and improvements have been identified.

The presented TDI CMOS structure shows high sensitivity allowing to image very faith signal levels. High performance and high speed applications together with light weight/compact imaging systems suit very much the presented TDI CMOS.

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