e2v technologies

Recent results from CMOS Back-thinning

Name Paul Jerram

Date 28th January 2010

Talk outline

- Brief introduction to back-thinning
- Performance of back-thinned devices
- Thinning of a 0.5MPixel commercial CMOS sensor
- Thinning of 2MPixel sensor designed for space applications
- Future plans

© e2v technologies (uk) limited

Introduction to back-thinning

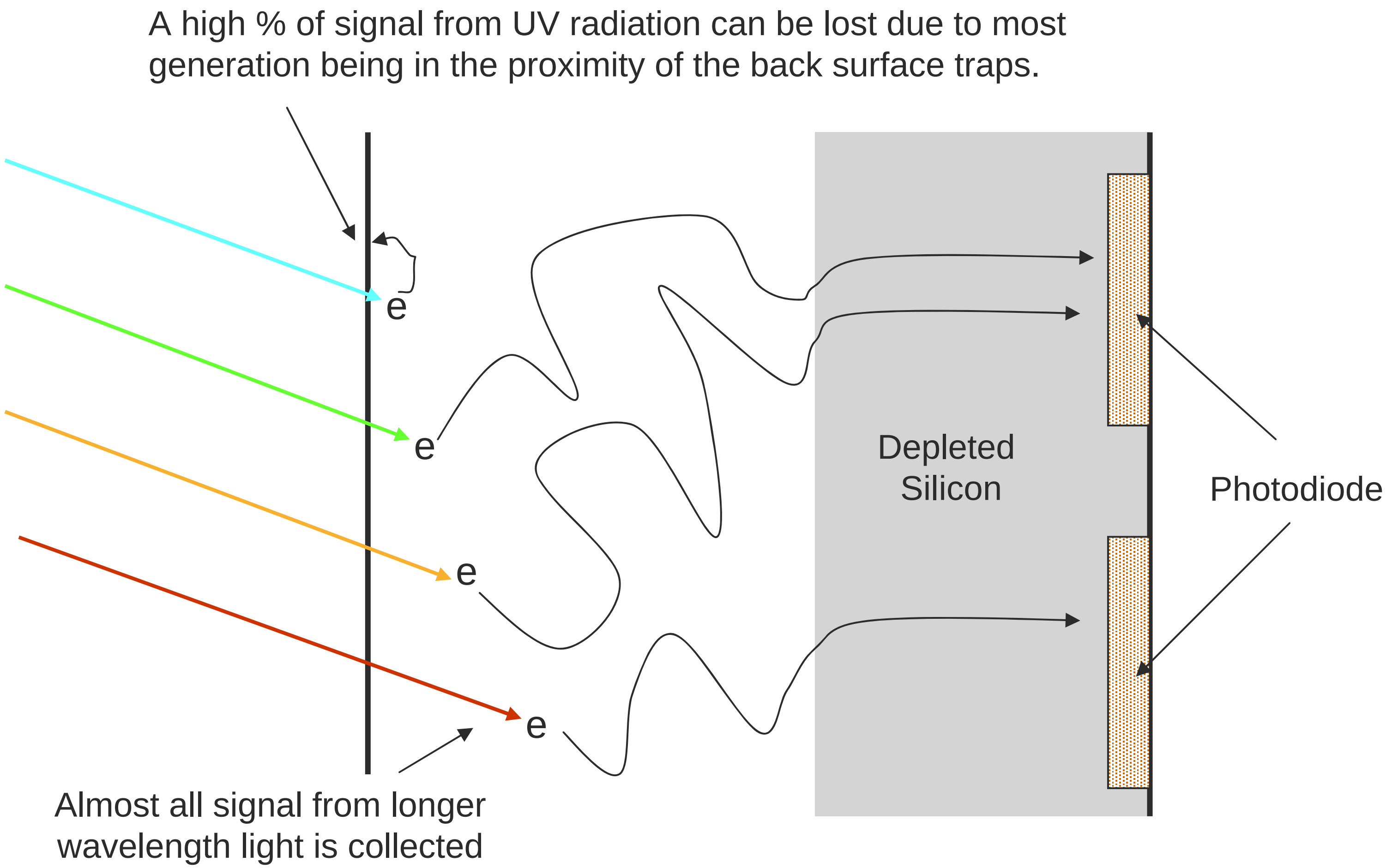
- The process has been successfully used on CCDs for nearly 20 years.

- A similar back-thinning process can be used for CMOS sensors and the first such devices were successfully thinned over 6 years ago.

© e2v technologies (uk) limited

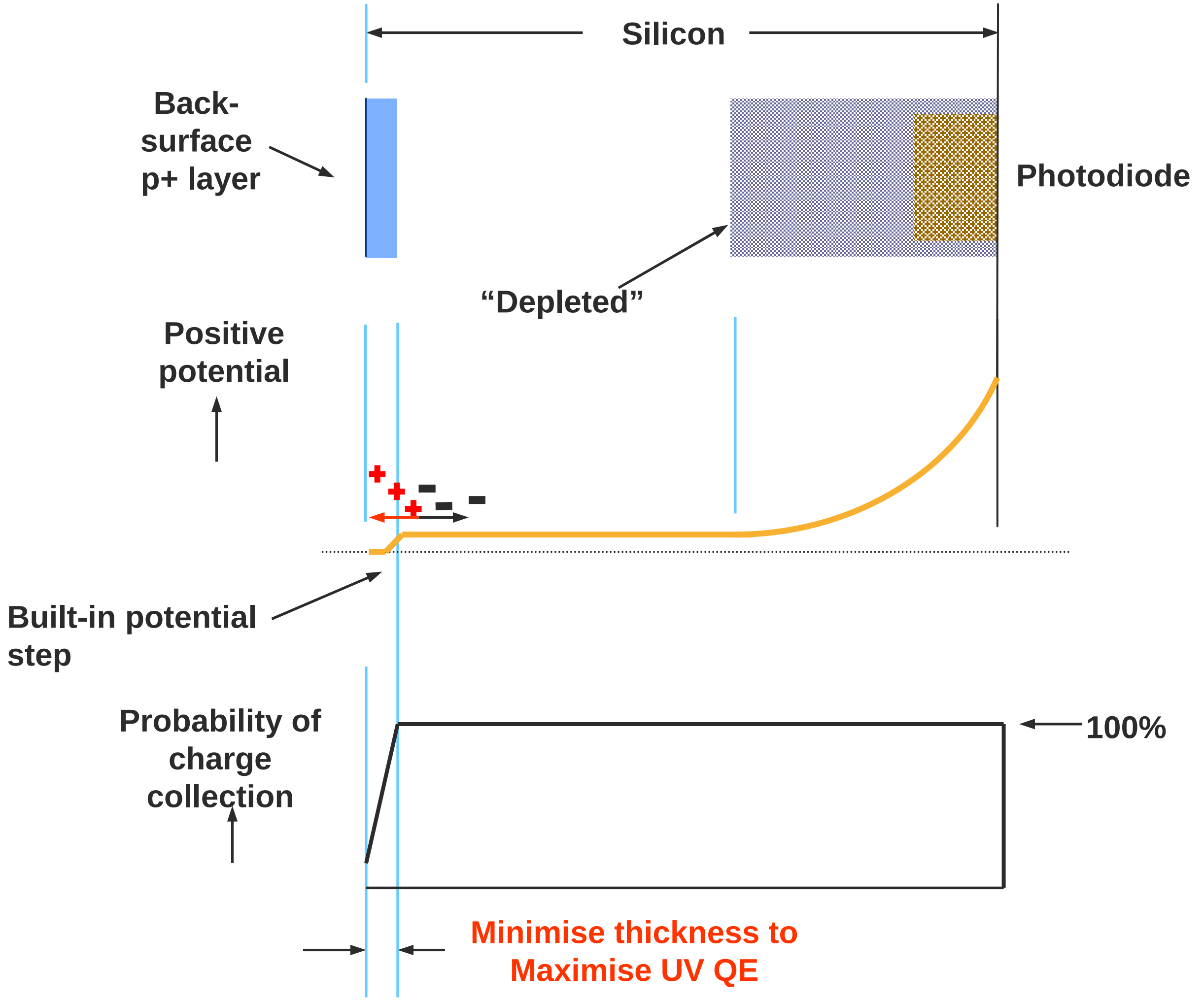
Introduction to back-thinning

➲The back surface passivation and AR coating are the critical factors that determine the QE of backthinned sensor.



© e2v technologies (uk) limited

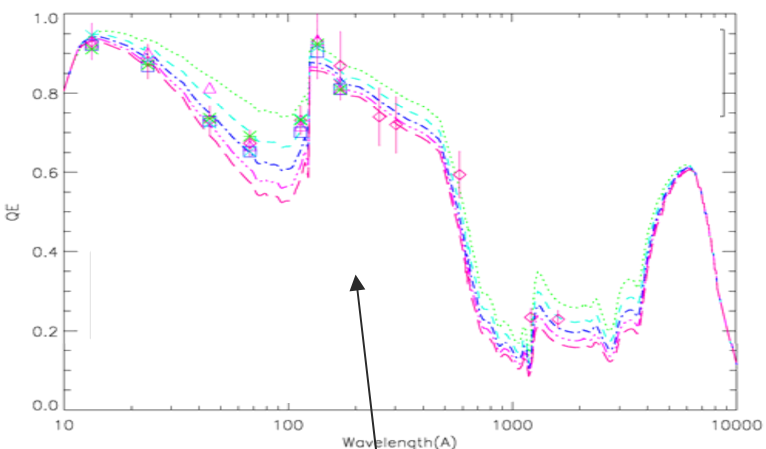
Introduction to back-thinning – QE model



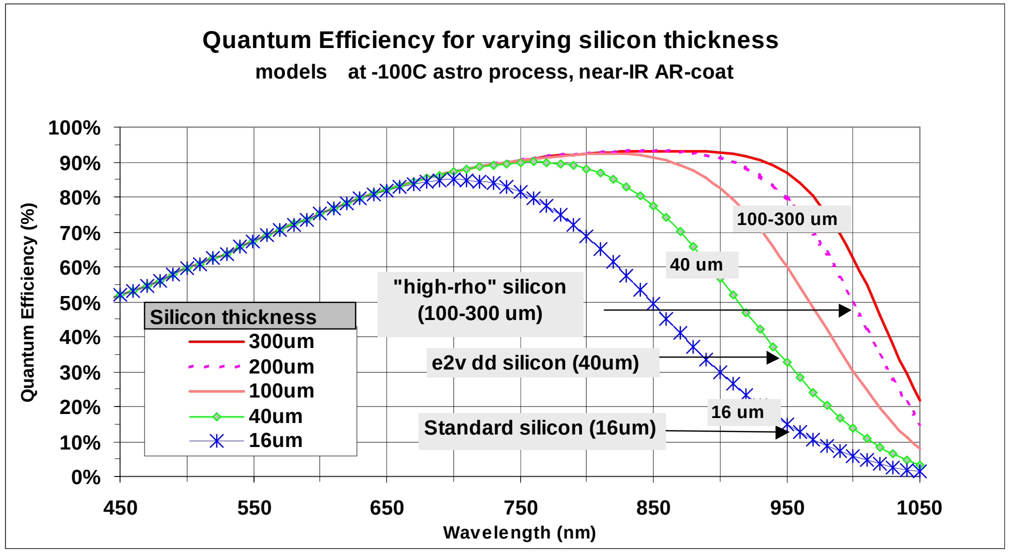
© e2v technologies (uk) limited

CCD back-thinning results

➲ With appropriate optimisation, CCDs have been produced to give excellent QE at optical wavelengths ranging from 1 Angstrom for UV applications right through to “Hi-Rho” devices now giving very high QE at NIR wavelengths



Vac UV to soft X-ray.
Data by Stern, LMMS



Devices optimised for NIR response

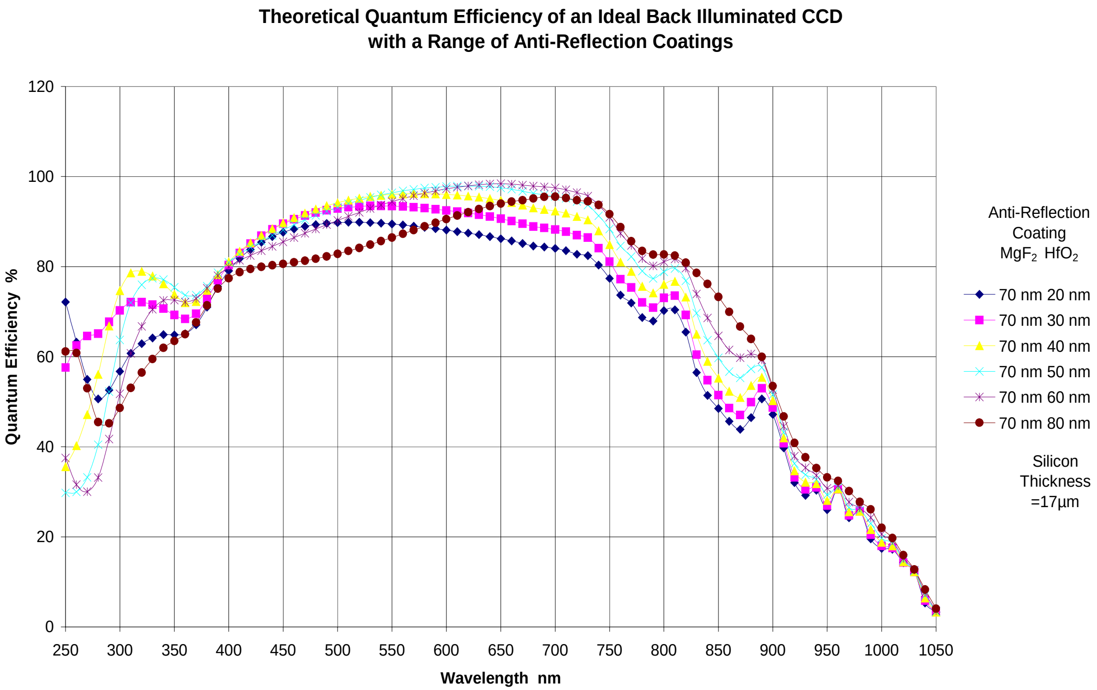
© e2v technologies (uk) limited

Introduction to back-thinning

- An antireflection coating is also critical to fully optimise optical performance

- Most e2v devices use a single-layer AR coating, which generally gives the best QE over a reasonably wide wavelength range.

- New two-layer coatings have been developed that give a significantly broader response.



© e2v technologies (uk) limited

0.5MPixel Sensor Back-thinning

- A recent programme has been to back-thin e2v's 0.5MPixel CMOS sensor

- 864 x 640 pixels
- 5T Pixel, 5.8 µm square
- Chip 8.08 mm x 7.78 mm with pads
- 1.8 V Digital / 3.3 V Analogue Supply
- Column ADC 8 bits
- **Global shutter** for capturing fast moving objects and eliminating distortion
- **High speed** (60fps) with 8 bit parallel output
- **High dynamic range capture** of a scene to reduce saturation in bright areas

© e2v technologies (uk) limited

0.5MPixel Sensor Back-thinning

- This programme has been carried out using epitaxial silicon thicker than the standard 5 μm. This is necessary as the thinning process cannot stop at the epitaxial interface and generally removes several μm of the epitaxial layer.

- In this case the final device thickness is ~ 8μm

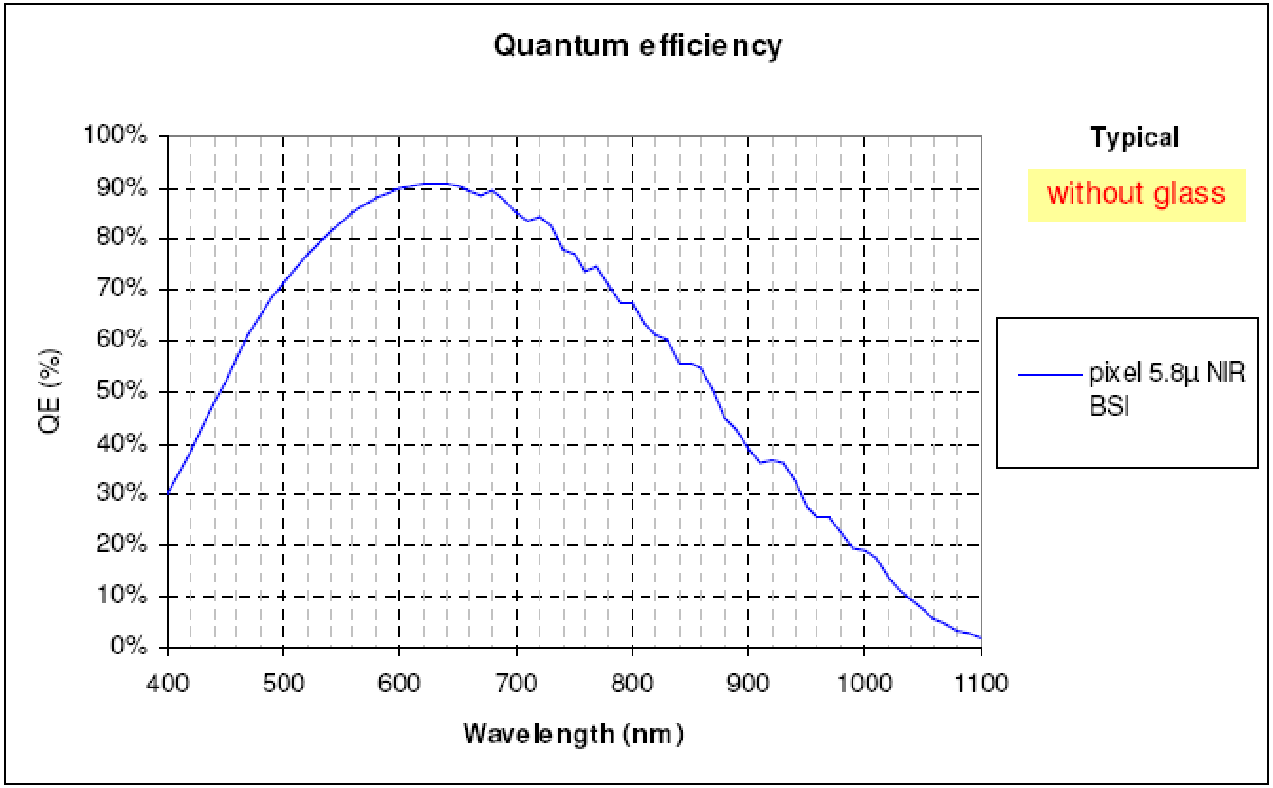
- Results are shown on the following slides:

© e2v technologies (uk) limited

0.5MPixel Sensor Back-thinning - QE

➲ The back-surface process is the low temperature thermal anneal type optimized for visible wavelengths and the QE results match the expected model very closely.

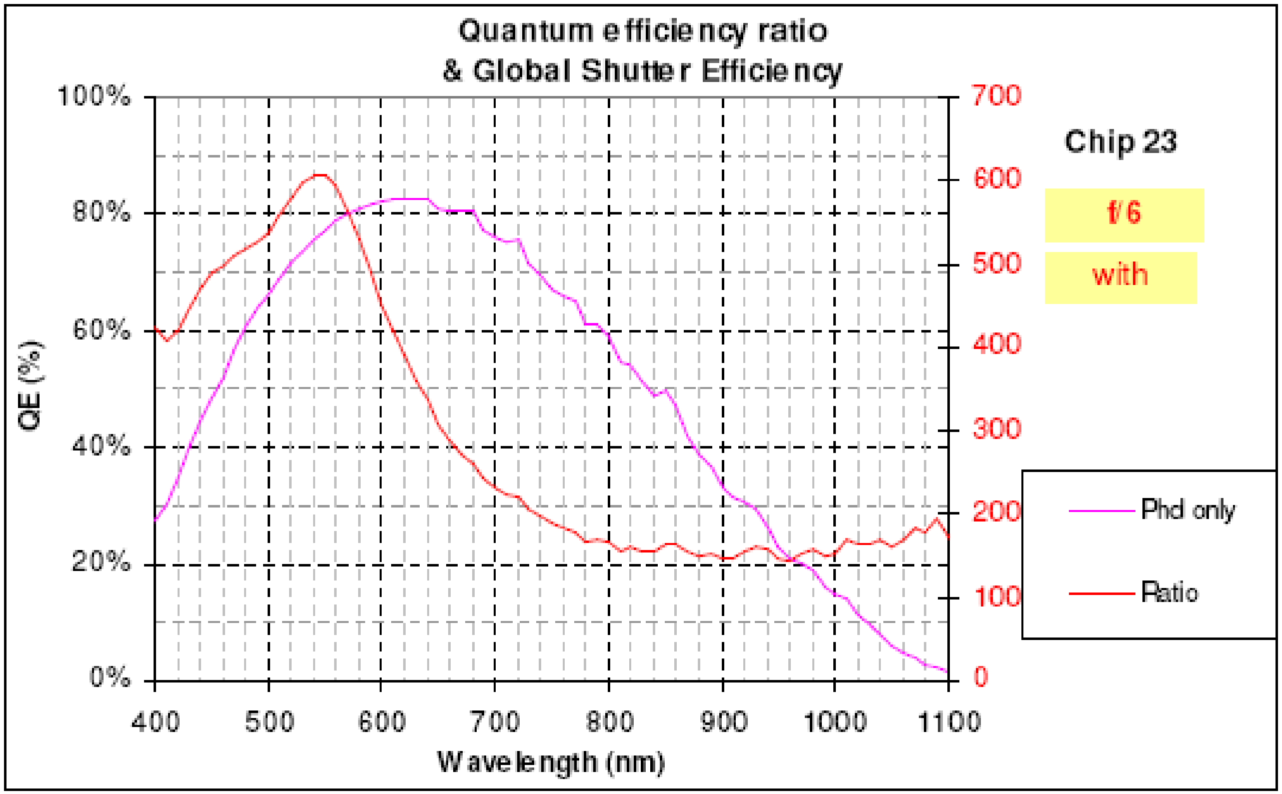
➲ The good match means that the fill factor is very close 100% (i.e. no charge is lost to the pixel circuitry) and results are in fact close to those seen with CCDs.



© e2v technologies (uk) limited

0.5MPixel Sensor Backthinning – Shutter efficiency

- The shutter efficiency with no shielding of the node is still very good (this is a 5T snapshot pixel)
- No optimisation of the node design has been carried out and further improvements are certainly possible



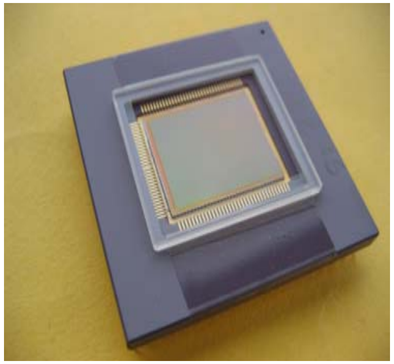
© e2v technologies (uk) limited

UV-optimised Process

- A second recent CMOS back-thinning programme has focussed on optimising UV performance

- This has used a 2MPixel device designed and developed by Astrium in cooperation with ISAE/CIMI and used for the GOCI space instrument.

Number of pixels	1415(H) x 1430(V)
Pixel Size	14.81 µm x 11.53 µm
Image area	20.96 mm x 16.49 mm
Optical Fill factor	65%
Conversion gain	4.75 µV/e
Dynamic range	0.98 V
Data rate	10 MHz
Package	Pin Grid Array (PGA)
Power consumption	50 mW



UV-optimised Process

- The sensor was intended for use in the standard front-illuminated mode, but two wafers were back-thinned despite being on silicon that was really too thin and the sensor layout was not designed for thinning

- The first device was processed with a visible optimised process with low temperature thermal anneal

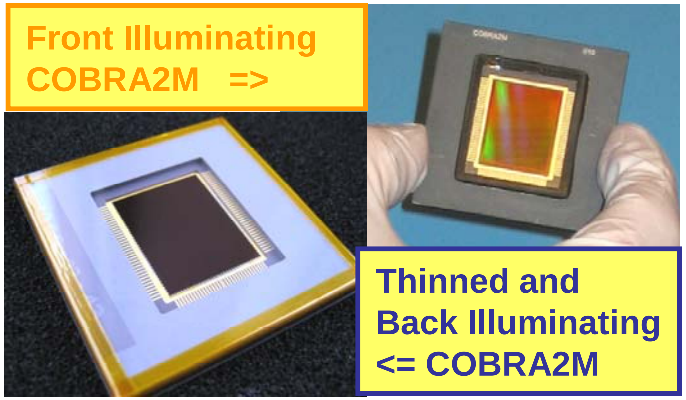
- For the second wafer an implant and anneal process was used with both an optimised implant and variants of the laser anneal process for QE optimisation.

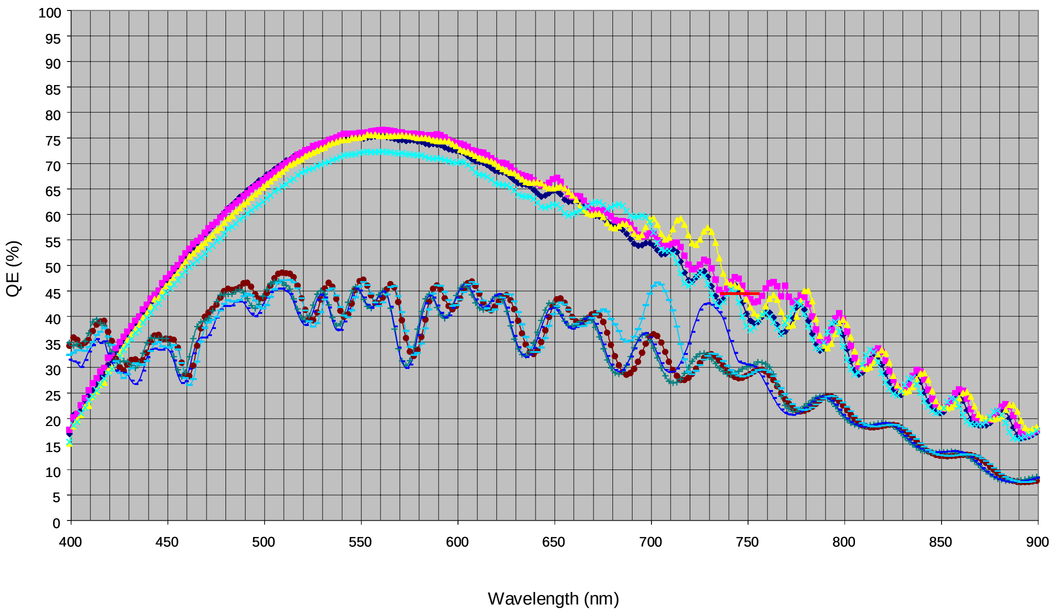
- Both wafers were on standard silicon and so the devices were only 3-4µm thick after backthinning.

© e2v technologies (uk) limited

UV-optimised Process

➲The first wafer gave results very close to the expected model with good QE in the visible but relatively poor QE at 400nm. Note that the QE curve has much less structure than for a FF device





The following parameters are all identical to FF measurements

➲CVF

➲Saturation signal

➲Output noise

➲Dark signal is significantly lower (÷2)

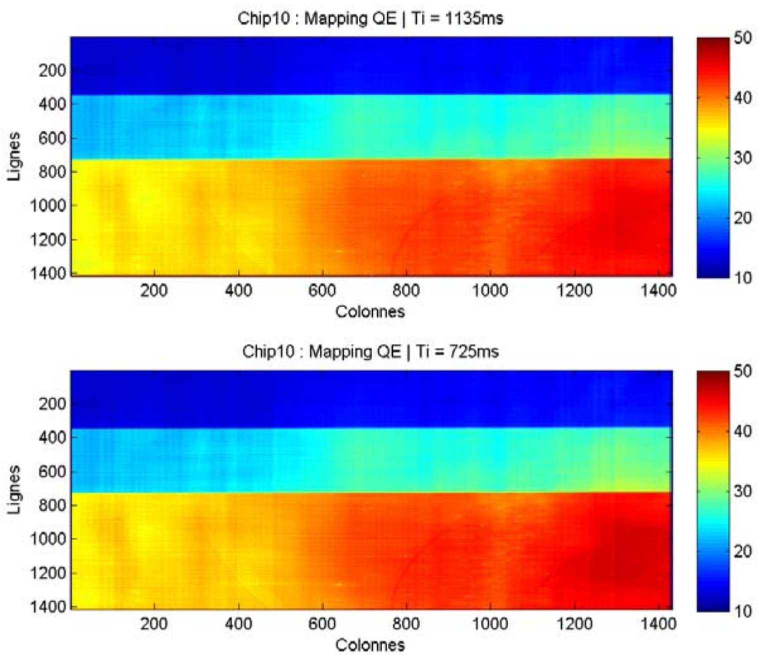
© e2v technologies (uk) limited

UV-optimised Process

➲ Each device on the UV processed wafer had a number of different laser anneal processes, with a total of 12 different processes. The best devices have a QE very similar to that which is obtained with our normal UV thinning process on CCDs.

➲ A typical image from one device is shown below and the different QEs of the stripes can be clearly seen.

QE = stripe 7, 8 and 9
stripe 9 = 9%
stripe 8 = 16.5%
stripe 7 = 26%



© e2v technologies (uk) limited

UV-optimised Process

- The measured QE for all variants is

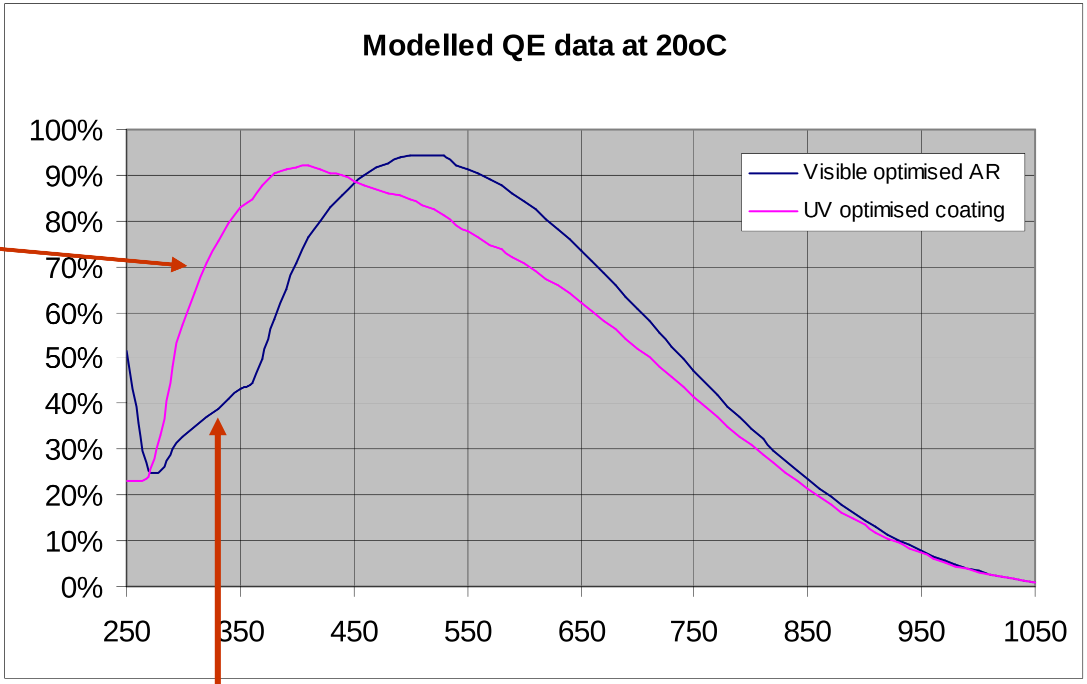
Variant	Measured QE at 320nm
1	25%
2	28%
3	28%
4	32%
5	32%
6	30.7%
7	26%
8	16.5%
9	9%
10	7.5%
11	15.3%
12	21%
Low temp thermal anneal	4%
FF sensor	13%

- As can be seen, there is a good process window around the process used for variant 4.
- The AR coating used for this process was optimised for visible performance (see next slide), a coating optimised for UV would give dramatically improved results

© e2v technologies (uk) limited

UV-optimised Process

➲ The device used for the UV performance assessment had 650nm of Si_3N_4 as an AR coating. Modelled performance from this coating (assuming a perfect surface) is shown below as "Visible optimised AR". Also shown is performance for a UV-optimised coating.



A UV-optimised coating would give over 70% QE at 320nm

Predicted QE at 320nm is 37%

© e2v technologies (uk) limited

Future developments

- The next step is to thin devices on optimised silicon

- In order to obtain QE values equivalent to the best CCDs, thicker epi is needed – which must be much more lightly doped as the voltage available for depletion is significantly less for CMOS sensors than for CCDs

- Two programmes are in progress to fabricate and then thin sensors on lightly doped epi, with a target of obtaining a depletion depth of at least 10 - 12μm with standard voltage levels

- The device must of course be designed to operate with the lightly doped material.

© e2v technologies (uk) limited

Acknowledgements

- Thanks to all who have provided data for this talk, particularly:

- Vincent Hibon
- Joel Vaillant
- Yann Henrion
- Neil Guyatt
- David Burt
- Andrew Harris

e2v technologies

- Olivier Saint-Pe
- Michel Breart de Boisanger

EADS Astrium

© e2v technologies (uk) limited