Measurements and Analysis of a 13um Pitch Charge Transfer TDI Suitable for Space Applications Using a Standard CMOS Technology

Frederic Mayer, Bruno Gili, Henri Bugnet, Frederic Ramus,
Frederic Devriere, Thierry Ligozat

CNES Workshop 26-27 November 2013

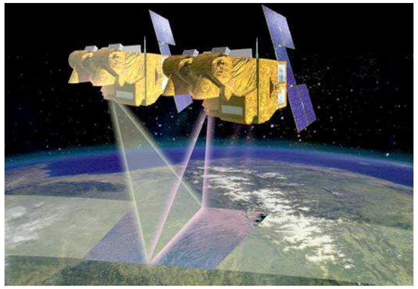
Summary

- Quick description of the TDI function
- Presentation of the test chip and the CMOS TDI pixel architecture
- Electro-Optical results
- Optimized Future TDI Architecture
- Conclusions

Why working on Time Delay Integration (TDI)?
➔ for high sensitivity, high speed applications

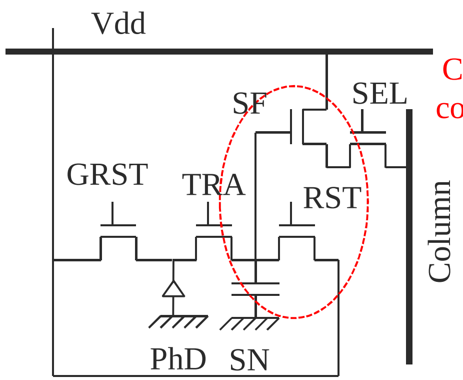
- Main Applications:
  - Machine vision (high sensitivity , high speed)
  - Space Earth observation (high sensitivity, SNR boost to overcome shot noise limitation)
- **Why moving from CCD to CMOS:**
  - Less cost at system level
    - Compact system (better integration with numeric on chip, more functionality
    - Lower power consumption
    - Smaller pixel size
  - …And ultimately better performances?
- **Eliixa+ is a successful TDI CMOS but is limited to 4 TDI lines**

➔ A new architecture is needed to overcome the limitation of the Eliixa camera



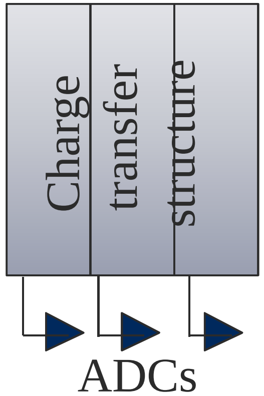
2 main ways to achieve TDI operation in CMOS technology

TDI mode (Charge summation) is done in the digital domain



Charge to voltage conversion is done at pixel level

TDI mode (Charge summation) is done inside the pixel



Charge to voltage conversion is done at column level after the charge summation

	Digital Summation	Charge Transfer Summation
Dynamic range	“Unlimited” Qsat	Qsat limited by pixel
Detectivity level	High noise level	Low noise level
Motion MTF	Spatial oversampling needed	Multiphase pixel
ADC speed	Slope ADC not suitable	Operating at line rate
Pixel architecture	Standard pixel	Charge transfer hard to achieve in CMOS IS process

Summary

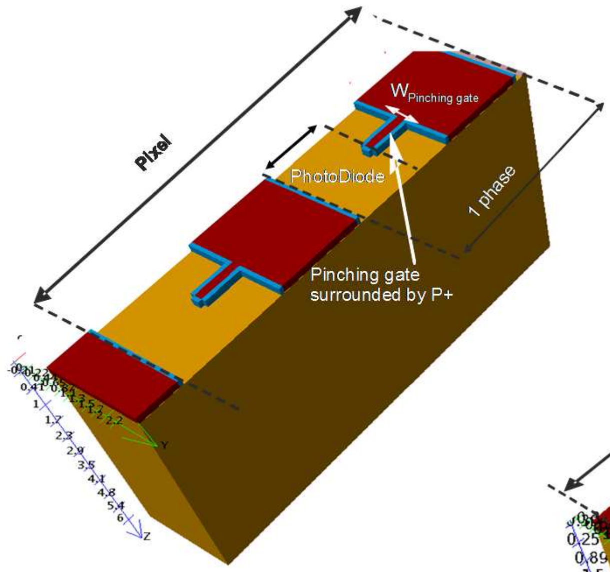
- Quick description of the TDI function
- Presentation of the test chip and the CMOS TDI pixel architecture
- Electro-Optical results
- Optimized Future TDI Architecture
- Conclusions

Charge Transfer Structures

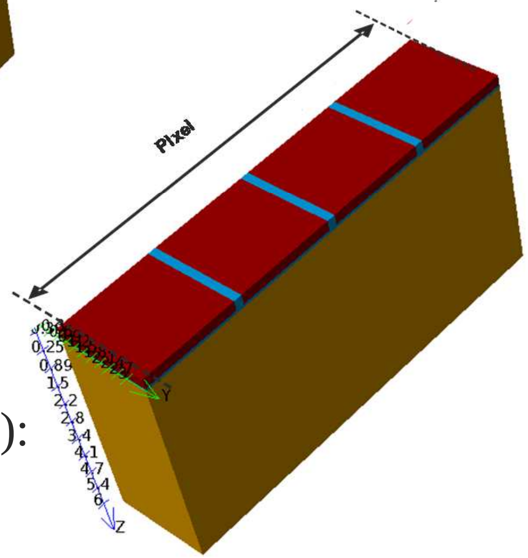
E2V developed the charge transfer TDI in order to benefit from:

- Absence of summation noise
- High motion MTF

Two structures are fabricated using a standard CMOS IS process



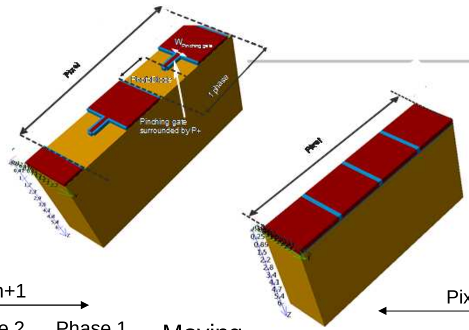
"Classical" CCD like structure



"Hammershape" structure (2 phases in this example):

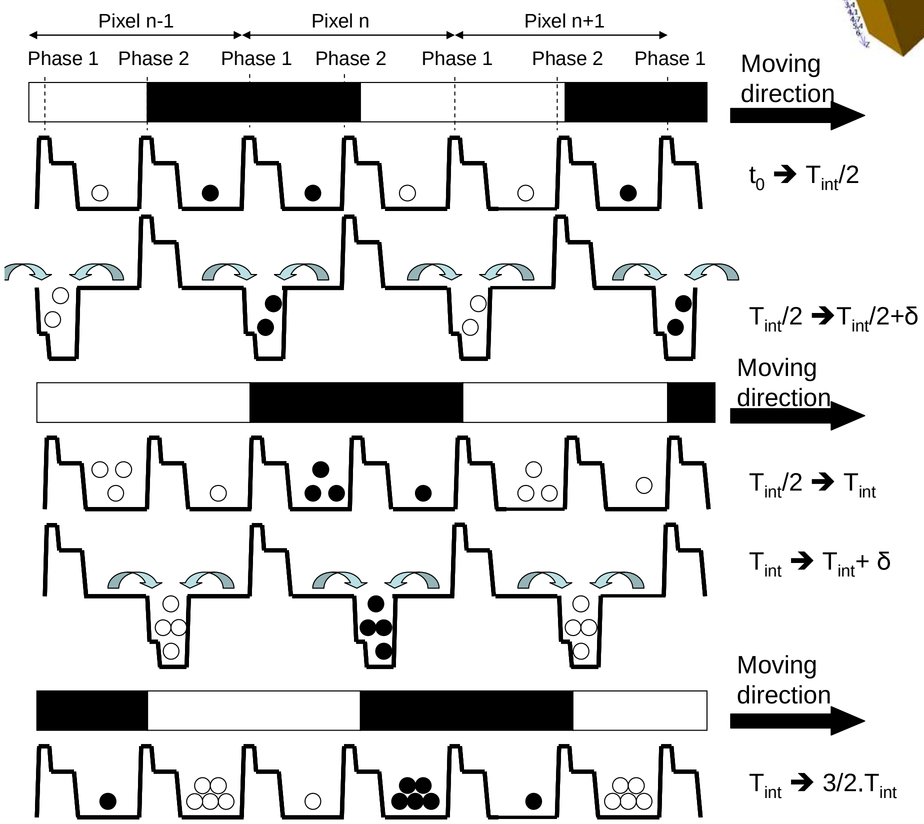
- 1 phase is composed of:
    - a photodiode part
    - a pinching gate
    - a transfer gate
- High fill factor due to the photodiode part

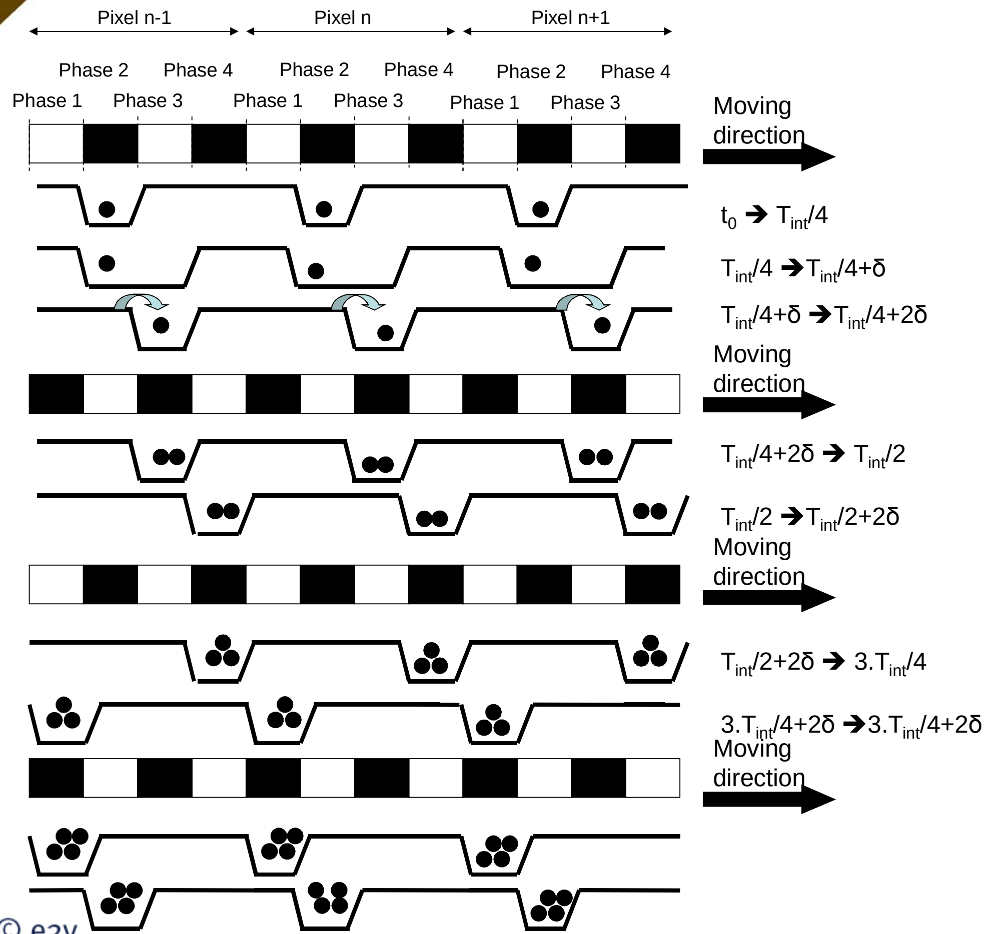
Comparative operation of both transfer structures



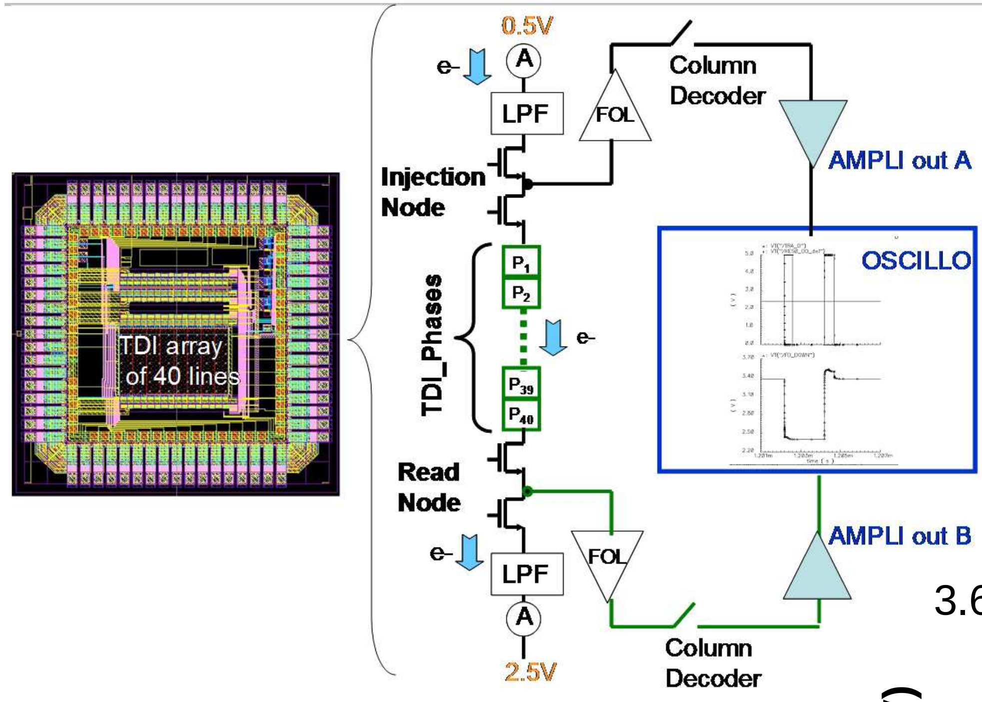
“Hammershape”

“CCD like”



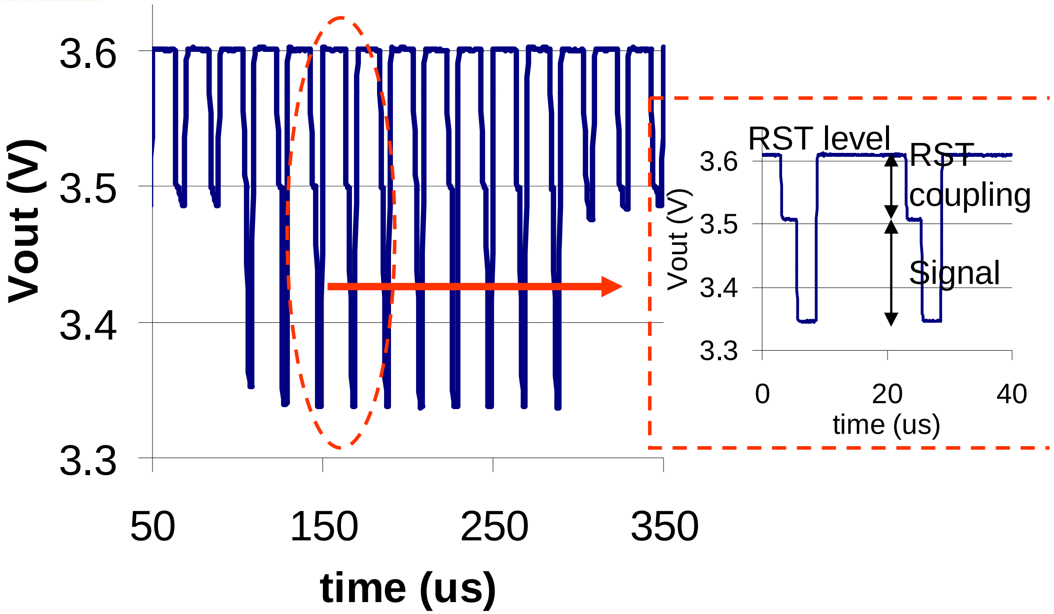


Test Chip Organization



- Full analog test chip
- 40 lines of TDI
- Devices 7um & 13um
- Possibility of controlled electrical charge injection

- “Classical” CCD video signal: RST/RST coupling/Signal

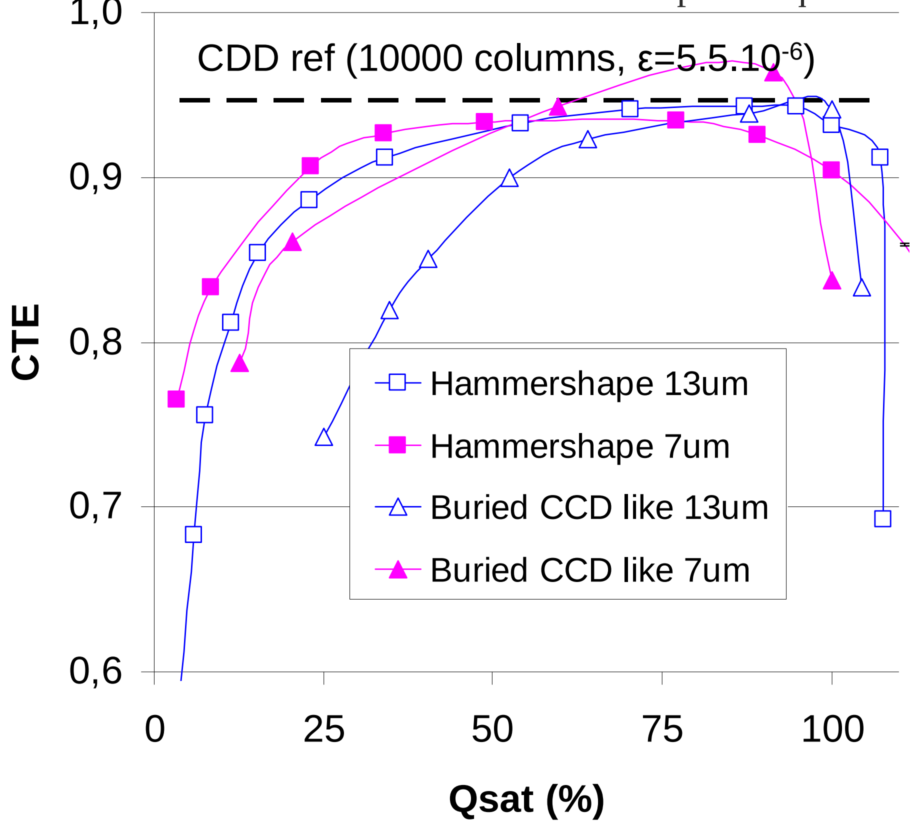


Summary

- Quick description of the TDI function
- Presentation of the test chip and the CMOS TDI pixel architecture
- Electro-Optical results
- Optimized Future TDI Architecture
- Conclusions

CTE Comparison between both Structures

*CTE of CCD like is done
for a 2-phase equivalent



CTE is measured as :

$$CTE = (1-\varepsilon)^{Nb_{stages}}$$

$$CTI = 1 - CTE$$

$$\varepsilon = \frac{\sum_{residual} V_{empty}}{Nb_{stages} . V_{signal}}$$

- Carriers can be converted into voltage at the bottom of each column
  ➔ fewer transfers compared to CDD (no need for horizontal registers)
  ➔ CTI requirements are relaxed compared to the CCD

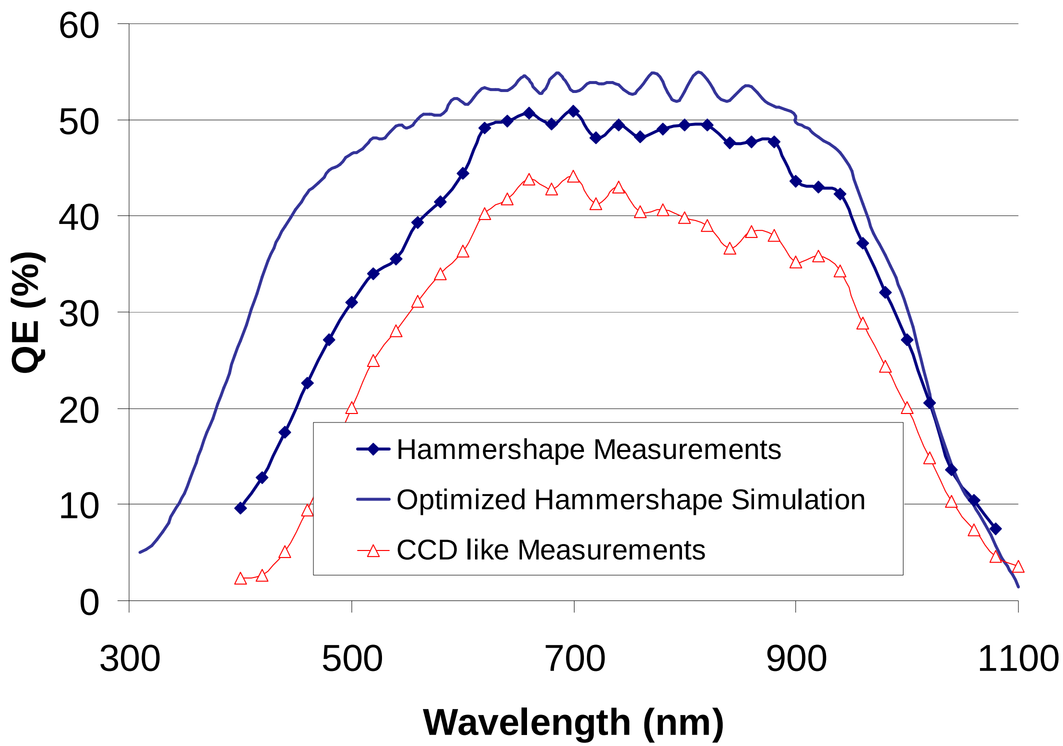
- At low level, the CTE is better for the Hammershape structure because the carriers are stored in the photodiode and thus are far away from interface states.

- Furthermore, the CTE discrepancy between 7 and 13um is smaller for the Hammershape structure

- Qsat CCD like > Qsat Hammershape

QE and MTF Comparison between both structures

- Actual Hammershape: photodiode ~25% of pixel
- Optimized Hammershape: ~75% of photodiode area
- Poor QE in blue for the CCD like due to the poly absorption
- No ulenses
- Use of Bulk wafer ➔ high QE in NIR (but lower MTF)



LED Wavelength (nm)		505	650	870
Static MTF across the track (%)	Hammershape	65	51	22
	CCD like	66	51	19
Static MTF along the track (%)	Hammershape	53	43	21
	CCD like	47	38	15

- MTF across the track is similar in both cases
- MTF along the track is slightly better for the Hammershape structure, but not sure why…

Summary

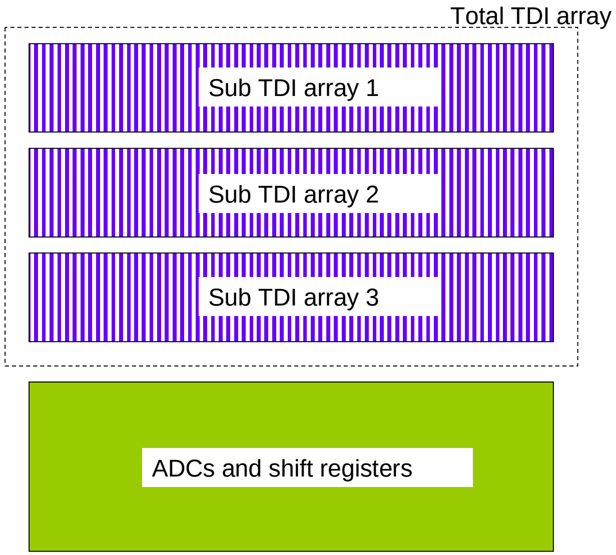
- Quick description of the TDI function
- Presentation of the test chip and the CMOS TDI pixel architecture
- Electro-Optical results
- Optimized Future TDI Architecture
- Conclusions

Future Work: Optimized TDI array (1/2)

- CCD like: high Qsat, lower CTE
- Hammershape: lower Qsat, better CTE
- CTE may degrade after irradiation at the end of the mission's life…

➔ For all these reasons, splitting the TDI array into a few sub arrays (typically 2 or 3) will relax the CTI requirement, increasing the Qsat and giving some margin versus end of life requirements

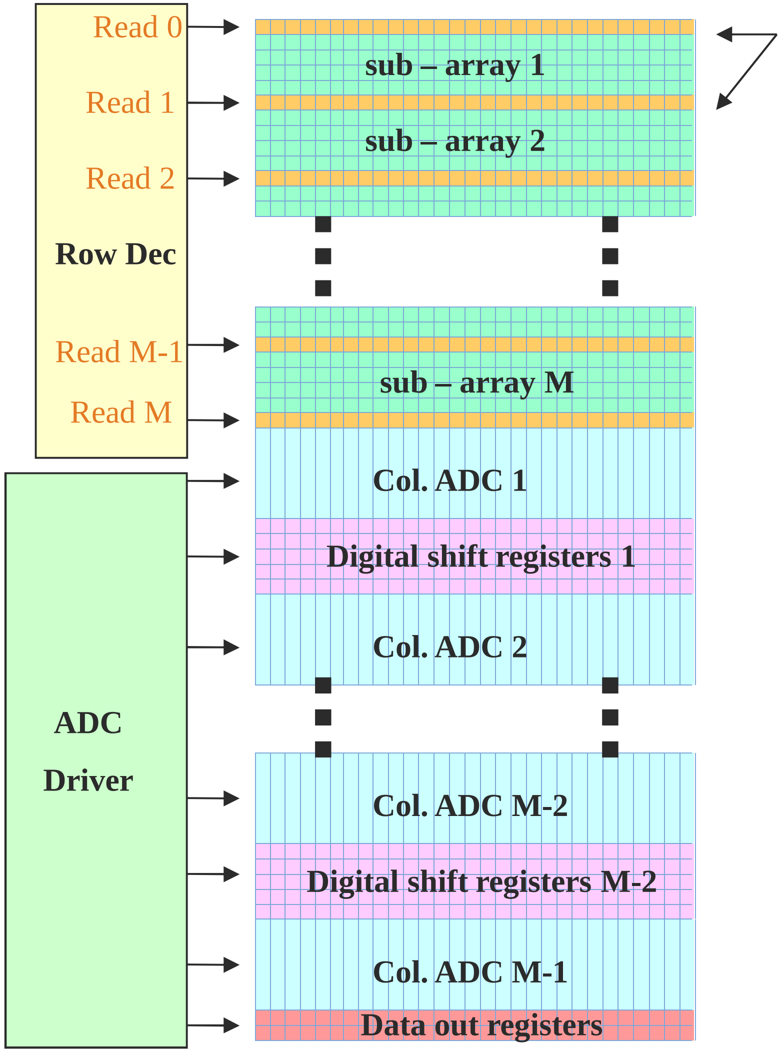
➔ The sub TDI will be added digitally



Adding the sub arrays may also enable some new features like misalignment corrections

Future work: Optimized TDI array (2/2)

➔ The trade-off could be splitting the TDI pixel array in 2, 3 or M sub-arrays



➔ Relaxed requirement for CTE

➔ Full Well enhanced by a factor M

➔ Each data has the same processing

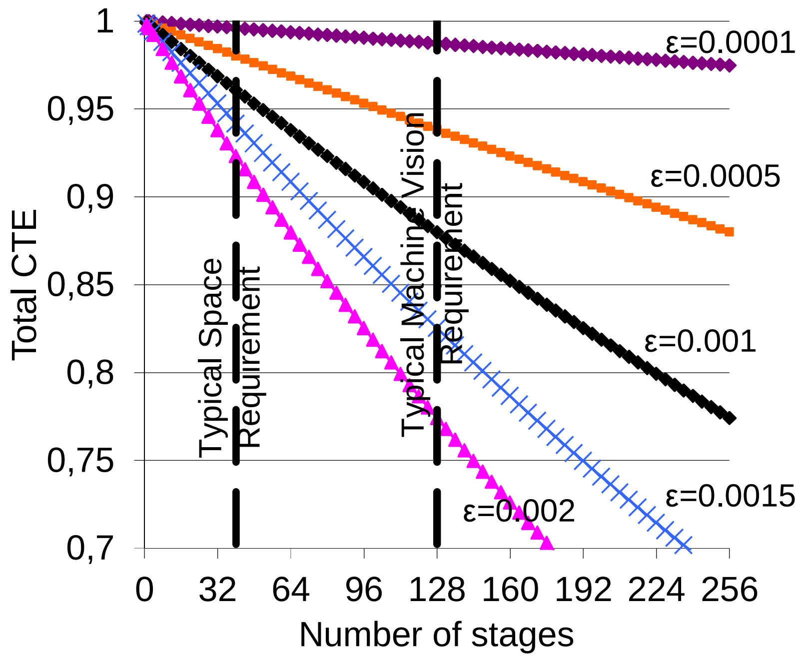
➔ Optimization of ROW FPN

➔ Bi-directionnality supported

but…

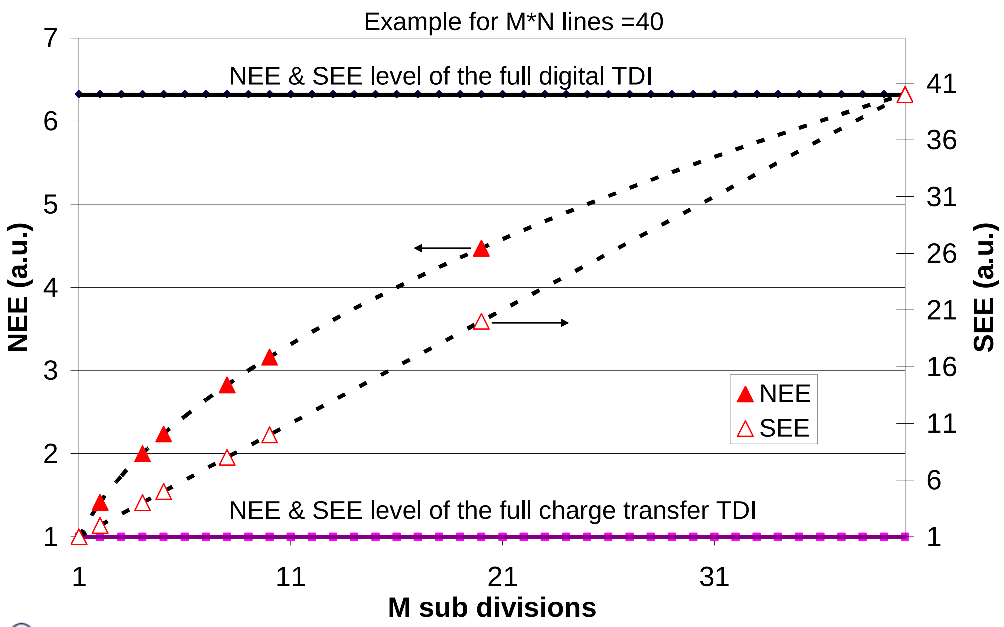
➔ Read Noise degraded by √M

Future work: trade off between the number of sub TDI



As the digitalization is done column wise, the number of transfers is limited to the number of TDI stages, unlike the CCD.
Thus what is an acceptable unitary CTI (ε) for a CMOS TDI ?
In order to achieve high CTE, with a $\varepsilon \sim 10^{-3}$, a sub TDI of 20 lines could be a good compromise

Increasing the number of sub divisions raises both the Noise/Saturation Equivalent Energy (NEE/SEE) thus on one hand leading to a poorer detection level, but on the other hand leading to a higher saturation level.



Conclusion

- E2V developed two charge transfer architectures using a classical IS CMOS process: a CCD like structure and an innovative high QE structure called “Hammershape”

- Both devices were fabricated with a 13 and 7 um pitch, characterized and compared

- An optimized architecture for future TDI was presented: splitting the main TDI array into sub-TDIs allows to relax the CTI constraints and improve the saturation level while keeping low detectivity level.

- The next step is to improve slightly the charge transfer efficiency of the structures and to optimize the pixel geometry…

Thank you for your attention !
... And now it’s time for questions