Electron Multiplying Device Made on a 180 nm Standard CMOS Imaging Technology

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I. ABSTRACT

In this presentation we show an Electron-Multiplying (EM) CMOS image sensor. This work includes the experimental study of two approaches and various EMCMOS pixels arrays have been implemented into the test circuits. The results have confirmed the increase of SNR with both approaches. This was demonstrated by the electro-optical measurements and on the captured images. The theoretical equations have been validated from experimental results, especially the new formulation of the gain versus multiplication steps for the structure featuring the multiplication into the photodiode.

II. INTRODUCTION

Despite the progress in this area, the sensitivity of CMOS image sensors are still limited by the read noise for extremely low light applications (few tens µlx). The EMCCD that operates with electronic multiplication has shown the potential of this noise reduction technology, making it of great interest to the scientific market. In general, CCDs have gradually been replaced by CMOS imagers and EMCCDs can potentially move to EMCMOS [1]. Like EMCCD, this technology is planned to be used to improve image quality at very low light levels for science or surveillance applications.

CMOS technology enables lighter and smarter systems, lower power consumption and are less expensive for large sale volumes (SWAP-C approach). The principle of electron multiplication is to apply a gain to the signal before any noise addition by the readout chain. The noise is virtually divided by this gain and SNR is improved. As a result of the CCDs principle, the signal is transferred in the form of electron packets and the multiplication is applied commonly to each pixel before reading out. For CMOS, the signal is in voltage domain, which means that the multiplication must be applied prior to transfer to the floating node and before adding the noise from the source follower transistor. There are various approaches to achieve the multiplication and this study focuses on two particular structures: multiplication in the photodiode and multiplication in the storage node, each with different impacts on multiplication gain and variance formulation.

III. CHARGE MULTIPLICATION PRINCIPLE

When an electric field greater than 1E5 V/cm is applied in silicon based material, the carriers are accelerated and gain sufficient energy above the critical energy U_C to behave like an ionizing radiation and can produce electron-hole pairs. This phenomenon is called impact ionization and was described previously by Chynoweth [2]. The efficiency of electron-hole pairs generation is characterized by the ionization coefficient noted α (%) which depends mainly on the effective electrical field E ($V.cm^{-1}$) and the mean free path of carriers L (cm) which is the distance traveled by the carriers between two collisions. Unlike for N/P junction, in a CCD or CMOS based detector, electrons are collected and holes are drained by the ground. As a consequence, only electron multiplication mechanism is operated. A calibration of the multiplication gain made with EMCCD confirms the model from Lackner [2] initially described for N/P junction and with adjustment of the constant as follows:

$$\alpha = \frac{1}{Z}\exp\left(-\frac{U_C L^{-1}}{E}\right) \quad (1)$$

With $U_C L^{-1} = 1.6E6$ V/cm and Z the Lackner's correction parameter of the Chynoweth's law:

$$Z = 1 + \left(\frac{U_C}{E}\right)\exp\left(-\frac{U_C}{E}\right) \quad (2)$$

Considering a relatively low probability of collision, the overall multiplication gain can be simplified from the avalanche multiplication factor m as follows:

$$M = m^N = (1+\alpha)^N \quad (3)$$

This equation states that the number multiplication N applies recursively to an initial charge. The multiplication process adds noise to the shot noise in relation to the successive application of stochastic processes during the impact ionization. The noise multiplication factor is denoted F. Excess noise formulation has been widely described in the literature for the EMCCD [4][5] and more recently for EMCMOS [6] by proposing a universal formulation for the equivalent gain $\langle m^{eq} \rangle$ and the excess noise factor including the branching model:

$$F^2 = \frac{\sigma_{out}^2}{\langle m^{eq} \rangle^2 \sigma_{in}^2} \quad (4)$$

This model is still valid when the multiplication is performed in parallel to the integration. The expression of $\langle m^{eq} \rangle$ is composed by two terms as follows:

$$\langle m^{eq} \rangle = \underbrace{(1-Np)m^N}_{serial} + \underbrace{p\frac{m^N - 1}{m-1}}_{parallel} \quad (5)$$

The term p is the probability mass function of the carriers arriving during a multiplication step. Therefore, by applying this formula from the measured equivalent gain $\langle m^{eq} \rangle$ corresponding to multiplication, it is possible to calculate the value of $m = (1+\alpha)$.

IV. PIXELS IMPLEMENTATION

In principle, the charge multiplication must operate upstream of the charge-to-voltage conversion in order to reject the noise added by the readout chain including the pixel source-follower. Two approaches are proposed in this study. The first pixel comprises multiplication electrodes implanted in the photodiode as shown in Figure 1 and presents an optimal fill factor. Multiplication is performed in parallel to the arrival of the photons.

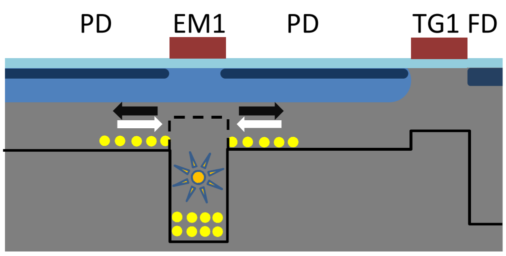


Figure 1 – Electron multiplying pixel-I

The second pixel consists of a conventional pinned photodiode joined to a multiplication stage as shown in Figure 2. In this case, the charge multiplication occurs after charge integration.

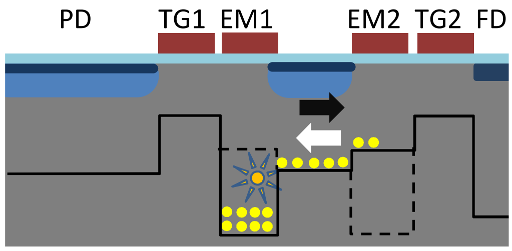
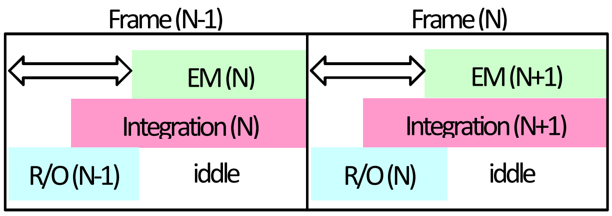
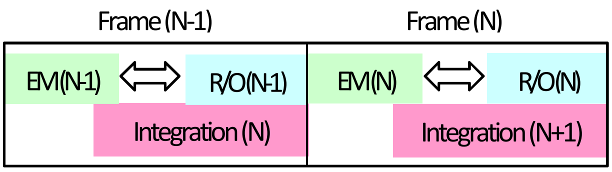


Figure 2 – Electron multiplying pixel-II

On the pixel-I, the EM gate is pulsed in such a way that the charges are transferred between the pinned photodiode and the potential well. At each passage, impact ionization operates and produces a multiplication gain that can be modulated depending on the number of cycles. According to the same principle, the EM gates of the pixel-II are pulsed in phase opposition in such a way that the charges move back and forth around the pivot potential. In a video mode, electro-multiplication is performed in parallel to the integration, resulting in no time loss as shown Figure 3 (a) and (b). The pixel-II is naturally used in a global shutter mode whereas the pixel-I is suitable for rolling shutter operation.



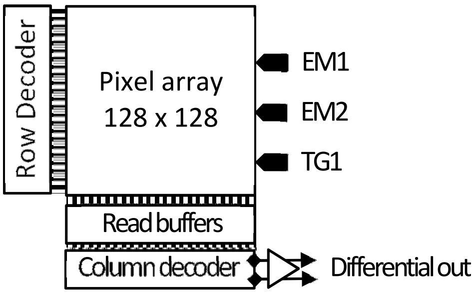
(a) Pixel-I



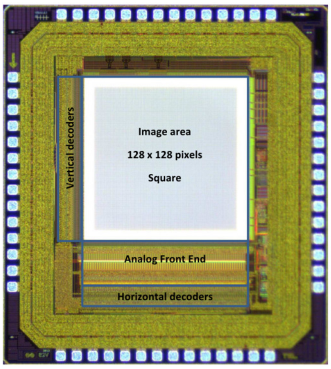
(b) Pixel-II

Figure 3 – Video sequence

The pixel circuit is composed of 128x128 pixels of 8µm pitch made on a 0.18µm 1P4M CMOS imaging technology. The Block diagram of the chip is shown in Figure 4(a). Pixel functionality is supported by the additional periphery blocks, including the 8-bit horizontal and vertical decoders, the analog front-end and the differential analog output. The global transfer and EM gates are provided in parallel for all pixels. Figure 4(b) shows the micrograph of the chip.



(a) Block diagram



(b) Chip Micrograph

Figure 4 –Block diagram and chip micrograph

The implementation and design of the pixels on CMOS technology were optimized using TCAD (Technology Computer Aided Design). A cross-section of pixel-II is illustrated in Figure 5 and shows the simulated potential maps corresponding to Figure 2.

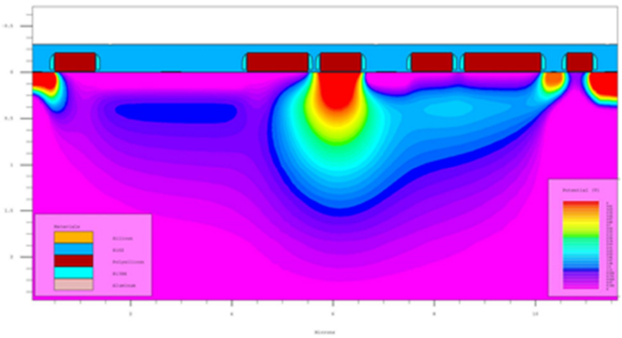


Figure 5 –TCAD simulation on Pixel-II

V. EXPERIMENTALS RESULTS

The measurements were performed in an environment dedicated to the single photon device characterization, the implementation of which is shown in Figure 6 (IPNL laboratory). The chip temperature is controlled and the acquisition system enables numerous measurements with the production of the associated statistics.

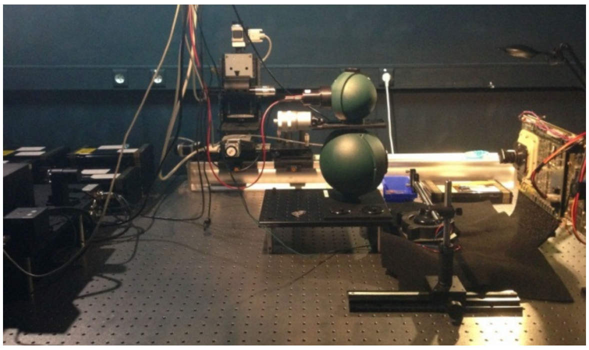


Figure 6 – Optical bench

The pixels embed a gate based structure to perform multiplication. The supplementary power dissipation *Pm* produced by the pulse generation is calculated by taking into account the actual capacity of the gates G_g based on a 180 nm CMOS technology and the frequency f_m. P_m is calculated assuming that f_m is equal to the number of multiplication necessary to achieve the gain M during the time Ti assumed 1/60 s as depicted in equation (5).

$$\begin{cases} P_m = C_g V^2 f_m \\ f_m = \frac{log(M)}{log(1+\alpha)\, T_i} \end{cases} \quad (5)$$

P_m is plotted on Figure 7 as a function of the gain M. The supplementary power dissipation is less than 10 mW per mega-pixel and was confirmed on the test pixel circuit.

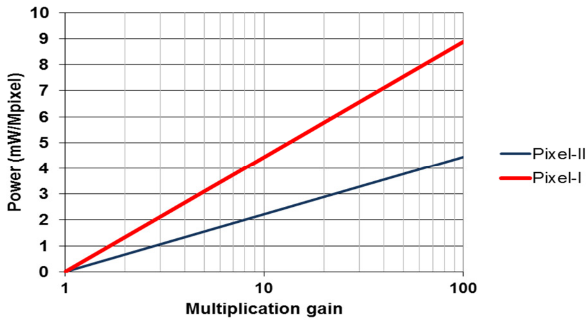


Figure 7 – Calculated power dissipation

The electron multiplication based on pixel II is plotted in Figure 8 for different electrical field values. The points represent the actual measurement of the average gain. The fitted curves are calculated using the analytical model. The multiplication probability factor α is deduced on the basis of the actual measurements. The dark current generated during the multiplication phase is also amplified on the model described in the equation (5) and can be characterized with respect to the number of EM reciprocation phases. This graphic shows that measurements are well aligned with the theory.

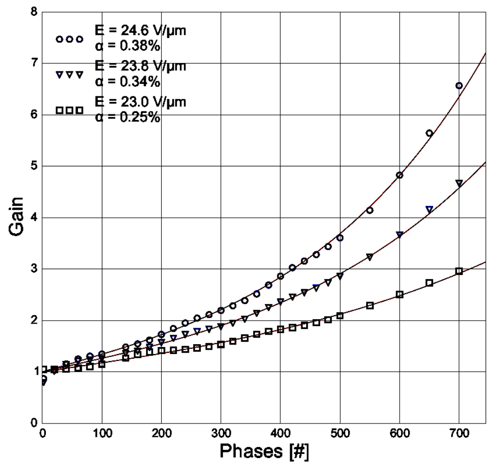


Figure 8 – Measurement of EM gain on pixel-II

The distribution of the ionization coefficient is plotted on Figure 9. It follows a normal distribution. The median value of α for this version of the pixel design is 0.43% with an RMS variation of 0.02%. This result shows a good reproducibility of the ionization factor for the 128x128 pixels of the array. It confirms the feasibility of using the EMCMOS technology on larger sensor formats.

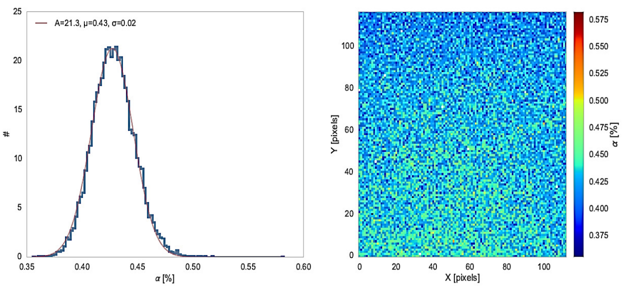


Figure 9 – Measured distribution of α on pixel-II

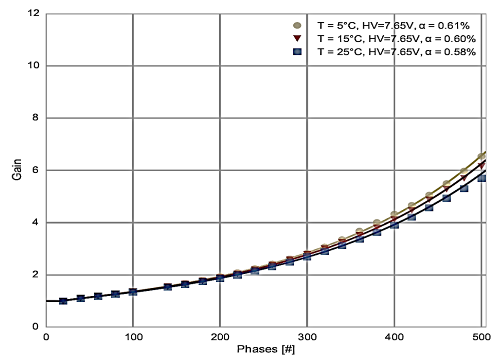
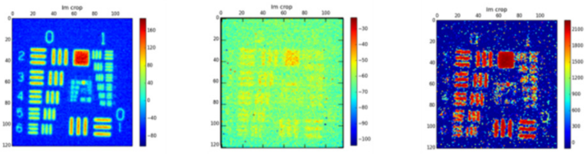


Figure 10 – Measurement of the gain vs the temperature on pixel-II

The variation of gain with temperature is shown in Figure 10. The α coefficient decreases as the temperature increases, which conforms to the theory (the mean free path L expressed in equation (1) varies in the opposite way direction with temperature). Figure 11 shows images in different conditions of a USAF 1951 test pattern made with a 128x128 pixel-I array. This demonstrates the increase of electron charge after electron multiplication.



(a) 1ke- **(b) 100e-** **(c) 5ke-**

Figure 11 – Pixel I - Images made under high illumination level (a), low illumination level without multiplication (b) low illumination level with 50x multiplication (c)

VI. CONCLUSION

In this work, we present a solid state solution suitable for low light applications. The proof of the concept is demonstrated with in-pixel electron multiplication and gain production on an actual image using a 180 nm standard CMOS imaging technology. Even though deeper study is planned, these results constitute the first breakthrough towards a full design.

ACKNOWLEDGMENT

This work was founded in part by the DGA, French MOD (Multimos program)

Special thanks to Jean-Marie Caupain for his support, Sylvain Ferriol and Cyrille Guerin for their valuable contribution.

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