Low-Light Technical Note 4
Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors

INTRODUCTION

The L3Vision™ Electron Multiplying Charge Coupled Devices (EMCCDs) from e2v technologies use a novel charge multiplication technique to facilitate gain in the charge domain and enable performance with an equivalent output noise of less than 1 e^- at pixel rates of over 11 MHz. Thus the sensors are excellently suited for scientific imaging where the illumination is limited or for TV applications at very low light levels.

The Technical Note 'The Use of Multiplication Gain in L3Vision™ CCD Sensors'[1] describes how the output noise can be effectively eliminated so that the noise is reduced to √2 of the photon shot noise[2] plus that due to any dark signal that is generated in the sensor.

The total dark signal consists of two components: the thermal dark signal due to the thermal generation of charge, and the Clock-Induced Charge (CIC), which is generated during the charge transfer operation. In this technical note the parameters influencing the dark signal and CIC are discussed, and it is explained how devices can be operated optimally to give the best possible performance. Note that although the context of this discussion is L3Vision™ EMCCDs, the conclusions apply with equal validity to conventional CCDs manufactured by e2v technologies.

THERMAL DARK SIGNAL

The thermal dark signal itself consists of two components: the thermally generated charge at the silicon surface (the surface dark signal, S_S), and that generated in the bulk (the bulk dark signal, S_B). For operation of a device in Non-Inverted Mode (NIMO) the total thermal dark signal SD is given by:

$$S_D = S_S + S_B \qquad (1)$$

Both the surface and bulk components of thermal dark signal are strongly temperature dependent and scale with the integration time.

The typical surface dark signal in nA/cm^2 is given by:

$$S_S = 122T^3e^{-6400/T} \qquad (2)$$

For NIMO device operation, this surface component is dominant, being typically two orders greater than the bulk component at room temperature.

If the device is operated in an Inverted Mode (also known as Multi-Phased Pinned, MPP), the surface dark signal is suppressed and only the bulk component contributes to S_D.

The bulk dark signal itself consists of two components, one due to diffusion current and one due to depletion current. Each of these components will have a temperature dependence of the form:

$$I = \text{const} \times T^n \times e^{-E_g/mk_BT} \qquad (3)$$

where T is the device operating temperature in kelvin, E_g is the band gap energy of silicon and k_B is Boltzmann's constant. Since n will usually take a value between 1 and 3 (depending on the exact nature of the generating mechanisms involved), the temperature dependence is dominated by the exponential term. For diffusion current the value of m will be approximately 1 and for depletion current m will be approximately 2.

The total bulk dark signal is the summation of the diffusion and depletion components. Since the activation energies of these two components are very different, the operation temperature determines which one dominates. At temperatures below ~240 K, the depletion current dominates whilst above ~300 K the diffusion current forms the dominant contribution. In between these temperatures both components are important.

To describe the temperature variation of dark signal in this intermediate region, the e2v technologies scaling relationship was developed:

$$S_B = 3.3 \times 10^6T^2e^{-9080/T} \qquad (4)$$

Note that this relationship underestimates the dark signal at both high and low temperatures, but has been found to provide a reasonable fit to measurement data in the range 240 – 300 K.

A further complication is introduced for back illuminated sensors, where the back thinning process changes the diffusion components and also adds extra back surface dark signal components.

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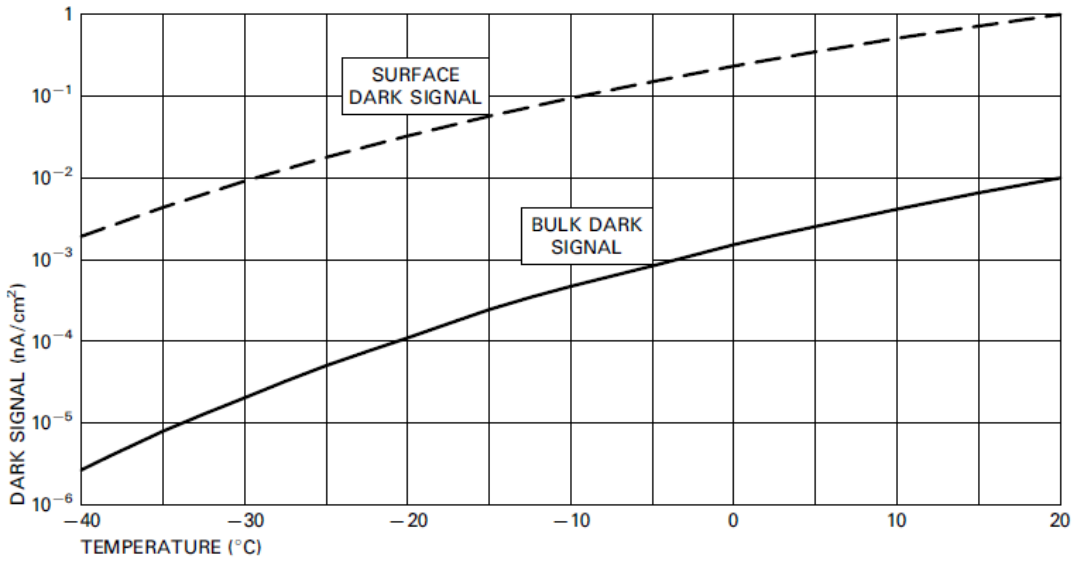

Fig. 1: Typical Bulk and Surface Components of Thermal Dark Signal versus Temperature

CLOCK-INDUCED CHARGE

Clock-induced charge (CIC) is spurious signal generated by the operation of transferring signal through the device. It is thus an integration independent contribution to the total dark signal. The CIC generated depends on a number of factors, most significantly the bias levels used, whether the device operates in inverted or non-inverted mode, and the details of the clock timings employed, as will now be discussed.

Most of the experimental and theoretical work carried out to date has concentrated on assessing the component of CIC generated by the parallel transfers, since this appears to dominate over the CIC generated in the serial register under most operating conditions.

Dependence of CIC on Applied Bias Levels

The CIC has been measured to have an exponential dependence on the clock high to substrate bias. Typical values of the CIC for different operating biases are shown in Figure 2. When the device is operated in an inverted mode (typically with image and store clock low at –5 V, and substrate at +4.5 V) a CIC of approximately 1 x 10^{-4} e^-/pixel/transfer is measured at normal clock amplitudes.

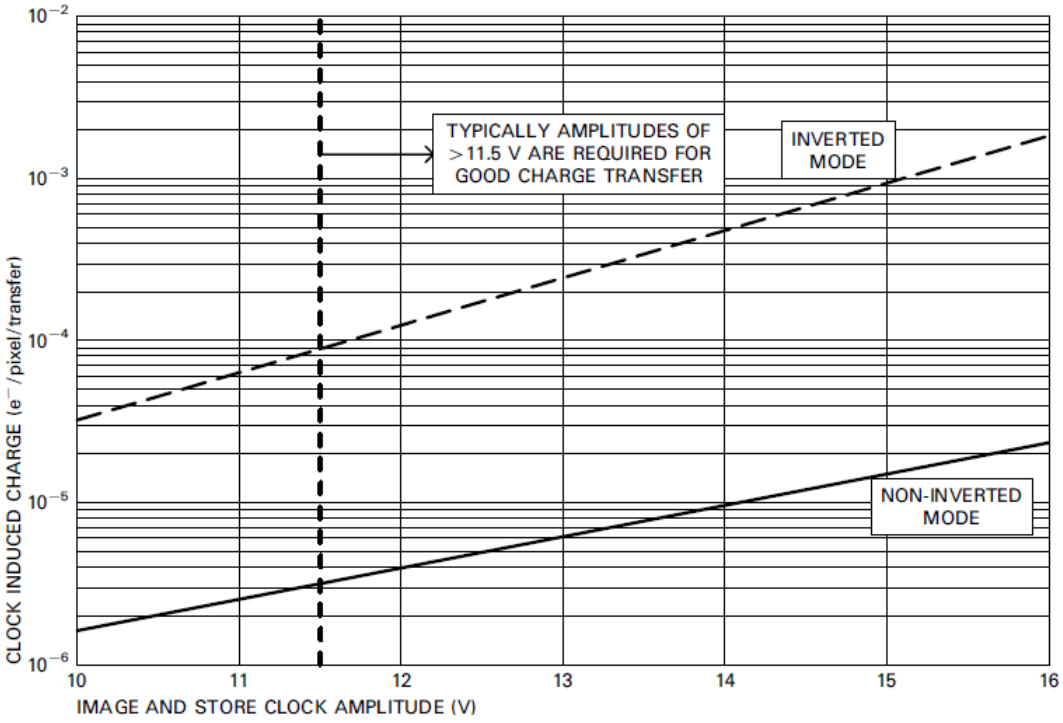

Fig. 2: Typical Measured Clock-Induced Charge for Operation of an EMCCD at –55 °C, shown for Operation in Inverted and Non- Inverted Modes. Based on Measurement Data with Parallel Transfer at 400 kHz and typical clock rise and fall times of 200 ns.

By operating the device in a non-inverted mode (typically with image and store clock low at –2 V, substrate at 0 V) the CIC reduces to approximately 3 x 10^{-6} e^-/pixel/transfer for typical clock amplitudes.

It should be noted that to operate devices in the non-inverted mode with very low CIC, it is necessary to set the substrate and parallel clock low biases to such values that the surface is completely out of inversion. Typical conditions to achieve this require that the substrate bias V_{SS} be set no more than 4 V positive relative to the image and store clock low levels.

CIC data has been presented as the number of electrons generated per pixel for each parallel transfer. Since the CIC scales linearly with the total number of parallel transfers, the total number of electrons generated per pixel per frame is given by multiplying the CIC by the total number of parallel transfers.

In the case of the CCD97 the total number of parallel transfers to read out an image is 1056, giving a total transfer generated signal of ~0.1 e^-/pixel/frame for operation in inverted mode or 0.003 e^-/pixel/frame for operation in non-inverted mode.

Whilst for the purpose of suppressing CIC it is clearly advantageous to operate the device in a non-inverted mode, this must be balanced by the fact that the thermal dark signal will be much greater because the surface component is no longer suppressed.

It should also be noted that 2-phase/inverted mode devices incorporating Shielded Anti-Bloomed (SAB) cannot be guaranteed to operate with optimum anti-blooming performance when biases are set appropriate for a non-inverted mode of operation. Users wishing to operate SAB devices in a non-inverted mode are advised to consult e2v technologies.

Dependence of CIC on Parallel Transfer Frequency

The CIC has been found to be roughly inversely proportional to the parallel transfer frequency employed. Therefore, to minimise CIC, the parallel transfer frequency should be made as large as possible. Operation is possible up to the maximum specified in the device datasheets.

Dependence of CIC on Clock Rise Times

The CIC increases as the image and store clock rising edge speeds are made faster. Therefore the clock rise and fall times should not be made too short. Typically, edge speeds of ~200 – 300 ns would be recommended to minimise the generation of CIC.

Dependence of CIC on Temperature

Figure 3 shows the inverted mode operation CIC measured with different clock amplitudes at different temperatures over the range –50 to –15 °C. Note that over this range the CIC appears to be almost independent of temperature.

The temperature dependence outside of this range is at present unknown.

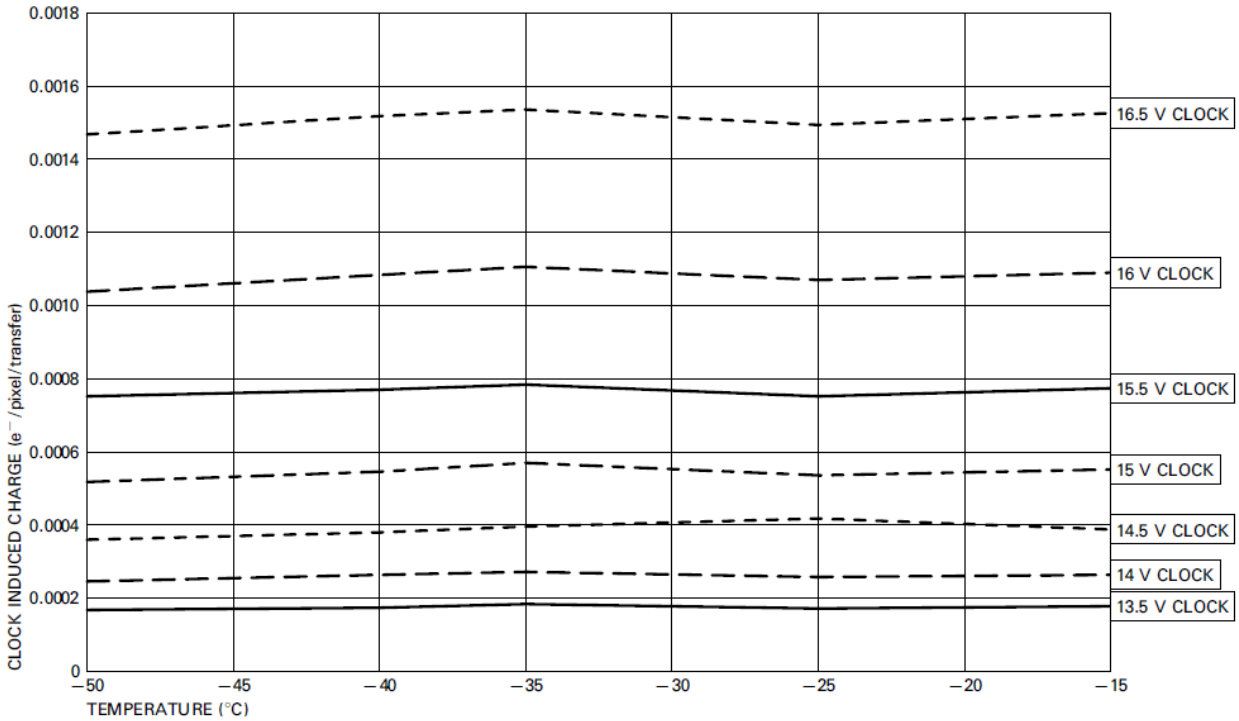

Fig. 3: Measured Variation of CIC with temperature for an EMCCD operating in Inverted Mode

DETERMINING THE OPTIMUM MODE OF OPERATION (IMO/NIMO)

Since the thermally generated dark signal is greater when operating in a non-inverted mode, whilst CIC is greater when operating in inverted mode, the optimum mode for operation (inverted or non-inverted mode) is a function of the operating temperature and the integration time being employed.

The total dark signal, D, present in an image is thus the sum of the thermal dark signal, S_D and clock-induced charge, C, i.e.:

$$D(T) = S_D(T)t + mC(T) \qquad (5)$$

where t is the integration time being used, m the total number of parallel transfers and T the operating temperature. The condition for which inverted mode and non-inverted mode give the same performance is given by:

$$S_I(T)t_0 + mC_I(T) = S_N(T)t_0 + mC_N(T) \qquad (6)$$

where S_I and S_N are the dark signal for inverted and non-inverted mode operation respectively, C_I and C_N are the CIC for inverted and non-inverted mode operation, and t0 is the integration time. Solving for t_0 then gives:

$$t_0 = \frac{mC_I(T) - mC_N(T)}{S_N(T) - S_I(T)} \qquad (7)$$

Thus, for integration times in excess of t_0, inverted mode operation is preferable, whilst for integration times less than t_0, non-inverted mode operation is optimum. In practice, non-inverted mode operation usually becomes optimum only for devices cooled to very low temperatures.

SUMMARY: OPERATING L3Vision™ DEVICES TO MINIMISE CLOCK-INDUCED CHARGE

In summary, the following principles of operation are recommended to minimise the generation of Clock-Induced Charge:

- If the operating temperature is sufficiently low, devices should be operated in non-inverted mode.
- The image and store clock amplitudes should be made as low as possible whilst still retaining adequate charge transfer performance.
- The parallel transfer frequencies should be made as large as possible, up to the maximum specified by the device datasheet.
- Clock edge rise and fall times should not be made too fast. Typically, ~200 ns gives good performance. Slower clock edges may have the additional advantage of reducing the on-chip fraction of the power dissipation.

FURTHER INFORMATION

For further information and technical support, please contact e2v technologies.

REFERENCES

1. The Use of Multiplication Gain in L3VisionTM CCD Sensors. A1A-Low-Light_TN2
2. The Noise Performance of Electron Multiplying Charge Coupled Devices