Characteristic of e2v CMOS Sensors for Astronomical Applications

Shiang-Yu Wang*[a], Hung-Hsu Ling[a], Yen-Sang Hu[a], John C. Geary[b], Stephen M. Amato[b], Jerome Pratlong[c], Andrew Pike[c], Paul Jorden[c]

[a]Institute of Astronomy and Astrophysics, Academia Sinica, P. O. Box 23-141, Taipei, Taiwan.
[b]Harvard-Smithsonian Center for Astrophysics, 60 Garden St., Cambridge MA 02138, USA
[c]e2vTechnologies, 106 Waterhouse Lane, Chelmsford, Essex, CM1 2QU, UK.

ABSTRACT

We report the testing result of e2v CIS 107 CMOS sensor for temperature from 300K to 170K. The CIS 107 sensor is a prototype device with 10 different variations of pixel designs. The sensor has 1500×2000, 7 μm pixels with 4 outputs. Each variation covers 1500×200 pixels. These are 4T pixels with high resistivity epitaxial silicon and back thinned to 11μm. At room temperature, the several variants of pixels show peak QE higher than 90%, readout noise around 5e- and dark current around 50e-/s/pix. The full well is about 15000 e- due to the limitation of the transfer gate capacitor. The CIS 107 device was further characterized at different device temperatures from 170K to 300K. The readout noise decreases and the full well increases as the device is operated at lower temperature.

Keywords: CMOS, array

1. INTRODUCTION

Traditionally, CCDs have been used as the only choice for the sensor of optical astronomical instruments. Large format CCDs provide excellent quantum efficiency (QE), low readout noise, non-detectable dark current at lower temperature. Different types of CCDs such as EMCCDs[1,2], orthogonal CCDs[3] and deep and fully depleted CCDs[4-6] were also developed to further enhance the performance for specific applications. The major caveat for large format CCDs is the slow readout time to keep the low readout noise. Especially, it is not possible to access a specific region of interests without dumping unwanted pixels unless a special design was given. On the other hand, CMOS sensors have been widely used in commercial sectors as a cost effective solution. The application of CMOS sensors in scientific research has been limited by the filling factor and QE of the devices. Hybrid visible CMOS sensor has been developed to overcome such drawback but with much higher cost. Recently, the development of monolithic CMOS sensor has shown promising performance[7]. The performance of back side illumination thinned monolithic CMOS sensors is close to what CCDs can provide.

The CMOS sensor is of an important feature to provide fast access to any region of interests on the array. This feature is attractive to the astronomical studies which require high sampling of stellar photometry such as stellar occultation and seismology studies. The authors have been working on the Transneptunian Automated Occultation Survey project (TAOS II)[8] which requires to sample about 10000 stars in the 154mm focal plane at 20Hz. Large format monolithic CMOS sensor with the capability to readout certain areas of the array is the best choice for TAOS II. With the encouraging result demonstrated so far, we decided to work with e2v to develop the large format monolithic CMOS sensor[9]. The develop work is based on the design of the internal device called CIS 107 in e2v. It is designed to include various pixels for optimizing the pixel parameters. And, the performance at room temperature was tested in e2v. In order to have a better understanding of the pixels and the required control electronics, we setup a system to run CIS 107 and test the device performance at lower temperature since the device was only measured at room temperature in e2v. In this paper, the results at different temperature are presented.

2. THE DEVICE AND TESTING SYSTEM

2.1 CIS 107

The CIS 107 imager features a pixel 2D array of 2000 rows and 1500 columns. This array is based on 10 variants of 4T type pixels. The read out circuitry is purely analogue and outputs the reference and the signal in parallel for the correlated double sampling (CDS) readout. This image sensor is designed for manufacturing on the Tower 0.18μm imaging CMOS process, with the option for low threshold voltage devices (reset, source follower and select). The periphery of the pixel array is designed with 3.3V high threshold voltage MOS devices. The sensors are back illuminated with 10μm epitaxy layer thickness. The left panel of figure 1 shows the pixel array configuration. The device is coated with e2v Multi-2 coating and delivered in an Aluminum Nitride ceramic PGA package as shown in the right panel of figure 1.
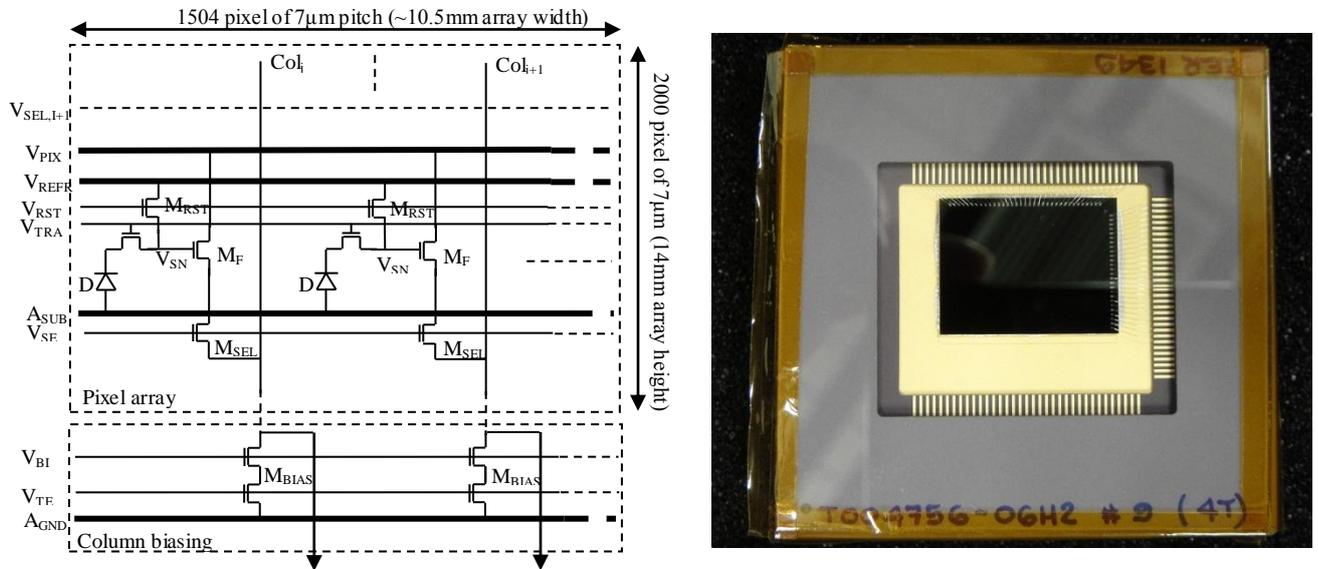

Figure 1. The pixel layout of CIS 107 (left) and the package of the delivered device (right).

As mentioned, the purpose of this device is to test the device characteristics with different design parameters. The 2000 rows are divided into 10 variants of pixels with 200 rows each. However, among the 10 variants, it shows mainly four different groups: pixel 1 (group1), pixel 2/3 (group 2), pixel 4/5/6/7 (group 3) and pixel 8/9/10 (group 4) and pixel 4 is lightly different than others in group 3. The 1504 columns are separated into four different outputs. Three different output driver circuits are used: The first output has an OTA, the second and third outputs are 5T structure and the fourth output is with a source follower. Figure 2 shows the locations of the different pixel variants and outputs.
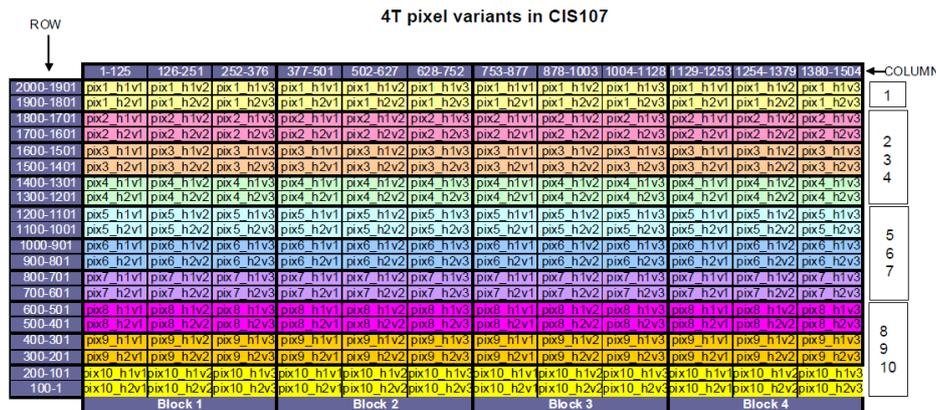

Figure 2. The format of pixel variant of CIS 107 pixels.

The device was tested at 20 degree C in e2v. The basic results were shown in Table 1. Group 2 and 3 pixels have higher charge to voltage conversion factor (CVF) to suppress the readout noise from the output transistor with the penalty of lower saturation level. Group 4 has the highest readout noise level with the lowest CVF. For the dark current, Group 1, 2 and 3 shows lower level compared with group 4 pixels. Group 2 and 3 show highest QE level which is close to the QE of CCDs. The group 1 pixels show lowest QE due to the effective filling factor of the photodiode inside the pixel. In short, pixel design for group 2 and 3 is more suitable for low flux, low noise, high sensitivity applications.

Table 1. The key parameters for different pixels of CIS 107 measured by e2v.

	Group 1	Group 2	Group 3	Group 4
CVF (μV/e$^-$)	39.8	49.6	56.3	12.1
Readout Noise (e$^-$)	7.2	4.9	5.3	18.6
Saturation level (ke$^-$)	52	12.5	16	62
QE @ 500nm	83	96	95	92
Dark current (e$^-$/s) @20C	37	36	38	61

2.2 The test facility

The CIS 107 device was tested in the cryogenic dewar with TP-14 Polycold Compact Cooler. The device can be cooled from room temperature to 160K through a cold plate on top of the ceramic package. The temperature was monitored with a temperature sensor mounted on the ceramic package and also another sensor on the cold plate as shown in figure 3. The electro-optical measurement setup includes a high power light bulb dispersed by the monochromator SP-2300i, an optical fiber for conveying light into the integrating sphere, a calibrated Si photodiode Hamamatsu S2386 mounted on one of the output port of the integrating sphere for photon monitoring. The calibrated Si photodiode was configured with a low-noise trans-impedance amplifier circuit to enhance the overall sensitivity. The ultra-low bias current operational amplifier OPA128 was used with 10MΩ resister and 5 pF capacitor on the feedback loop.

The control electronics is based on the BINOSPEC guider control electronics[10]. It consists of the preamplifiers, bias voltage and current circuit, video signal processors and a Xilinx Avnet Virtex-5 FX70 FPGA based digital circuit. The sensor is mounted on the preamplifier board inside the dewar. The bias voltages and current circuit, video signal processors and the digital circuits are outside of the dewar. The signal output and reference output signals are sampled through the differential input of the video processor. The offset, conversion gain and signal integration can be adjusted from the timing control of the FPGA or the resistors inside the circuit. The IL715 series of magnetoresistive couplers from NVE Corporation are used to isolate very high frequency internal chopping clocks with the highly sensitive analog system. During the test, the conversion gain for the video processors is set to be 50 μV/DN and the pixel rate is about 0.5MHz. The control electronics has been used with CIS 107 devices is shown in Figure 4.
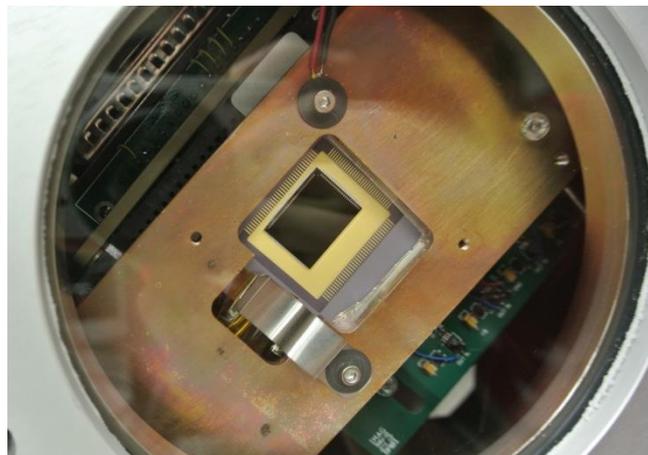

Figure 3. The CIS 107 device inside the test dewar. The copper cold plate is attached from the top with a temperature sensor on top of the picture. The device temperature is monitored by another sensor on top of the ceramic package.
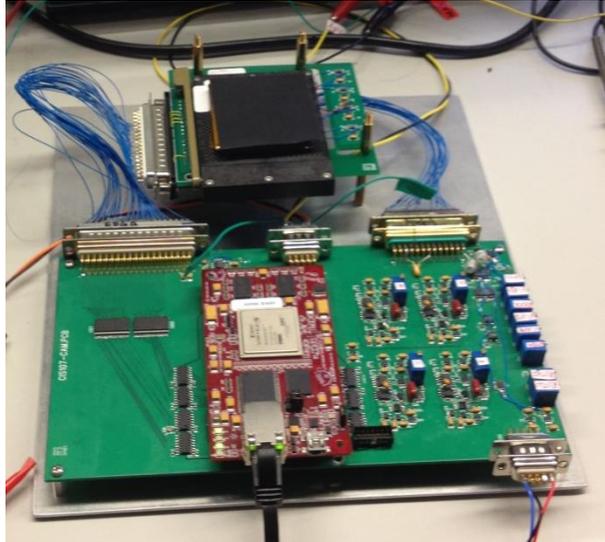
Figure 4. The control electronics used for CIS 107 tests.

3. TEST RESULTS

As the 10 variants of pixels showed roughly 4 different groups, we only discussed the difference between the 4 major groups in the following report. Figure 5a showed the CDS bias image for the CIS 107 at 170K. Although the reset reference signal had been removed by the differential output, the CDS image still shows some residual pattern that makes the bias level lower for columns at the two sides of each output block and higher at the center of the block. The difference is about 150 digital numbers (DN). It is due to the three points column bias ground return path. An I×R drop on the ground generates a voltage offset of V_{BIAS} and is shown in the image as a bump for the bias level in each output block. Such feature can be removed with a bias frame as shown in figure 5b. After the subtraction, some row pattern showed up at a level of 5 DN. This might be related to the stability of the bias voltages and currents. E2v confirmed higher row pattern can be seen for output1 and this is consistent with our result. In the analysis, all frames were subtracted with the bias frame to get the right signal level. The row pattern contributes to the readout noise estimation as we will explain in the following section.

The photon transfer method was used to get the system conversion gain (e-/DN) to correlate the digital output signal to the number of electrons in the pixel. Once the number of electrons in pixel was measured, it was then divided by the photon number that is measured by the calibrated Si photodiode to get the QE. With the system conversion gain, the CVFs of the pixels were also obtained.
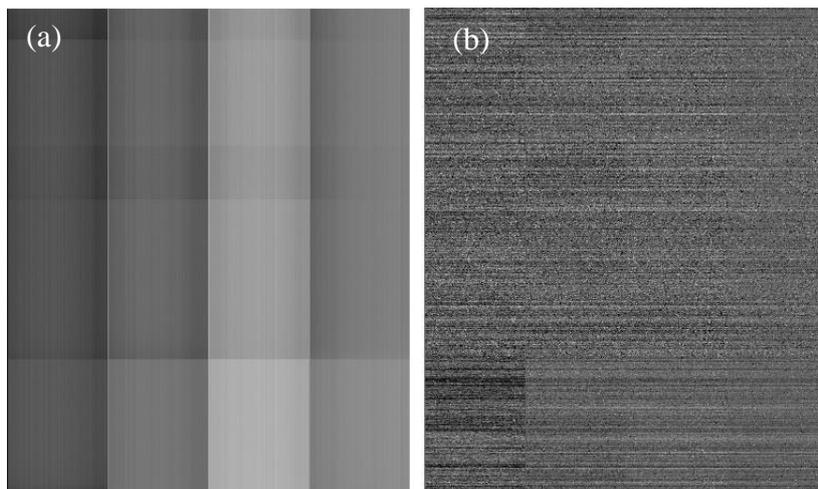
Figure 5. (a)The CDS image for 1s dark exposure of CIS 107 at 170K. (b)The subtracted frame of two CDS images.

3.1 Dark current

The dark current for CIS 107 was measured without any incoming light. Due to the limitation for the temporal control electronics, the integration time is limited to 1 minute and the measurement at 230K is not reliable due to the very small dark count. The dark frames with different integration time were taken to extract the dark current with linear fitting. The result was shown in figure 6. The decrease of the dark current follows the normal exponential relationship. Group 4 pixels show the highest dark current while the other three groups show similar dark current. This is consistent with the result from e2v from 0~20 degree C. The dark current is projected to be less than 0.1e/s/pix for group 1, 2 and 3 when the temperature is lower than 240K. Due to the higher readout noise for group 4 pixels, the measurement at lower temperature was not stable with the limited exposure time. The curve fitting for group 3 were also shown in figure 5, the dark current doubles for every 6.2K temperature change.
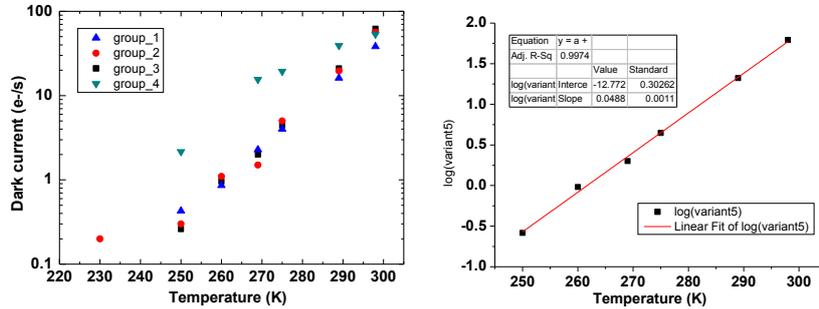

Figure 6. The dark current at different temperature for the four different groups (left) and the fitting result for group 3 pixels (right).

3.2 Readout noise

The readout noise of the device at different temperature was extracted from intercept of the photon transfer curve. The shut noise contribution from the dark current was subtracted in quadrature. The estimated noise was shown in the left panel of figure 7. The measured readout noise at room temperature is higher than the number given by e2v. As mentioned, this is due to the row pattern noise in the subtracted CDS frames. As we do not expect the row pattern noise level to change with device temperature, the trend of the decrease of readout noise with device temperature should be from the reduction of readout noise from the device itself. Furthermore, the result had been repeated for few times to confirm the variation of the row pattern did not affect the general trend. The readout noise at 170K for group 2 and 3 are lower than 5e$^-$ even with the row pattern shown in figure 5b. In order to extract the real readout noise, we removed the average row value in the subtracted frame and calculated the standard deviation again. As shown in the right panel of figure 7, the real readout noise is around 4e$^-$ when the temperature is lower than 260K for group 3 pixels. The readout noise decreases when the temperature decreases from 300K to 260K. As the room temperature readout noise shown is still higher than the value measured by e2v, there might be some error when we obtained the dark current. In any case, the noise level measured at 170K for all 4 groups are lower than the value measured by e2v at room temperature. The readout noise is 4.6, 4.0, 3.8, and 11.6 e$^-$ for group 1 to 4 respectively. The reduction of the readout noise comes from the reduction of the noise from the output transistor and also the increase of the CVF. The CVF can increase for 10% for 100 degree temperature change according to e2v. With the photon transfer curves, the CVF of different groups can be extracted. The measured CVFs are 34.4, 48.8, 56.6 and 11.4 µV/e- for group 1 to 4 respectively. It is similar to the value measured by e2v. The CVF measured at 170K is slightly higher with roughly 5% increase. For example, the CVF for group 1 device is 35.4µV/e- at 170K.
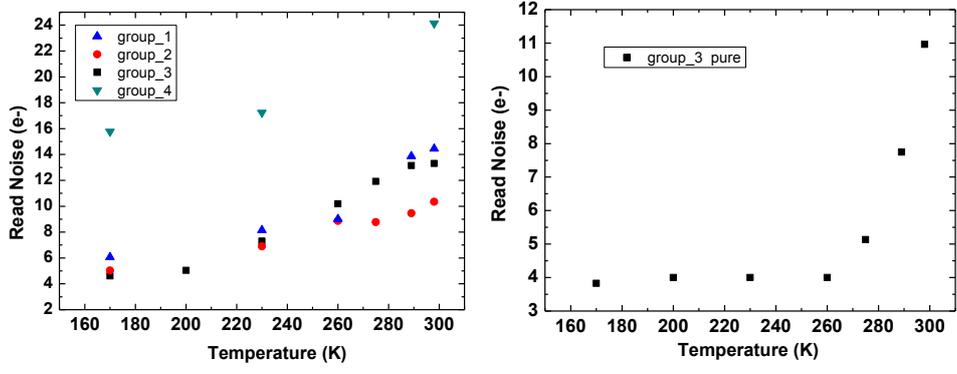
Figure 7. The readout noise at different temperature for the four different groups (left) and the readout noise after row pattern removal for group 3 pixels (right).

3.3 Full well and QE

The full well was estimated by increasing the incident light source power monitored by the photodiode at two different temperatures. Figure 8 shows the full well of group 1 pixels at 170K and 296K. The full well increases from 62ke⁻ to about 80ke⁻. This might be related to the change of the output transistors and the capacitors in the pixel structure.
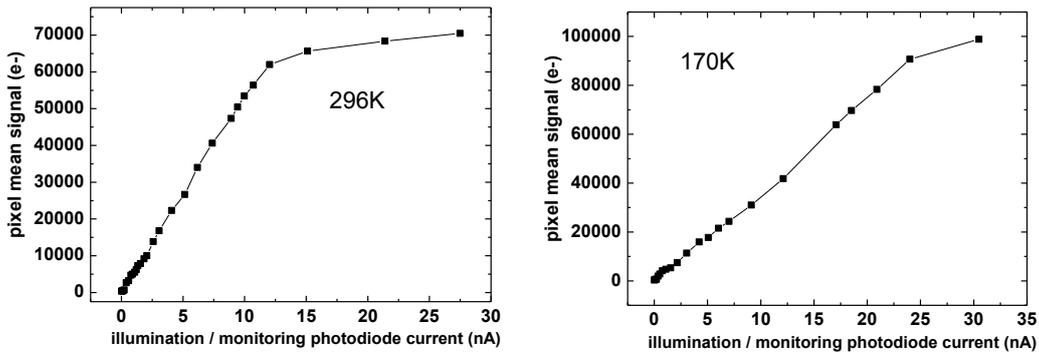

Figure 8. The pixel signal respected to the increase of incident flux monitored by a calibrated photodiode for group 1 pixel at 296K (left) and 170K (right).

The same measurement for group 2 and 3 shows different behavior. At room temperature, the slope changes around 12ke⁻ which is consistent with the saturation level measured by e2v. The signal continues to increase as the flux increases with different slop until the signal reaches about 30 ke⁻. However, for the measurement at 170K, the slop change around 12 ke⁻ disappeared and the signal continue to increase until it hits the plateau of 30 ke⁻ as shown in figure 9. The difference between group 1 to group 2/3 is that the capacitor is dominated by the sense node capacitors for group 1 but dominated by parasitic capacitors for group 2 and 3 pixels. More analysis is needed to answer the observed difference we saw. Nevertheless, the increase of full well at lower temperature is good change for any applications.
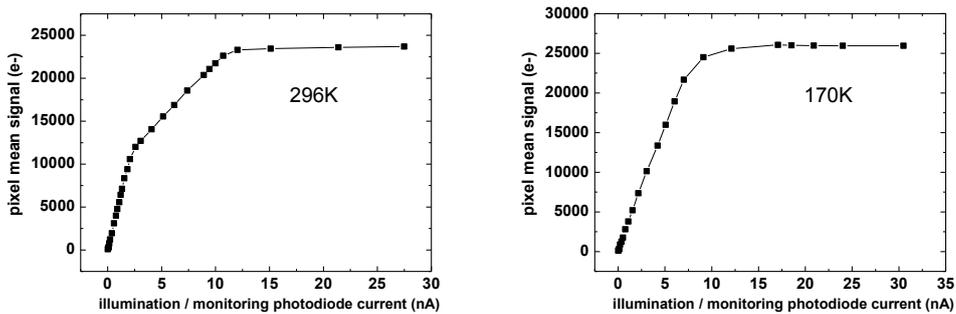
Figure 9. The pixel signal respected to the increase of incident flux monitored by a calibrated photodiode for group 2 pixel at 296K (left) and 170K (right).

To check the device QE and the bandgap change at low temperature, the QE spectrum was also calculated at 170K. The QE higher than 90% is obtained from 400nm to 600nm and then decreased monotonously to 10% at 1000nm as shown in figure 10. The high QE performance of the e2v sensor was confirmed with our measurement setup. Compared to the room temperature QE spectrum measured by e2v, the long-end corner wavelength is shorter with about 100nm, which agrees with the bandgap variation with temperature. The peak QE is higher for group 2 and 3 pixels and is slightly lower for group 1 and 4. This is also consistent with the measurement in e2v.
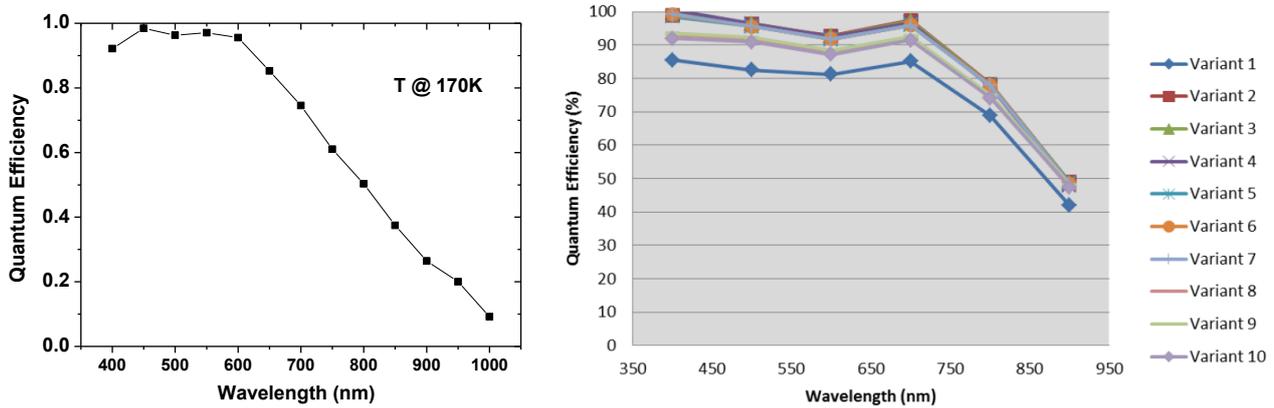

Figure 10. The measured QE for pixel group 3 at 170K (left) and the data took by e2v at room temperature (right).

4. SUMMARY

The characteristics for the e2v CIS 107 at low temperature (300~170K) were presented. Compared with the room temperature data, the dark current decreased exponentially as expected. The readout noise also decreases slightly at lower temperature. The full well increases slightly for group 1 and 4 devices but jumps dramatically for group 2 and 3 devices. At 230K, the group 2 and 3 pixels shows excellent performance with the dark current lower than $0.1e^-/s$, peak QE > 95%, readout noise ~ 4 e^- and full well ~25 ke^-. The result will provide the information for the design of future detectors. The result shows than the CIS 107 devices can be used for the prototype camera for TAOS 2 project to help on the optical quality check of the telescopes and the automation system tests.

ACKNOWLEDGEMENT

REFERENCES

[1] Denvir, D. J., Conroy, E., "Electron multiplying CCDs," Proc. SPIE, 4877, 55-68, (2003).
[2] Gach, J.-L. et al, "Development of a 4k4k EMCCD for scientific applications," SPIE 9154-4, in press (2014).
[3] Burke, B. E. and Tonry, J. L. "Recent developments with the orthogonal-transfer CCD," Proc. SPIE, 3019, 233-240, (1997).
[4] Stover, R. J. et al., "Characterization of a fully depleted CCD on high-resistivity silicon," Proc. SPIE, 3019, 183-188, (1997).
[5] Jorden, P. R., "Silicon-based image sensors," Planets, Stars, and Stellar Systems, chapter 80, Springer, (2012).
[6] Kamata, Y. et al., "Recent results of the fully-depleted back-illuminated CCD developed by Hamamatsu," Proc. SPIE, 6276, 72671U, (2006).

[7] Janesick, J. et al., "Fundamental performance differences between CMOS and CCD imagers, part IV" Proc. SPIE, 7742, 77420B-2, (2010).

[8] Lehner, M. J. et al., "The Transneptunian Automated Occultation Survey (TAOS II)," Proc. SPIE, 8444, 84440D-2 (2012).

[9] Geary, J. C., Wang, S.-Y., Lehner, M. J., Jorden, P., Fryer, M., "Wide-field photometry at 20 Hz for the TAOS II Project," Proc. SPIE, 8446, 84466C-4 (2012).

[10] Amato, S. M. and Geary, J. C. "A powerful ethernet interface module for digital camera control," Proc. SPIE, 8446, 84464M-4 (2012).