1. Introduction

This application note provides some recommendations for the correct synchronization of multiple
EV10AQ190A Quad 10-bit 1.25 Gsps ADCs.

It first presents the single ADC SYNC signal usage and then provides some recommendations with
regard to the device settings and system / board design to obtain the best performance of the device.

This document applies to the:

- EV10AQ190A Quad 10-bit 1.25 Gsps ADC
- EVX10AQ190ATPY
- EV10AQ190ACTPY
- EV10AQ190AVTPY
- EV10AQ190AVTP

This document should be read with all other applicable documentation related to this part.

The key to successful synchronization is to reset each converter into a known state and to release the
reset in a known timeslot.

The SYNC signal is used to reset the component and so this should be used in the synchronization
scheme.

SYNC resets the internal timers and it also resets the test signal generation circuitry. It should be used in
the following situations:

After power up or power configuration:- when switching the ADC from standby (full or partial) to normal
mode.

After channel mode configuration:- when switching the ADC from four-channel mode to one-channel
mode.

For entering test sequence:- when switching the ADC from normal running mode to ramp or flashing
mode. It is not needed when the ADC is switched from test mode (ramp or flashing), to normal running
mode.
The timing functionality of the SYN signal is shown in Figure 1-1. From the rising edge of SYN the Data Ready clocks return to zero and after the falling edge of SYN the Data Ready clocks start to toggle, after a fixed delay.

There is a minimum period that the SYN pulse should be active for correct operation of this function.

**Figure 1-1.** SYN Timing in 4-Channel Mode, 1:1 DMUX Mode (for each Channel)

Note: X refers to A, B, C and D.

A new functionality for the version ‘A’ of the silicon which can be selected using the Control register address 0x01 bit 10, available using SPI, will enable a SYN mode that will be timed to the falling edge of SYN and will also not stop the Data Ready signal from toggling while SYN is high.

The timing diagram for this mode (RM = 1) is shown below.
A delay $y$ can be added to extend the time of the reset, this could be used to provide a delay in the output of good data from one ADC to another in a multi-ADC system.

Note that the time from the falling edge of SYNC to the first edge of DATA READY is constant, fixed and defined. This applies for all clock frequencies greater than 1.2GHz. For the region between 1.1GHz and 1.2GHz the delay between the falling edge of SYNC and the first DATA READY edge increases by one clock cycle. For this reason it is recommended that the part be used above the clock frequency of 1.2GHz (a sample rate of 600MHz).

For correct operation, the SYNC pulse should maintain the timing constraints shown in Figure 1-3 on page 4. Failure to conform to these rules may mean that the part would not respond in time to the SYNC signal and would add a cycle to the SYNC delay. In the worst case the Data Ready clocks may not respond correctly.
Test Functions for Synchronization

The converter has two in-built functions to aid synchronization, flashing patterns and ramp pattern.

The flashing patterns produce an output of all ‘1’s for one output sample followed by a period of ‘0’s. This period can be programmed by SPI register to be 10, 11 or 15.

The flashing pattern can be used by the FPGA during a ‘training’ procedure in which delays within the FPGA are adjusted to give best performance of the interface. This procedure is explained in application notes from the major FPGA manufacturers Xilinx xapp880 Altera AN580

The other pattern produced by the converter is the ramp, this is of use during the debug stage where the output ramp can be used to confirm correct operation of the interface.

Detecting Synchronization Information in the Data.

There are a number of possible ways for the FPGA to use data from the ADC to perform synchronization.
**Trigger**

The QUAD 10bit has 4 Data ready but for the FPGA you could use only one or two Data Ready output signal, because after SYNC signal, all internal ADC are synchronous and all Data Ready output signal toggle synchronously.

One of these Data Ready output signals could be used as TRIGGER signal

**Figure 1-4.** Using the Data Ready Signal to Calibrate Delays

The Timing could be:

With a relation between X and Y: \( Y = nX \)

The system receive the TRIGGER signal coming from several ADCs and we could calculate the delay of each ADC.

Other solution is to use the Ramp test mode. In this case the FPGA of each ADC could detect the transition 1024 to 0 and FPGA would generate a TRIG signal based on this.

The ramp test is active via a SPI register, but the activation using this can’t be synchronous for all ADCs because of the timing imprecision in SPI writes

A SYNC signal should be used to be sure that all ADC are synchronous. in this case the restart of ramp signal is synchronous; and you could detect a difference of timing between several ADC.
Another solution is to generate in the input analog data a large step or over range condition which could be used to synchronize data at the FPGA.
System Diagram of Multiple ADC Synchronization.

Figure 1-6 below shows a laboratory set-up to demonstrate synchronization of two ADCs.

**Figure 1-6.** Set-up for Experimental Tests on ADC Synchronization

**Figure 1-7.** Oscilloscope Screen Shot Image
2. EV10AQ190A ADC Hardware Signals

2.1 ADC Synchronization Signal (SYNC, SYNCN)

The SYNC, SYNCN signal has LVDS electrical characteristics. It is active high and should last at least \( T_{\text{syncmin}} \) ns to work properly.

The best way to implement this interface is to use a dedicated LVDS interface – which could be using an FPGA output or a LVDS buffer.

**Figure 2-1.** SYNC Signal with LVDS Flip Flop

The Low SYNC LVDS signal coming from FPGA goes to a Flip-flop (input D and DN)

The Clock CLK1 of QUAD 10bit goes to Flip-Flops (input CLK and CLKN) but the signal is inverted

Positive clock signal goes to CLKN and negative clock signal goes to CLK

-> In this case the SYNC signal of FPGA is sampling with the falling edge of CLK Clock of QUAD 10bit and you are sure to respect the SYNC timing.

Note: if you used a LVDS flip flop, you could connect directly the output of flip flop to QUAD 10 bit.
If the FPGA generated a low speed signal and if this signal is sampling with a high speed clock (like a 2.5GHz Clock QUAD), you could have a Meta-stability phenomena. In this case, it is better to add a fast buffer or fast voltage comparator between FPGA and Flip Flop to remove this problem.

You could use the ADCMP580 fast SiGe Voltage comparators.

**Clock Driver**

For the clock, you need to have two clocks, one for the ADC and another for the Flip Flop.

In this case, a Clock buffer with fanout 2 is mandatory.

Warning: This Clock buffer needs to have a very low jitter (< 100 fs rms)

You could use ADCLK9285 of Analog Devices for create two clock CLK1 and CLK2, differential ended. For transform CLK2 in opposition of phase, you need to inverse the polarity of this clock.

**Some recommendations**

Inphy: 25717CF clock buffer fanout 2

Inphy: 25707CP Fast latch

AD: ADCMP580 Fast Voltage Comparator

AD: ADCLK925 clock buffer fanout 2
On Semi NBSGS3A or NB4L52 Data Flip Flop

SYNC Timing with external Latch

Use an external faster latch, for resynchronize the SYNC signal with falling edge of CLK, or used CLKN (inverse clock).

Note: you could use a faster Latch come from: ON Semiconductors or INPHI

**Figure 2-4.** Re-timing SYNC

Use an external faster latch, for resynchronize the SYNC signal with falling edge of CLK, or used CLKN (inverse clock).

**Figure 2-5.** SYNC After re-timing

With this configuration, SYNC_New has no problem with Setup and Hold time specification

In case you want to use the SYNC signal to synchronize several ADC and to use this signal as a TRIGGER. You could applying a pulse train to the ADC’s SYNC input without any problem

For further information and assistance please contact Hotline-BDC@e2v.com
How to reach us
Home page: www.e2v.com

Sales offices:

Europe Regional sales office
e2v ltd
106 Waterhouse Lane
Chelmsford Essex CM1 2QU
England
Tel: +44 (0)1245 493493
Fax: +44 (0)1245 492492
mailto: enquiries@e2v.com

e2v sas
16 Burospace
F-91572 Bièvres Cedex
France
Tel: +33 (0) 16019 5500
Fax: +33 (0) 16019 5529
mailto: enquiries-fr@e2v.com

e2v Aerospace and defense inc
765 Sycamore Drive
Milpitas
California 95035
USA
Tel: +33 (0) 1 408 737 0992
Fax: +33 (0) 1 408 736 8708
mailto: e2v-us.com

Americas
e2v inc
520 White Plains Road
Suite 450 Tarrytown, NY 10591
USA
Tel: +1 (914) 592 6050 or 1-800-342-5338,
Fax: +1 (914) 592-5148
mailto: enquiries-na@e2v.com

Asia Pacific
e2v ltd
11/F.,
Onfem Tower,
29 Wyndham Street,
Central, Hong Kong
Tel: +852 3679 364 8/9
Fax: +852 3583 1084
mailto: enquiries-ap@e2v.com

Product Contact:
e2v
Avenue de Rochepleine
BP 123 - 38521 Saint-Egrève Cedex
France
Tel: +33 (0)4 76 58 30 00
Hotline:
mailto: hotline-bdc@e2v.com

Whilst e2v has taken care to ensure the accuracy of the information contained herein it accepts no responsibility for the consequences of any use thereof and also reserves the right to change the specification of goods without notice. e2v accepts no liability beyond that set out in its standard conditions of sale in respect of infringement of third party patents arising from the use of tubes or other devices in accordance with information contained herein.