

## Application Note

### 1. Introduction

e2v Broadband Data Conversion products are based on differential architectures chosen to optimize the devices' noise immunity.

From the input buffers down to the output buffers, all the high speed signals are handled internally in a differential fashion but does this mean that in the case of a high speed ADC, you need to drive externally the ADC in a differential fashion also?

This document is meant to resolve all your doubts about this.

This document applies to the:

- TS83102G0B 10-bit 2 Gsps ADC
- AT84AS008 10-bit 2.2 Gsps ADC
- AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX
- AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX

### 2. Clock Input Implementation

#### 2.1 Recommended Implementation

In the case of the TS83102G0B 10-bit 2 Gsps ADC, AT84AS008 10-bit 2.2 Gsps ADC, AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX and AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX, it is recommended to drive the input clock differentially.

The differential implementation is preferred to the single-ended fashion for the following reason:

The differential input clock buffer is on-chip terminated by two  $50\Omega$  resistors connected to the die ground plane via a 40 pF capacitor (as described in [Figure 2-1](#)).

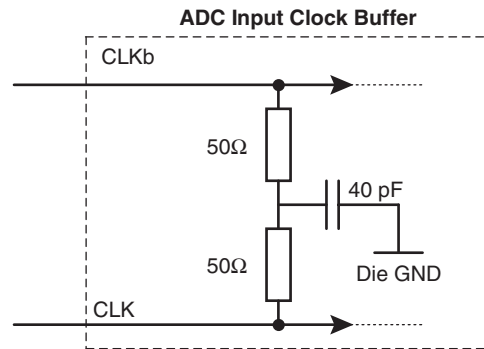
If the differential pair is used in a single-ended way (in which case, it would be necessary to terminate one signal of the pair - more likely CLKb - to ground via a  $50\Omega$  termination in order to keep the balance within the differential pair), then all the noise induced on the unused signal would affect the die ground directly and thus may degrade significantly the ADC performance.

However, this is a recommendation only. Providing a proper decoupling of the ADC power supplies to ground, the difference in performance between a differential and a single-ended use may not be significant.

Visit our website: [www.e2v.com](http://www.e2v.com)  
for the latest version of the datasheet

# Single-ended or Differential Clock and Analog Inputs?

**Figure 2-1.** Clock Input Differential Buffer



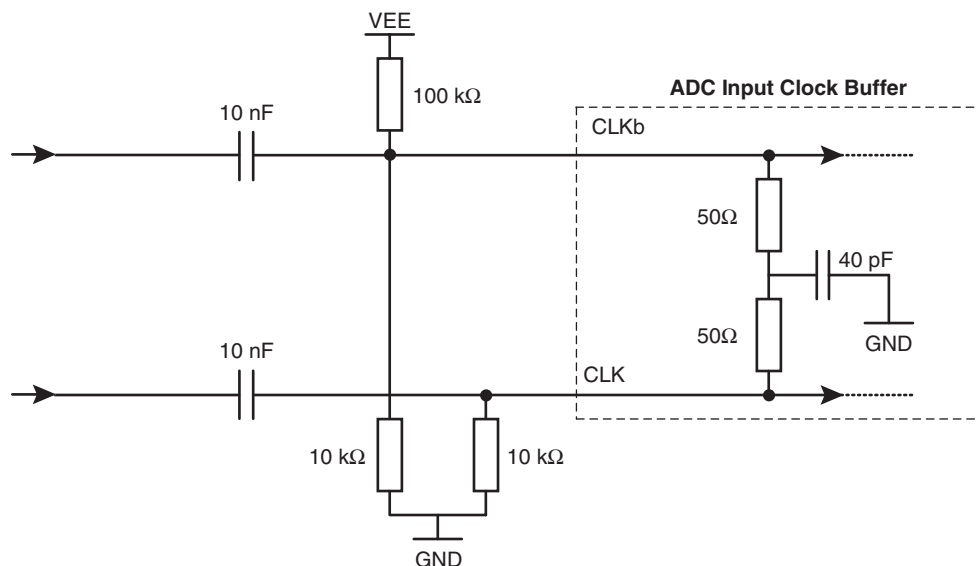
The clock inputs of the ADC have a 0V common mode and can accept signals with 1V peak maximum and -1V peak minimum.

This means that if the  $V_{IH}$  max of the signal you would like to drive the ADC clock with is higher than 1V peak or the  $V_{IL}$  min is lower than -1V peak, then you need to AC couple the input signals before applying them to the ADC: this can be done by connecting 100 pF (or 10 nF) capacitors in series with the incoming signals to the ADC. If you do so, then you need also to bias the CLK and CLKb signals as follows:

- CLK or CLKb biased to ground via a 10 k $\Omega$  resistor
- CLKb or CLK respectively biased to ground via a 10 k $\Omega$  resistor and to  $V_{EE}$  via a 100 k $\Omega$  resistor

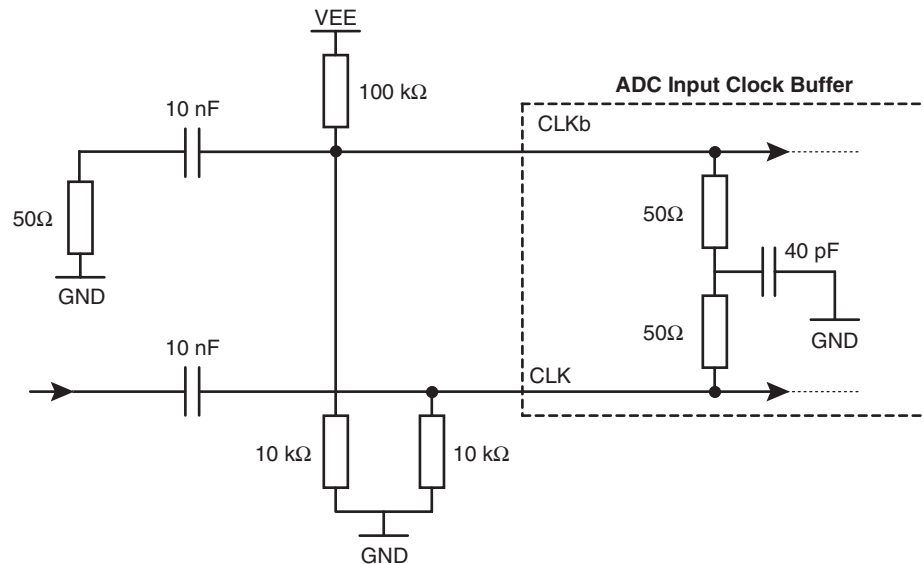
This will ensure that if no signal is applied to the differential pair, this one will not be floating but tied to a low level.

**Figure 2-2.** Recommended Clock Input AC Coupling Scheme



# Single-ended or Differential Clock and Analog Inputs?

**Figure 2-3.** Single-Ended Scheme (Allowed But Not Recommended)



## 2.2 Case of an Application Requiring a Fixed Clock Frequency

In the case of an application requiring a fixed clock frequency, it is recommended to filter the clock signal for improved jitter performance. The benefits of filtering the clock signal can be quantified to a 1 or 2 dB improvement in the SNR figure and thus in an increase of about 0.1 to 0.2 bit in the ENOB figure.

The filtering can be done using a narrow-band filter but because beyond the stop-band frequency the noise is not filtered out, it may be necessary to have a low pass filter after the narrow band filter.

**Table 2-1.** References for Filters (For Information Only)

Filter Type	Reference	Frequency
Band pass	4DF12-500/X2-MP (Lorch)	500 MHz
Band pass	4DF12-1000/X2-MP (Lorch)	1000 MHz
Band pass	6DF12-1400/X2-MP (Lorch)	1400 MHz
Low pass	4LP7-550X-MP (Lorch)	550 MHz
Low pass	5LP7-1000X-MP (Lorch)	1000 MHz
Low pass	6LP7-1800X-MP (Lorch)	1800 MHz

# Single-ended or Differential Clock and Analog Inputs?

## 2.3 Examples of High Speed Drivers (For Reference Only)

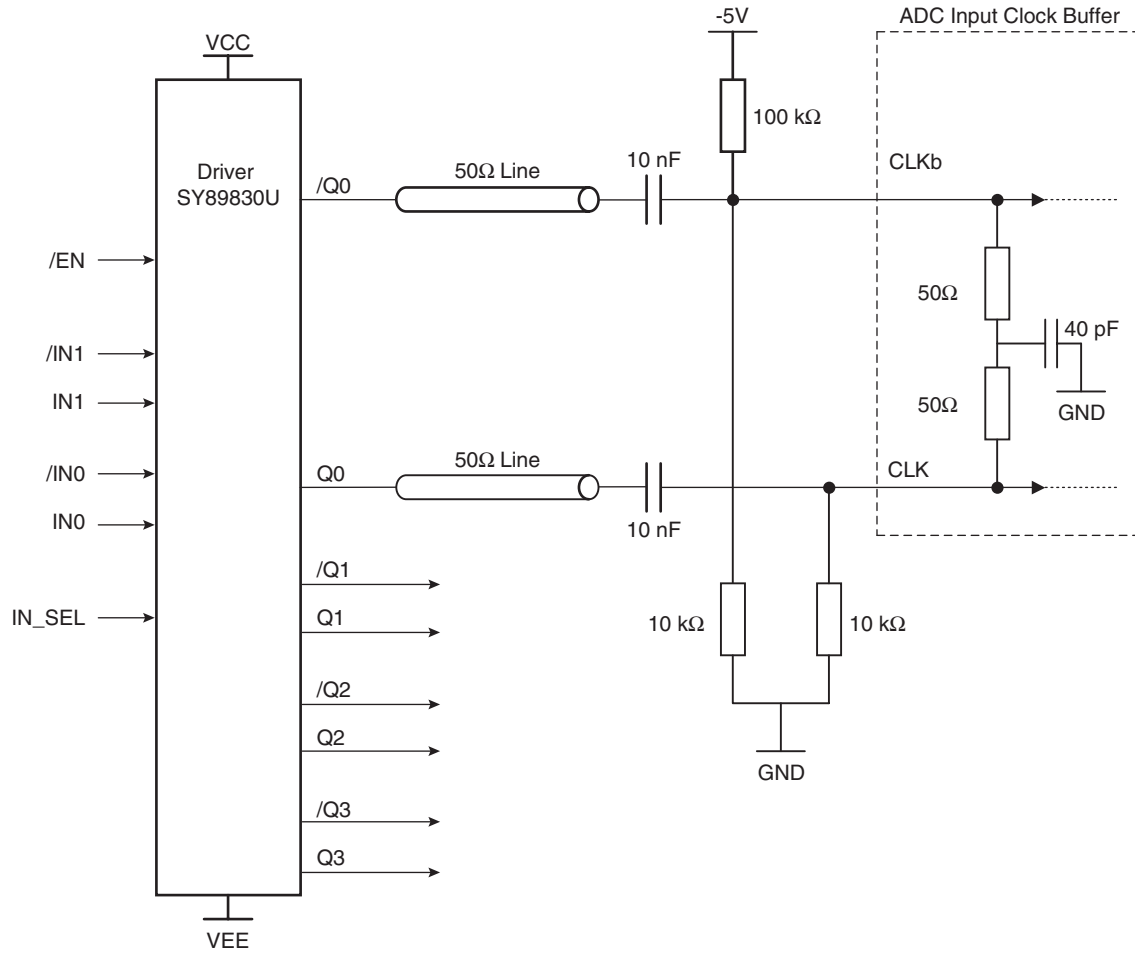
Table 2-2. Differential Buffer/Gates Examples (For Information Only)

Manufacturer	Part Number	Description	Input Compatibility	Output Compatibility	Max Frequency	Propagation Delay
On Semi-conductor	MC100LVEP14	Clock Driver	ECL/PECL/HSTL	ECL/PECL	2 GHz	400 ps
Micrel	SY898830	Clock Driver	PECL/LVPECL/ECL/HSTL	PECL	2.5 GHz	450 ps
On Semi-conductor	MC10LVEP16	Differential Driver	ECL	ECL	4 GHz	240 ps
On Semi-conductor	NB6L11	Differential Driver/translator	ECL	ECL	6 GHz	150 ps
Micrel	SY58012U	Differential Driver/translator	LVPECL/LVDS/CML	LVPECL	5 GHz	260 ps
Micrel	SY89311U	Differential Driver	PECL/LVPECL/ECL	ECL/PECL	3 GHz	300 ps
Micrel	SY8985	Differential Driver/translator	LVPECL/CML/LVDS	LVPECL	2 GHz	380 ps

# Single-ended or Differential Clock and Analog Inputs?

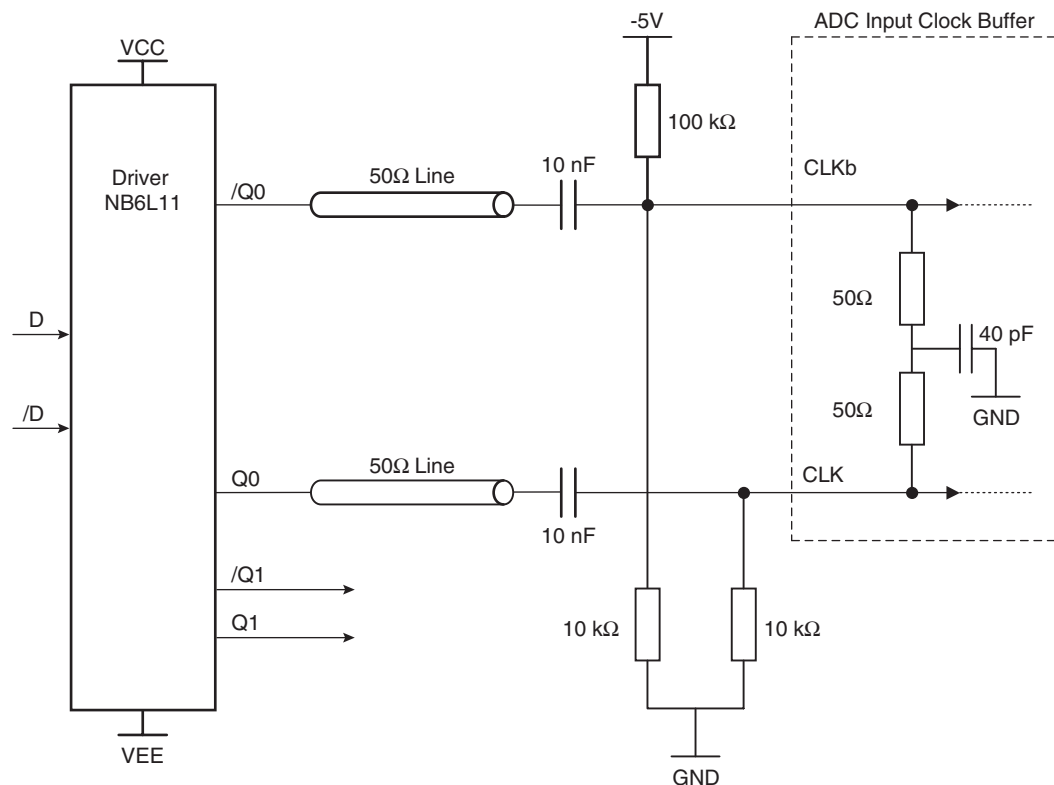
## 2.4 Practical Examples

Figure 2-4. Clock Input Implementation (Example 1)



# Single-ended or Differential Clock and Analog Inputs?

Figure 2-5. Clock Input Implementation (Example 2)



## 3. Analog Input Implementation

### 3.1 Recommended Implementation

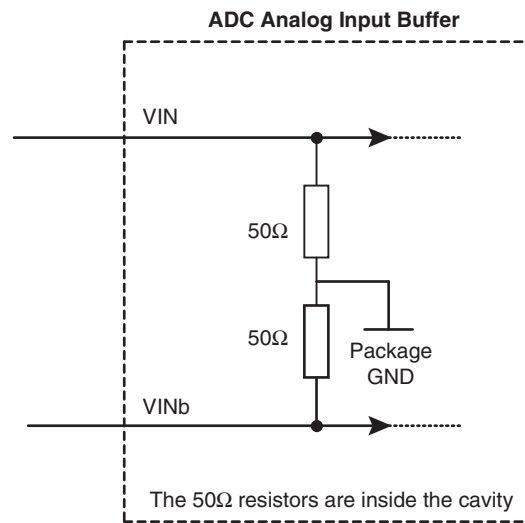
Although it is necessary to drive the input clock differentially with the TS83102G0B 10-bit 2 Gsps ADC, AT84AS008 10-bit 2.2 Gsps ADC, AT84AS003 10-bit 1.5 Gsps ADC with 1:2/4 DMUX and AT84AS004 10-bit 2 Gsps ADC with 1:2/4 DMUX, the analog input can be indifferently driven single-ended or differential.

On the contrary to the differential input clock buffer, the analog input buffer is not on-chip terminated by two 50Ω resistors connected to the die ground plane but it is terminated either inside the cavity, in which case the 50Ω resistors are connected to the package ground plane (as described in [Figure 3-1](#)), or externally via 50Ω reverse termination resistors (as described in [Figure 3-2](#)).

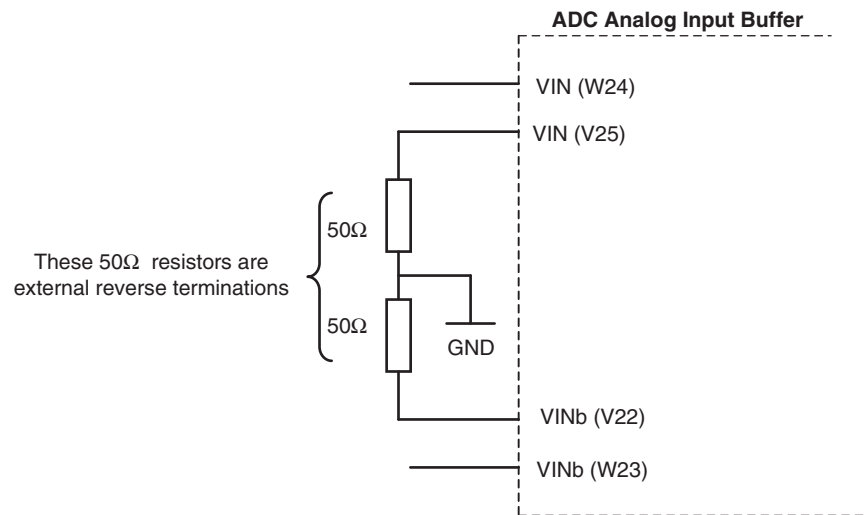
If the differential pair is used in a single-ended way (in which case, it would be necessary to terminate one signal of the pair - more likely VINb - to ground via a 50Ω termination in order to keep the balance within the differential pair), then all the noise induced on the unused signal would not affect the die ground directly.

# Single-ended or Differential Clock and Analog Inputs?

**Figure 3-1.** TS83102G0B and AT84AS008 Analog Input Buffer Schematic



**Figure 3-2.** AT84AS003 and AT84AS004 Analog Input Buffer Schematic

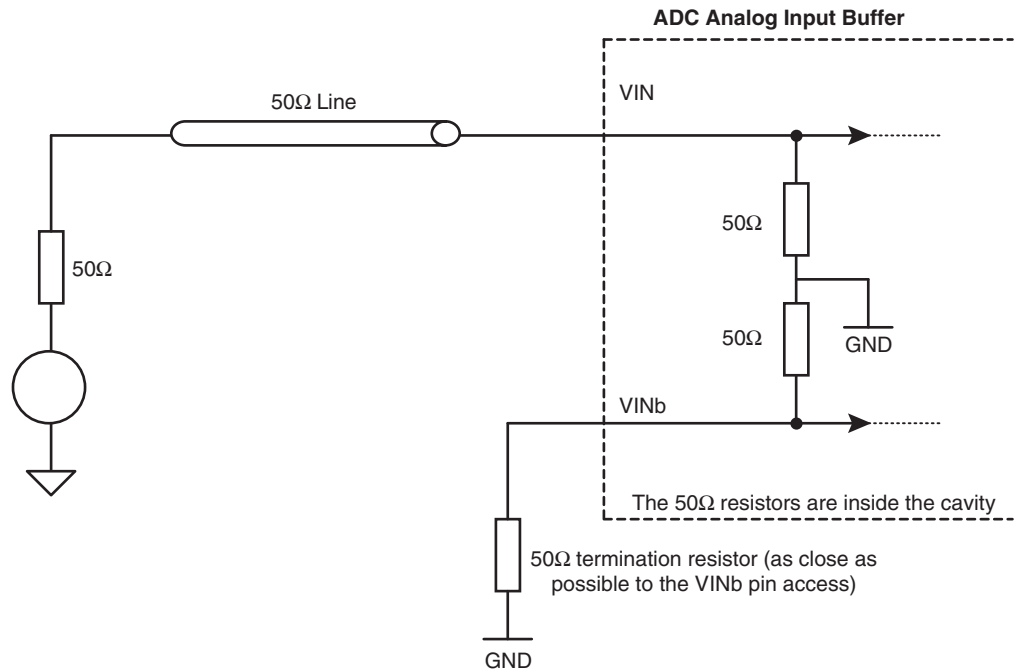


# Single-ended or Differential Clock and Analog Inputs?

## 3.2 Single-ended

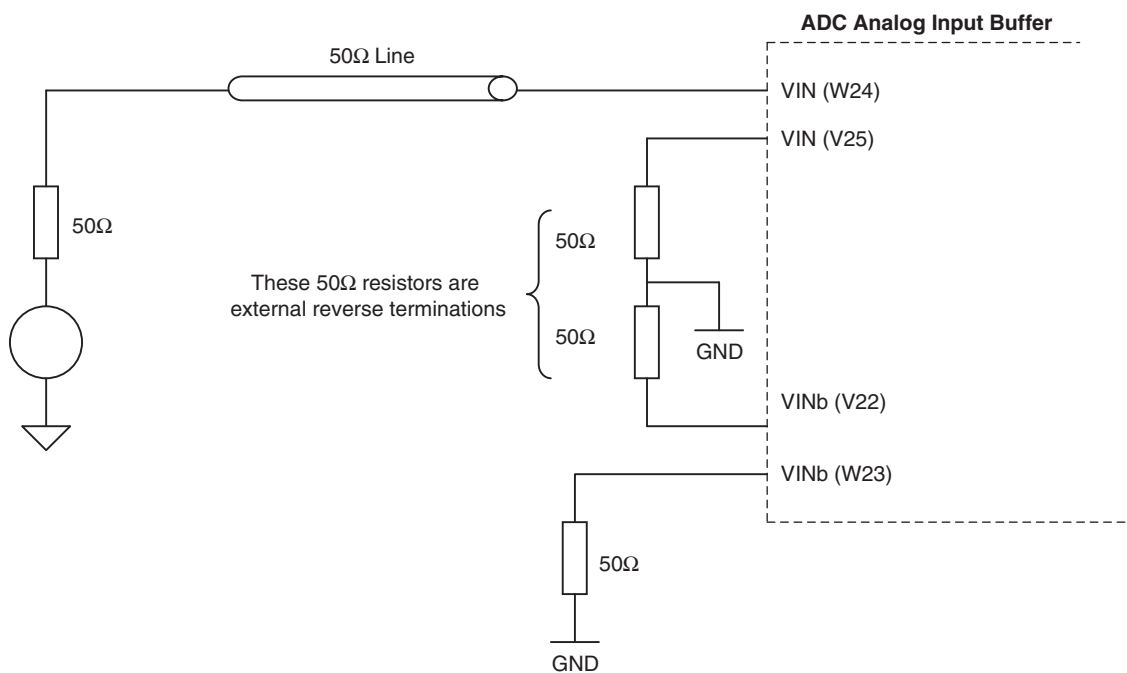
### 3.2.1 TS83102G0B, AT84AS008 Devices

Figure 3-3. TS83102G0B and AT84AS008 Analog Input Termination Scheme



### 3.2.2 AT84AS003, AT84AS004 Devices

Figure 3-4. AT84AS003 and AT84AS004 Analog Input Termination Scheme

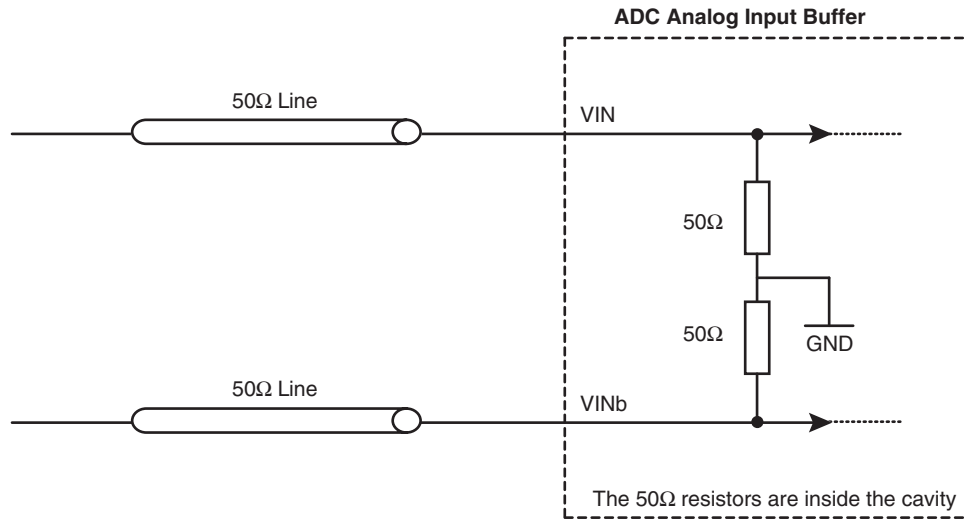




# Single-ended or Differential Clock and Analog Inputs?

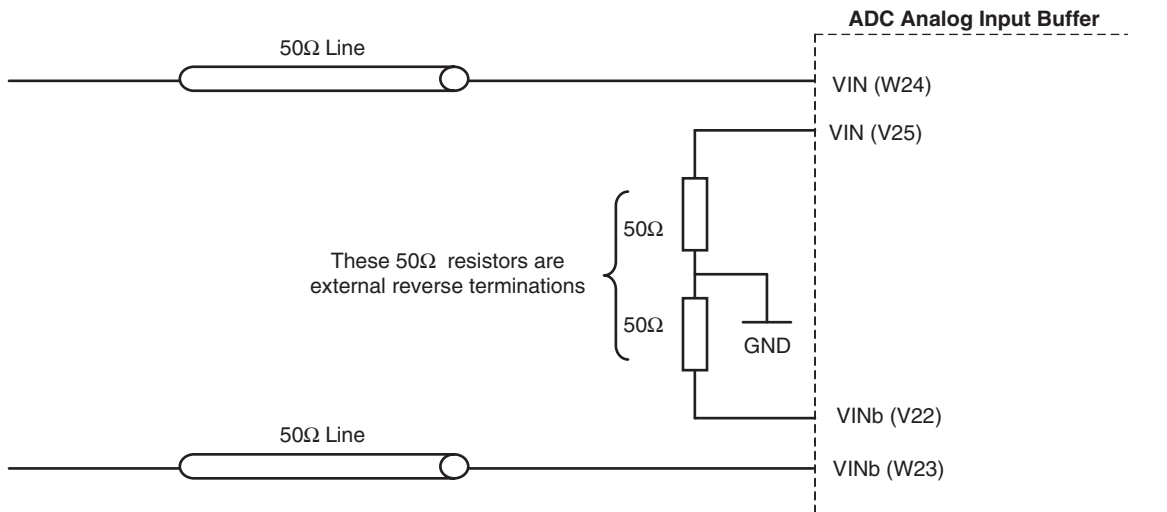
## 3.3 Differential

Figure 3-5. TS83102G0B, AT84AS008 Devices



For more information concerning the conversion from a single-ended signal to a differential signal using transformers, please refer to the "Single to Differential Conversion in High Frequency applications" Application note (Ref. 5359).

Figure 3-6. AT84AS003, AT84AS004 Devices



For more information concerning the conversion from a single-ended signal to a differential signal using transformers, please refer to the "Single to Differential Conversion in High Frequency applications" Application note (Ref. 5359).

# Single-ended or Differential Clock and Analog Inputs?

## 4. Board Layout Recommendations

There are common rules for layout of HF systems, such as the following:

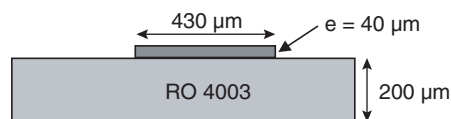
- Avoid traces with angles or too many patterns (to avoid crosstalk between traces)
- Keep all traces matched to  $50\Omega$
- Have the same length for traces corresponding to signals of the same function (clock, analog in, analog out, data in, data out)
- Avoid through hole vias for signal traces
- For differential signals, keep the True and False signal traces close to one another
- For single-ended signals, make sure that all signals are far enough from their neighbor to avoid crosstalk

In all cases, all lines should be matched to within 2 mm and the two lines of a differential pair should be matched to within 1 mm of each other.

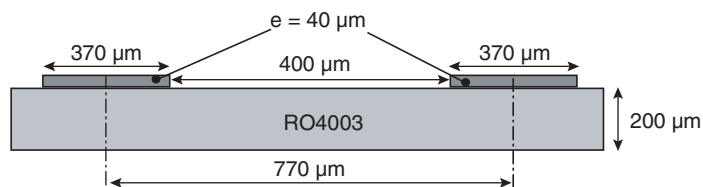
Depending on the choice made between a single-ended or a differential mode, the board layout rules are different.

Figure 4-1 and Figure 4-2 show the recommended board layout, as used for e2v converter evaluation boards. Please note that these rules depend on the PCB material used.

**Figure 4-1.**  $50\Omega$  Matched Line on R04003 Layout (Single-ended Signal)



**Figure 4-2.**  $50\Omega$  Matched Line on R04003 Layout (Differential Signal)





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