

# Recent Sensor Designs for Earth Observation

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## ABSTRACT

The large number of missions associated with ESA's Copernicus program has necessitated several new image sensor designs for earth observation (or living planet) applications as each instrument needs to be highly optimized. Whilst the majority of these sensors have utilised CCD technology, the use of CMOS is starting to increase.

New CCD designs and technology trends for hyperspectral applications such as Sentinel 4, Sentinel 5, Sentinel 5 precursor (TropOMI), Flex and 3MI are described. In these the sensor design has been optimized to provide highest possible signal levels with lowest possible noise in combination with higher frame rates and reduced image smear.

CMOS sensors for MTG (Meteosat Third Generation) and METImage are then described. Both use extremely large pixels, up to 250 $\mu$ m square, at high line rates. Radiation test data and key performance measurements are shown for MTG and for a test device that has been made for METImage. Finally, newer developments including back-illumination and means for achieving a TDI function in standard-processed CMOS are briefly described.

**Keywords:** CCD, CMOS, Hyperspectral, TDI, Dynamic range

## 1. INTRODUCTION

A Hyperspectral sensor is an area image sensor but configured as an array of many linear imaging devices each targeted at a different spectral band. The satellite scans the ground with the spectrum from a narrow slit image being spread across the imager using, for example, a diffraction grating. The row data from the device then provides spatial information and the column data provides spectral information. Wavelengths of interest generally range from the ultra-violet to near infra-red.

The challenge for Hyperspectral imaging is that there is a very large variation in intensity between the different spectral bands that may be defined across the spectral range. This causes two significant problems; firstly the detector must be able to operate with a very large range of signal intensities and secondly care must be taken to avoid cross-talk of the high intensity spectral bands with those which are less bright.

Meeting these specific requirements leads to the design of highly dedicated sensors. In recent years there has been a large expansion in the number of Earth observation (living planet) missions that have pushed image sensor design beyond the previous state of the art. This has been particularly true of sensors for ESA's Copernicus programme. The main performance parameters that have been further optimized are peak signal, frame rate, quantum efficiency and minimization of ghost images. Most of the higher-resolution Earth Observation missions such as the Sentinels still use CCD sensors as a key requirement is very high dynamic range. However, the atmospheric image sensors that need to operate at very high line rates (MTG and METImage) are using CMOS technology which has a poorer dynamic range than CCD but can operate at much higher line rates with little or no performance degradation.

## 2. TECHNOLOGY DEVELOPMENT

### 2.1 Dynamic Range

For many earth observation missions such as Sentinel 4 or Sentinel 5, dynamic range is one of the most critical parameters and these projects have necessitated a significant development in our capability. Dynamic range is improved by both increasing the peak signal and decreasing the sensor noise floor, but unfortunately the parameters are linked and there are limitations to what can be achieved.

#### 2.1.1 Peak signal

The CCD peak signal is primarily determined by the charge storage capacity of the pixel. This is determined by the area within the pixel available for storage and the maximum storage density just before signal charge fills the buried channel and starts to come in contact with traps at the silicon/silicon dioxide interface –the so called “buried channel limit”.

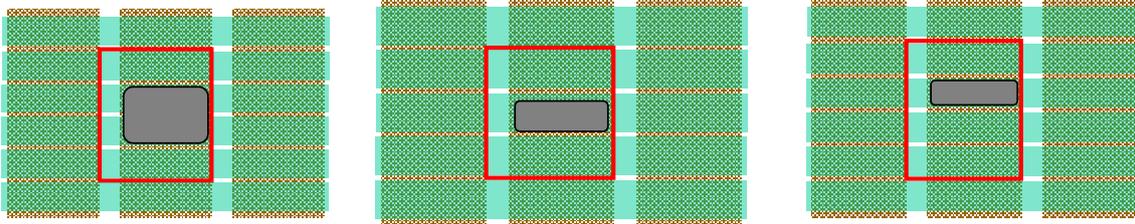


Figure 1: 4-phase, 3-phase and 2-phase charge storage areas

Since charge can be stored and transferred under two adjacent electrodes in a four-phase pixel, the storage area  $A_S$  is generally higher than in an equivalent three-phase pixel, as may be seen in figure 1. Two-phase technology has somewhat lower capacity, typically half that of four-phase.

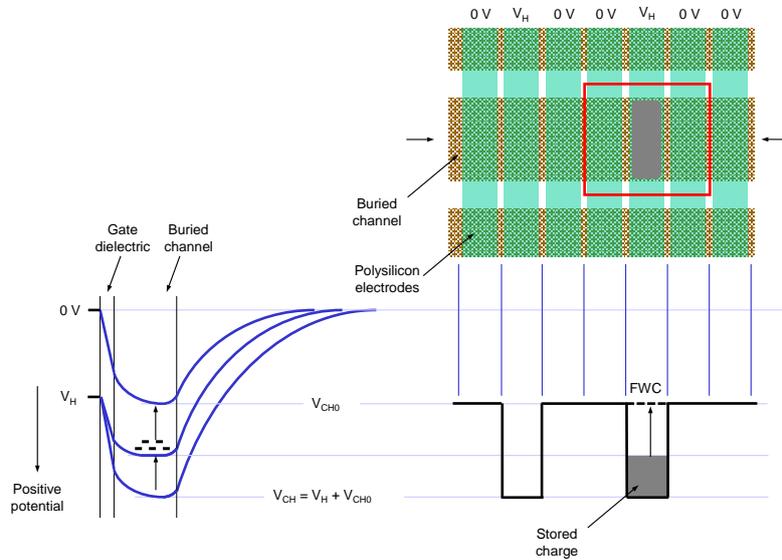


Figure 2: Channel potentials

The potential distribution beneath an electrode can be determined using the classic depletion layer approximation and the results are as shown schematically in figure 2 for an electrode at 0V, and one at clock-high level  $V_H$  with and without stored charge. If the buried channel has a total dose per unit area of  $N_{CH}/\text{cm}^2$ , comprising a uniform n-type doping of  $N_D/\text{cm}^3$  and thickness  $t_{CH}$ , and the gate dielectric has capacitance  $C_O$ , assuming the underlying p-type substrate doping  $N_A/\text{cm}^3$  is very much less than  $N_D$ , then:

$$V_{CH0} = qN_{CH}[(1/C_O) + (t_{CH}/2\epsilon_0\epsilon_s)] - V_{FB} \quad \text{and} \quad V_{CH} = V_H + V_{CH0}$$

Where  $q$  is the electron charge,  $\epsilon_0\epsilon_s$  is the dielectric constant of silicon and  $V_{FB}$  is the “flat-band voltage” related to the inherent positive charge in the dielectric. If the stored charge has a density equal to a fraction  $\beta$  of the total channel dose (i.e. stored charge per unit area =  $\beta N_{CH}$  electrons/cm<sup>2</sup>), then the minimum clock level required for transfer is given by:

$$V_H(\min) = q\beta N_{CH}(1 - \beta)[(1/C_O) + (t_{CH}/2\epsilon_0\epsilon_s)(2 - \beta)]$$

This equation is derived by equating the channel potential under the biased electrode with stored charge to that under the 0V electrode, as may be seen in figure 2. The total stored charge per pixel is then  $A_S\beta N_{CH}$  electrons.

By simulation and practical measurements it is found that the buried channel limit is reached at typically  $\beta \sim 0.8$ . With standard process values for  $N_{CH}$ ,  $C_O$  and  $t_{CH}$ ,  $V_H(\min) \sim 10V$  the following is obtained:

$$\text{Full-well capacity (FWC)} \sim 0.8A_S N_{CH} \text{ electrons}$$

As a first improvement the thickness of the gate dielectric can be halved, doubling  $C_O$ , and this allows  $V_H(\min)$  to be reduced to about 7V whilst maintaining the same storage capacity. This is useful to minimize the clocked power dissipation which varies as the pulse amplitude squared. The revised process is designated “thin gate”. It is then possible to also increase the buried channel dose such that  $V_H(\min)$  returns to the 10V standard value. This is designated our ‘thin gate plus’ process. Since the maximum storage density is still a fraction  $\beta \sim 0.8$  of the channel dose, the storage capacity is about 40% higher than the other processes. Even higher values could be possible with adjustment of  $N_{CH}$  and  $C_O$ , but this has not yet been attempted.

An added advantage of the reduced dielectric thickness is that the change of flat-band voltage due to radiation-induced positive charge build-up is also reduced to about a quarter of that experienced with standard devices<sup>1</sup>.

### 2.1.2 Output circuit limitations

The standard CCD output circuit comprises an output gate at fixed bias  $V_{OG}$ , a detection node of capacitance  $C_N$  with a reset switch transistor and one or more source-follower amplifiers, as shown in figure 3. The node is reset to the reference voltage  $V_{RD}$  by a pulse  $\emptyset R$  applied to the gate of the reset transistor. A charge signal of  $N_S$  electrons transferred to the node then causes a voltage change of  $V_{SN} = qN_S/C_N$ , which is present at the output buffered by the amplifier of voltage gain  $G_O$  to give the final output signal  $V_{SO} = G_O qN_S/C_N$ . The overall “responsivity” or “charge-to-voltage conversion factor” (CVF) is therefore  $G_O q/C_N$  volts/electron. The node is then reset again for the next charge signal to be detected. The output gate ensures that charge transfers to the node and not back down the register.

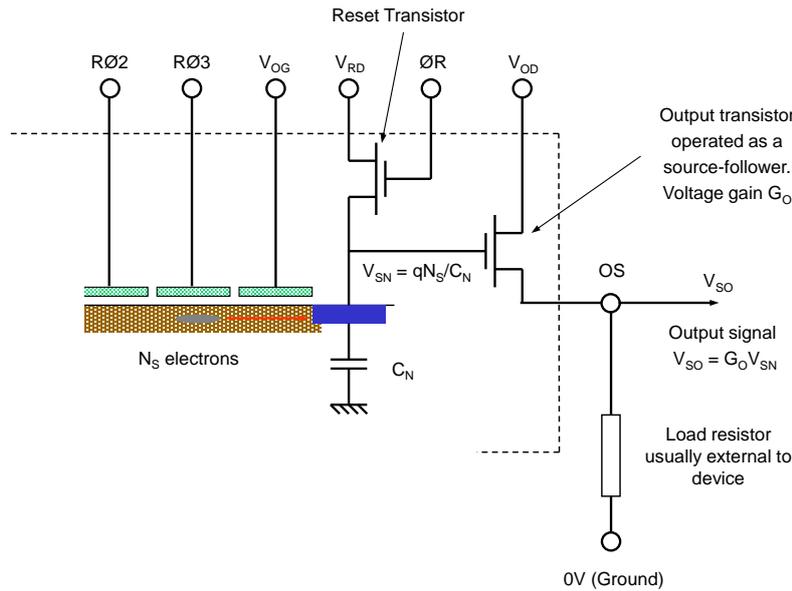


Figure 3: CCD Output Circuit Schematic

A first requirement for reliable resetting is that:

$$\varnothing R_H + V_{CHO} \geq V_{RD} + V_{ON}$$

Where  $\varnothing R_H$  is the high level of the reset pulse and  $V_{ON}$  is the effective voltage above threshold needed to form a conducting channel in the transistor.

The maximum voltage swing at the node  $V_{SN}(\max)$  before charge spills back over the output gate is given by:

$$V_{RD} - V_{OG} - V_{CHO} - 1V \geq V_{SN}(\max)$$

Where the extra margin of 1V is included to allow for factors such as reset pulse feed-through.

Then, with typical values  $\varnothing R_H = 10V$ ,  $V_{CHO} = 11V$  and  $V_{ON} = 3V$ ,  $V_{RD}$  has a maximum value of 18V and 17V is generally used. Since  $V_{OG}$  is typically 2V, this leads to  $V_{SN}(\max) = 3V$ . The drain voltage of the output source followers  $V_{OD}$  is generally set at about  $V_{OD} = V_{RD} + V_{CHO}$  as this is found to provide lowest noise.

The maximum charge handling capacity of the output circuit is then:

$$N_O(\max) = V_{SN}(\max) \times C_N/q \sim 3C_N/q \text{ electrons.}$$

Clearly, this needs to be larger than the pixel full-well capacity so as not to be a limit to performance. An obvious consequence is that the value for  $C_N$  must be sufficiently large, and this has a consequence for the noise performance.

A higher signal swing  $V_{SN}(\max)$  can be achieved by increasing  $\varnothing R$  and  $V_{RD}$ , with a corresponding increase in  $V_{OD}$ . If the resulting value for  $V_{OD}$  becomes too high for system requirements, then it is possible to fabricate the source-follower transistors with a somewhat reduced channel dose to decrease their value for  $V_{CHO}$  and avoid this increase.

### 2.1.3 Output circuit noise

Assuming the use of correlated double sampling in the external electronics, the output circuit can be expected to have a minimum noise (expressed as noise equivalent electrons) for back-illuminated sensors given by

$$\text{Minimum NES} \sim \frac{1}{2}\sqrt{[C_N(2 + f_B/f_O)]} \text{ electrons rms}$$

$C_N$  is the value of the node capacitance in fF,  $f_B$  is the system bandwidth and  $f_O$  is a constant equal to about 150 kHz (actually the 1/f “corner” frequency). The minimum external pre-sampling bandwidth which defines  $f_B$  is normally assumed to be twice the read-out rate  $f_R$  as this is found to be about the minimum possible for reliable sampling to be carried out. If a higher bandwidth is used to improve the settling performance, then this will result in proportionally higher noise.

Achieving this performance is found to be reasonably straight-forward in practice using reasonably efficient electronics.

The value for  $C_N$  is essentially defined by the requirement  $N_O(\max) \geq FWC$ , and the noise performance is thus defined.

### 2.1.4 Dummy outputs

Devices can be designed with additional “dummy” outputs. These are of the same design as the main or “real” amplifier but receive no signal charge. These give the option of suppressing common unwanted feedthrough, e.g. reset, by means of a differential output in the external electronics. The penalty is that the amplifier noise is increased by a factor  $\sqrt{2}$ .

## 2.2 Frame rate

The speed of parallel transfer is generally limited by the parasitic resistance and capacitance of the electrodes, which give an RC time constant that slows the applied pulse edge speeds on propagation across the array. The capacitance components are largely intrinsic to the structure and cannot be reduced. As a rough guide the maximum transfer rate is equal to  $1/W^2$  MHz, where  $W$  is the device width in cm. The only prospect for faster operation is to reduce the resistances, and this can be achieved using overlaid metal connections, a technique often described as “buttressing”.

### 2.2.1 Metal buttressing

There are essentially two basic approaches for metallising the electrodes. A first uses a metal track running horizontally across the width of the electrode, but there are complications in making connections at the sides of a three-phase array, as

shown schematically in figure 4a. One phase ( $\phi_3$ ) cannot join with the metal of the bus lines running down the side of the array, meaning that this will have somewhat higher series resistance. A special arrangement is possible with two-phase pixels giving low resistance connections with only a single level of metallisation, as shown in figure 4b. One phase is connected on one side of the image section, the second phase on the other.

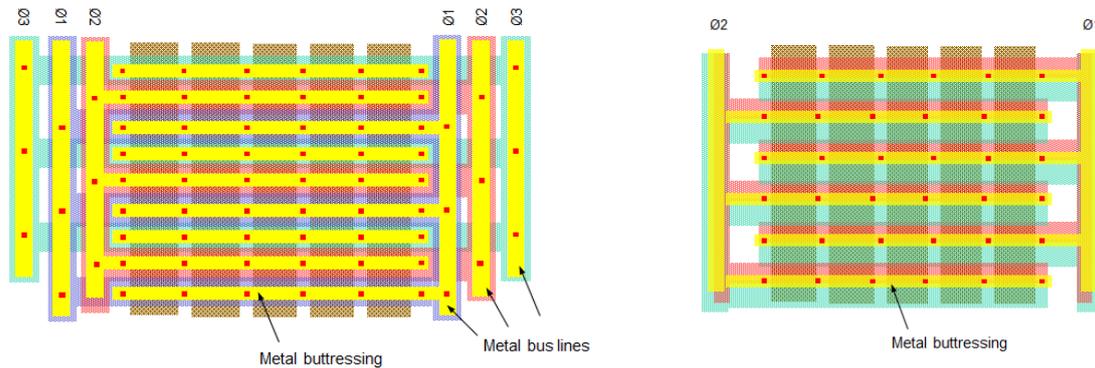


Figure 4: Metal bussing a) 3-phase (left), b) 2-phase (right)

The second approach uses vertical tracks, generally one per column, as shown schematically below. With only a single level of metal the connections require either multiple bond pads with in-package tracking to give a single pin per phase, or on-chip polysilicon under-passes to reduce to fewer bond pads but giving increased series resistance. The solution is to use a second level of metal to form the bus connections, as shown in figure 5, but such technology has only recently been developed at e2v for a production capability and none of the devices to be described use it.

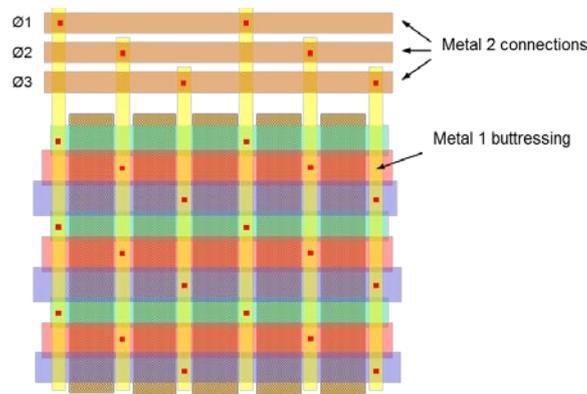


Figure 5: Metal bussing with second level metal

Clearly, once metal bussing is employed, there is a large decrease in front-face quantum efficiency and back-illumination is essential.

### 2.2.2 Effects of lead inductance

A practical difficulty with utilising devices having metallised electrodes is that the intrinsic inductance of the leads forms a tuned circuit with the capacitive component and the series resistance may now be insufficient to damp out oscillations, with the result that severe overshoot and/or ringing may be experienced when applying drive pulses to the device. Any drive system may need to have additional series resistance to damp out the effect of the series inductance and the speed as calculated from the on-chip resistance and capacitance components may not be fully achieved in practice.

## 2.3 CMOS dynamic range

The limitations on the available dynamic range are similar to those found for the output circuit of the CCD.

### 2.3.1 3T pixel

In the case of the three transistor pixel (3T), as shown schematically in figure 6, the signal charge is generated in the photodiode and collected on the associated capacitance  $C_D$ .

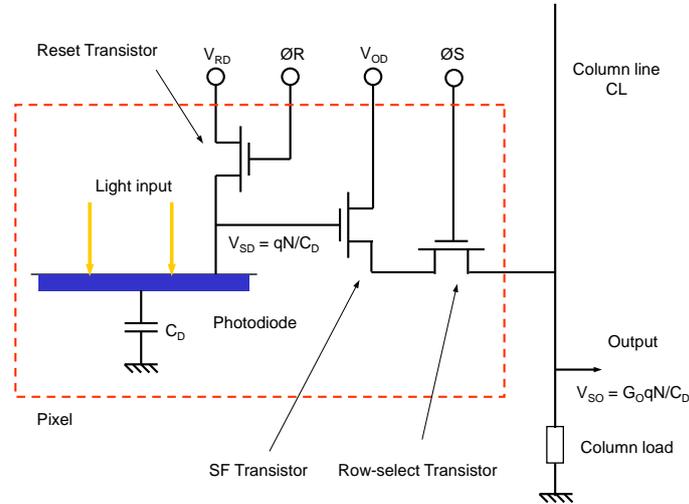


Figure 6: Three transistor pixel

The peak signal capability  $N_O$  is determined by the maximum voltage swing which for 3.3V CMOS is  $\sim 2V$ . Thus:

$$N_O (\text{max}) = V_{SD} (\text{max}) \times C_D / q \sim 2C_D / q \text{ electrons}$$

Since correlated double sampling is not practicable, the minimum noise is that arising from resetting the voltage on  $C_D$  of a magnitude given by:

$$NES = (1/q) \sqrt{kTC_D} \text{ electrons rms}$$

Where  $k$  is Boltzmann's constant and  $T$  is absolute temperature.

The dynamic range is therefore directly dependent on  $C_D$ .

$$\text{Dynamic range} = N_O (\text{max}) / NES \sim 2 \sqrt{C_D / kT} \sim 1000 \sqrt{C_D}, \text{ where } C_D \text{ is in units of fF.}$$

Achieving higher dynamic range is therefore at the expense of higher noise.

### 2.3.2 4T pixel

In the case of the four transistor pixel (4T), as shown schematically in figure 7, the signal charge is generated in the photodiode and transferred to the adjacent detection node  $C_N$  under control of the transfer gate, much in the same way as the CCD. Generally, however, the maximum signal swing is now about 1V, but higher values can sometimes be achieved, possibly with reduced linearity and/or lag. The peak signal is therefore given by:

$$N_O (\text{max}) = V_{SN} (\text{max}) \times C_N / q \sim C_N / q \text{ electrons}$$

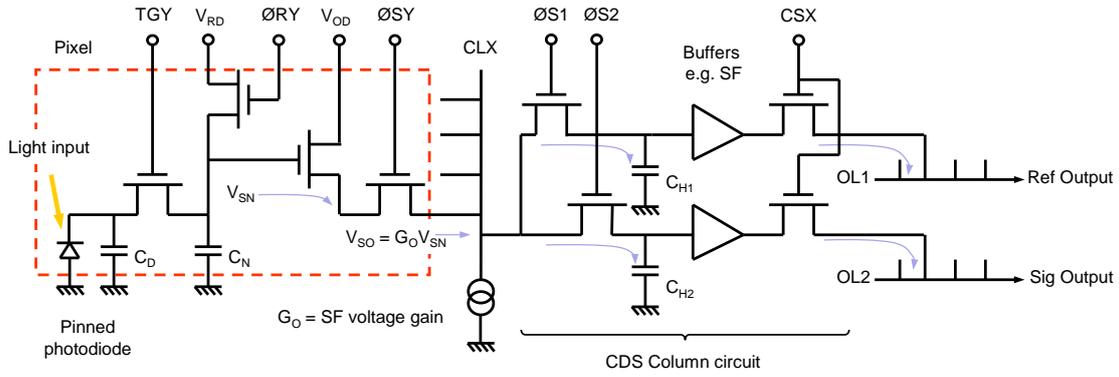


Figure 7: Four transistor pixel and read-out circuitry

Correlated double sampling is possible by measuring the output level after resetting and then again after signal transfer. Many devices have means to store these samples on-chip for subsequent read-out on two output lines such that a difference signal is easily achieved off-chip using a differential amplifier. A common method is to use sample-and-hold circuits and follower amplifiers, as shown schematically in figure 7. Each column has such circuitry and the sampling is done in parallel prior to sequential signal read-out along the line. This gives an important advantage of CMOS over CCD in that the pre-sampling bandwidth  $f_B$  can be set at a relatively low frequency to give low floor-value noise, as there is generally sufficient time for the long settling time such bandwidth requires. The noise is thus at a fixed value, and the subsequent read-out can be at any rate without influencing this value. With CCD the bandwidth must increase with the read-out rate  $f_R$  and faster operation is accompanied by higher noise.

The minimum noise with correlated double sampling can again be expressed (with  $C_N$  in units of fF)

$$\text{Minimum NES} \sim \frac{1}{2} \sqrt{[C_N(25 + f_B/f_O)]} \quad \text{electrons rms}$$

The first factor in the bracket is higher than with CCD because the source-follower transistors are typically surface channel, rather than buried channel. Since it is now possible for  $f_B \ll f_O$ , the noise can be the floor-value given by:

$$\text{Typical NES} \sim \sqrt{[5C_N/2]} \quad \text{electrons rms}$$

Note, however, that this assumes that the  $kT/C$  noise from the subsequent capacitor sampling and the amplifiers can be made sufficiently small not to contribute to the total. It appears that in many cases this is not possible and the noise is higher than the minimum.

The dynamic range is therefore again directly dependent on  $C_N$  (expressed here in units of fF).

$$\text{Dynamic range} = (C_N \times 10^{-15}/q) / \sqrt{(2.5C_N)} \sim 4000 \sqrt{C_N}.$$

For a given value of  $C_N$  the dynamic range is higher than with a 3T pixel. Increasing the dynamic range requires a larger value for  $C_N$  and hence higher noise. There are, however, circuit techniques by which this basic limitation can be exceeded. For example, the pixel can be provided with a non-linear detection node. The node is primarily designed to provide a small  $C_N$  for low noise but, as the quantity of stored charge increases and the node voltage decreases, it is possible to include a circuit that automatically adds additional capacitance below a certain voltage level to thereby reduce the CVF and accommodate peak signals higher than would be possible with  $C_N$  alone. It is also possible to provide circuitry for the response to become logarithmic at higher signal levels. In all such cases re-linearization can usually be provided in the external signal processing electronics.

## 2.4 Quantum efficiency

All the new CCD sensors to be described are back-illuminated types and, to achieve high quantum efficiency, there is a need for a back-surface anti-reflection coating. Standard manufacture uses a single-layer coating which provides maximum efficiency at the wavelength  $\lambda$  for which its thickness is  $\lambda/4$ . In the case of hyperspectral devices, where the

light input has a known variation of wavelength across the sensor, a technique has been developed to accordingly vary the thickness of the layer, i.e. a “wedge” coating, to give high quantum efficiency over the full wavelength range.

Coatings with more than one refractive index layer can give a much broader response, i.e. not peaked at  $\lambda/4$ . One such coating designated “astro multi-2” has been developed at e2v and is being used for conventional products. This or a similar coating could be used for future hyperspectral devices to avoid the need for specialized wedge coatings.

### 3. NEW SENSORS DEVELOPED

Details of various new sensors are now described

#### 3.1 TropOMI (CCD275)

The Tropospheric Ozone Monitoring Instrument (TropOMI) aims to bridge the gap between the current Envisat and the future Sentinel 5. For this the CCD275 comprises a back-illuminated frame-transfer sensor with a split read-out register, each register half having output amplifiers at either end. An outline chip schematic is shown in figure 8. The image section comprises 1024 rows on 26  $\mu\text{m}$  pitch by 1024 columns also on 26  $\mu\text{m}$  pitch, and the store section comprises 1024 x 1026 elements. In order to achieve the required fast line transfer time of  $\leq 750$  ns, a two-phase clocking scheme is used with the individual electrodes metallised to reduce their series resistance, as shown in figure 5 above. The “thin gate” process is used to minimize the on-chip power dissipation. The nominal full-well capacity is 850k electrons.



Figure 8: TropOMI (CCD275) chip schematic

The register is designed to bin up to 4 lines from the image section, and the output circuit is optimized accordingly. Read-out can be via two or four outputs, the latter halving the read-out rate  $f_R$  for possible noise reduction.

The output amplifier is a standard two-stage type but with selectable responsivity. The circuit has a node capacitance of 75 fF to give a nominal CVF of 1.4  $\mu\text{V}/\text{electron}$  and a corresponding peak signal capacity of 1.4M electrons (designated gain 1) assuming a 3V maximum swing at the node. A capability for detecting up to 3M electrons in a high signal mode (designated gain 2) is possible by switching in an additional capacitance of 90 fF to give a total capacitance of 165 fF and a nominal CVF of 0.6  $\mu\text{V}/\text{electron}$ . Dummy outputs are provided.

The noise at 5 MHz is nominally 40 electrons rms with gain 1, increasing to about 80 electrons rms with gain 2.

The device is fabricated as four different variants having the QE optimized for the wavelength bands 270-320 nm, 295-380 nm, 360-500 nm and 680-780 nm. The optimization is primarily achieved by an appropriate choice of anti-reflection coating, plus thicker silicon for the fourth.

### 3.2 Sentinel 4 (CCD374)

The Sentinel 4 spectral imaging instrument is being developed as part of the Meteosat Third Generation (MTG) mission. For this the CCD374 sensor has an asymmetric split frame-transfer format with a smaller A section referred to as Zone I UV (305-343 nm), and a larger B section as Zone II VIS (343-500 nm). The asymmetry is to minimize crosstalk with the smaller UV signals not having to traverse the high-intensity mid-range bands. All sections contain 600 columns on a 27.5 $\mu\text{m}$  horizontal pitch. Store rows adjacent to the registers have the columns slanted to facilitate the layout of additional output ports within the extent of the register. An outline chip schematic is shown in figure 9. The required 400 kHz parallel transfer frequency is possible without metallising the electrodes. The “thin gate plus” process is used with four-phase clocking to maximize the full-well capacity, which is nominally 1.6M electrons.

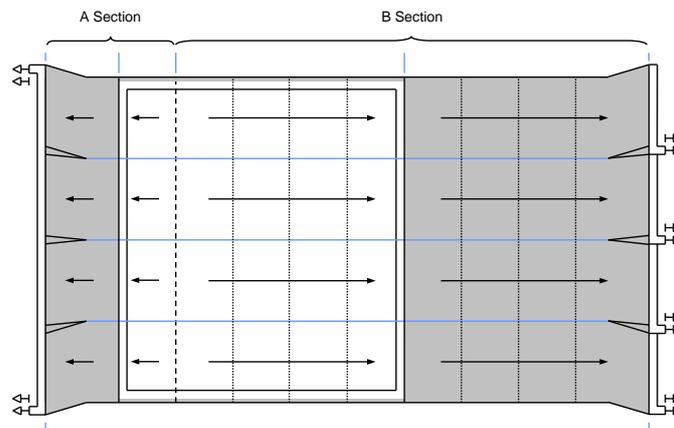


Figure 9: Sentinel 4 (CCD374) chip schematic

The A section comprises 250 image rows on a 15 $\mu\text{m}$  vertical pitch transferring into a store section with 300 rows. The serial register has an output at each end such that the user can choose to read out through either a low responsivity output (identical to those with the B section) or a High responsivity output. The B section comprises of 1000 image rows on a 15 $\mu\text{m}$  vertical pitch transferring into a store section with 1050 rows. The serial register is split into four independent sections, each interfacing with a separate low responsivity output.

The amplifiers are again two-stage types but operated with increased voltage levels to permit the signal swing at the node  $V_{SN}$  (max) to reach nearly 8V. The output drain supply is however kept within a maximum of 30V by means of reducing the channel dose in the source-follower transistors. The low responsivity amplifiers have a node capacitance  $C_N$  of 65 fF, a CVF of 1.5  $\mu\text{V}/\text{electron}$  and a peak signal capability of 3M electrons. The high responsivity amplifier has a node capacitance of 16 fF, a CVF of 5.4  $\mu\text{V}/\text{electron}$  and a peak signal capacity of 800k electrons. Additional dummy outputs are included.

The read-out rate is 1.4 MHz and since there is a requirement for reasonably fast signal settling the system bandwidth cannot be set at the minimum normally specified for minimum noise. The actual single-ended noise values are about 30 electrons rms for the low responsivity amplifiers and 14 electrons rms for the high responsivity amplifier.

The back-surface treatment is optimized for maximum QE in the UV Zone I; this gives some loss of QE in Zone II which is of no consequence because of the higher input intensity. All store sections are covered with a metal light shield.

### 3.3 Sentinel 5 (CCD314)

The prime objective of the S5 instruments is to monitor air pollution levels in the atmosphere. The detection wavelength ranges from the UV to the NIR which is achieved using three CCD314 sensors in the focal plane each having a back-thinning treatment optimized for a particular band of wavelengths (referred to as UV1, UV2VIS and NIR).

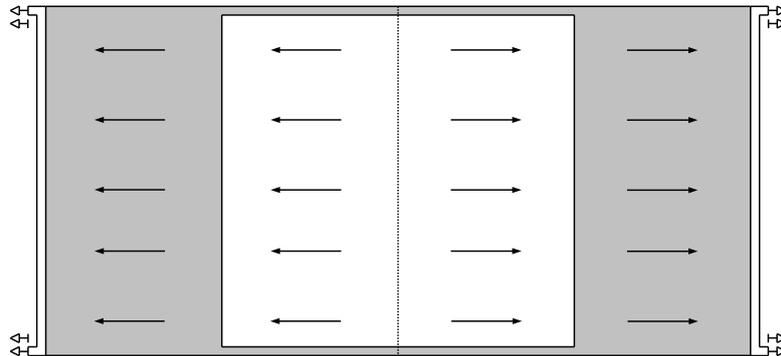


Figure 10: Sentinel 5 (CCD314) chip schematic

The CCD314 sensor is a split frame transfer type with read-out through 4 ports, as shown schematically in figure 10. The four-phase image section has a total of 1404 columns on 20  $\mu\text{m}$  pitch by 1350 rows on 30  $\mu\text{m}$  pitch, which is split into two equal independently clocked sections of 675 rows. Store sections, each with 695 rows, are placed above and below the image region, and are also independently clocked. The electrodes are not metallised and the maximum frame transfer rate is about 125 kHz. This, together with the split architecture, provides speed sufficient to minimize cross-talk. The “thin gate plus” process is used to maximize the charge storage density giving a full-well capacity of about 2M electrons.

Three-phase registers are positioned adjacent to both store sections; these have a capacity of about twice the pixel FWC. The serial read-out rate is nominally 2.94 MHz. A register dump gate is included.

The output circuits are the conventional two-stage type with a node capacitance  $C_N \sim 122$  fF to give a maximum charge handling capacity with a 3V signal swing  $N_O$  (max)  $\sim 2.3$ M electrons, exceeding the pixel FWC. The corresponding CVF  $\sim 0.85$   $\mu\text{V}/\text{electron}$  and the bandwidth is at least 20MHz. Dummy output circuits are available and are separately powered. The NES is about 50 electrons rms or 70 electrons rms differential.

### 3.4 Floris (CCD325)

The FLORIS instrument is a satellite-based imaging grating spectrometer that measures fluorescence and reflectance from vegetation. Three CCD325 sensors are required with one covering a wide spectral range (500nm to 780nm) and two covering relatively narrow ranges (677nm to 697nm and 740nm to 780nm). All devices utilize thick silicon with a broad-band anti-reflection coating peaking at about 700 nm.

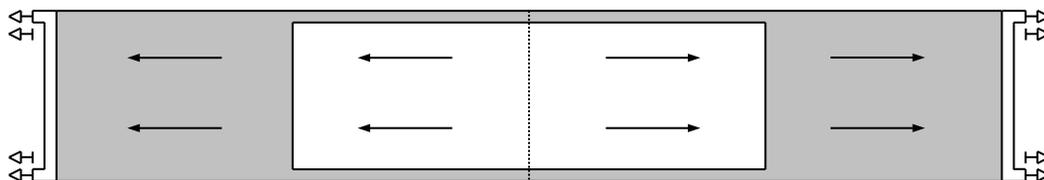


Figure 11: Floris (CCD325) chip schematic

The CCD325 sensor is a split frame transfer array of a design similar to that shown schematically in figure 10. The three-phase image section has 460 columns on 28  $\mu\text{m}$  pitch by 1072 rows on 42  $\mu\text{m}$  pitch and is split into two independently clocked sections of 536 rows. Store sections, each with 538 rows, are located above and below the image section, and are

also independently clocked. The electrodes are metallised, with the arrangement as shown in figure 4a, to permit frame transfer at frequencies of at least 800 kHz. The “thin gate” process is used and the pixel FWC  $\sim 1.3\text{M}$  electrons

Registers are placed adjacent to both store sections with a capacity of at least twice the pixel FWC to accommodate binning of two lines. A register dump gate is also included. The nominal read-out rate is 3 MHz.

The output circuits are the conventional two-stage type with a node capacitance  $C_N \sim 149\text{ fF}$  to give a maximum charge handling capacity with a 3V signal swing  $N_O$  (max)  $\sim 2.8\text{M}$  electrons, which is in excess of twice the pixel FWC. The corresponding CVF  $\sim 0.66\text{ }\mu\text{V/electron}$  and the bandwidth is about 12 MHz. Dummy output circuits are available and are separately powered. At full bandwidth the NES is about 41 electrons rms or 60 electrons rms differential.

### 3.5 3MI (CCD327)

The Selex Multi-viewing Multi-channel Multi-polarization Imager (3MI) is being developed for the MetOp-SG program under ESA contract.

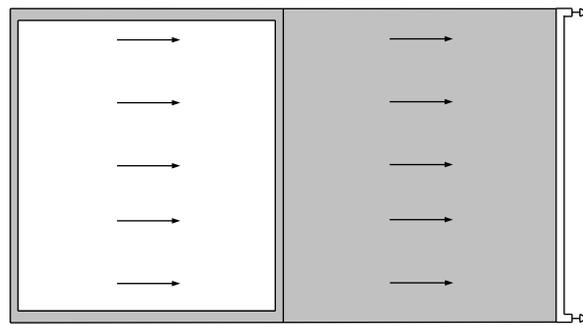


Figure 12: 3MI (CCD327) chip schematic

The CCD327 sensor being produced for this is a basic frame-transfer array with a four-phase anti-bloomed image section having 512 columns on  $26\text{ }\mu\text{m}$  pitch and 512 rows also on  $26\text{ }\mu\text{m}$  pitch active, as shown in figure 12. The total number of image elements is actually  $528 \times 516$ . The underlying store section has  $528 \times 520$  elements leading to the 3-phase serial register with output circuits at either end. Overall the device is designed to be compatible with the packaging used for the standard CCD47 device.

The standard process is used and provides a pixel FWC  $\sim 1.3\text{M}$  electrons. The output circuits are of a standard design having  $C_N \sim 63\text{ fF}$  with corresponding CVF  $\sim 1.3\text{ }\mu\text{V/electron}$ . Some adjustment of the operating voltages is required to give a signal swing  $V_{SN}$  (max) a little higher than the usual 3V to accommodate the full-well signal. The NES at full 10 MHz bandwidth is about 25 electrons rms, but the value can be reduced down to about 15 electrons rms by using an external 3 MHz pre-sampling low-pass filter (minimum  $f_B$  for the nominal 1.5 MHz read-out rate).

The device utilizes a standard broad-band anti-reflection coating to cover the 400-920 nm spectral range, rather than the wedge type.

### 3.6 MTG FCI (CIS111)

The CMOS sensor (CIS111) intended for the MTG Flexible Combined Imager (FCI) instrument has 5 independently-operated channels of large rhombus shaped 4T pixels operating at different wavelengths between 414 nm and 924 nm, as shown schematically in figure 13. The inner block has  $40\text{ }\mu\text{m}$  square pixels arranged as  $448 \times 4$ . Each of the four outer blocks has  $80\text{ }\mu\text{m}$  square pixels arranged on a staggered format of 224 rows and 4 columns. The layout of the rhombus shapes gives an effective pixel pitch that is smaller than the photodiode pitch; this is important for maximizing spatial resolution (MTF). The output circuits have CVF values between  $0.83\text{ }\mu\text{V/electron}$  and  $7.53\text{ }\mu\text{V/electron}$  to suit the signal

levels to be generated by the anticipated illumination levels. There is on-chip circuitry to select one of the four columns on read-out at 4 MHz. The device is assembled in a package that includes a ribbon flex connection, custom optical filters and a permanent window.

An important consideration is that the charge accumulated in the large photodiode transfers to the detection node in a reasonably short time period (few  $\mu\text{s}$ ) such as to not leave charge behind on read-out, a phenomenon called “lag”. This has been achieved by careful design of the transfer paths from the diode and through TG giving a residual  $< 0.1\%$ .

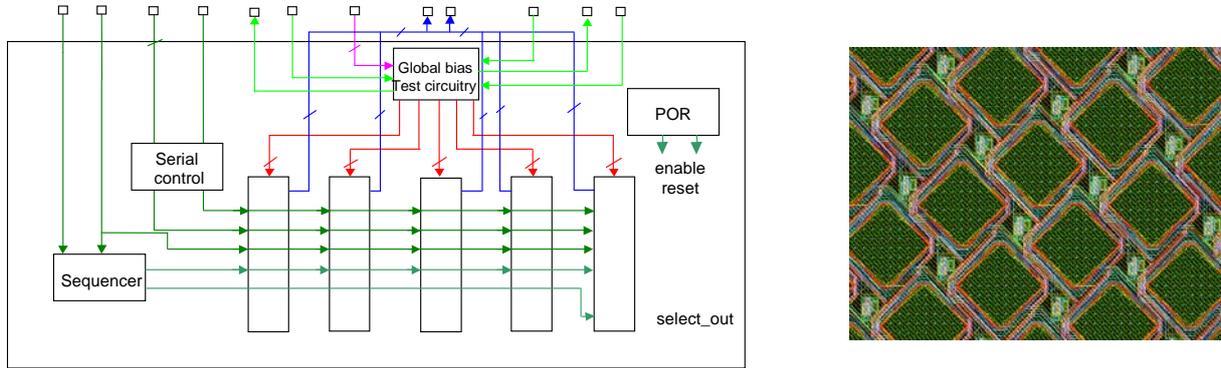


Figure 13: MTG CMOS sensor schematic and pixel array

As the pixels have a large fill-factor the QE is reasonably high front-face and the device is operated in this mode. There is, however, an undesirable feature in that with highly monochromatic light the variation of QE with wavelength shows pronounced peaks and troughs across the whole spectral range with a period that increases with wavelength, as shown in figure 14. This is termed an étalon effect and is a result of the optical interference between the light reflected from the silicon surface and that reflected from the dielectric layers covering the photodiode. At wavelengths where the waves are out-of-phase the reflection is a minimum and the QE is a maximum, where the waves are in-phase the reflection is a maximum and the QE is a minimum. Back-illuminated devices tend to show a similar effect but only at longer wavelengths (where the optical adsorption length is greater than the silicon thickness). Techniques for reducing the effect include roughening the dielectric surface and/or the use of an additional anti-reflection coating.

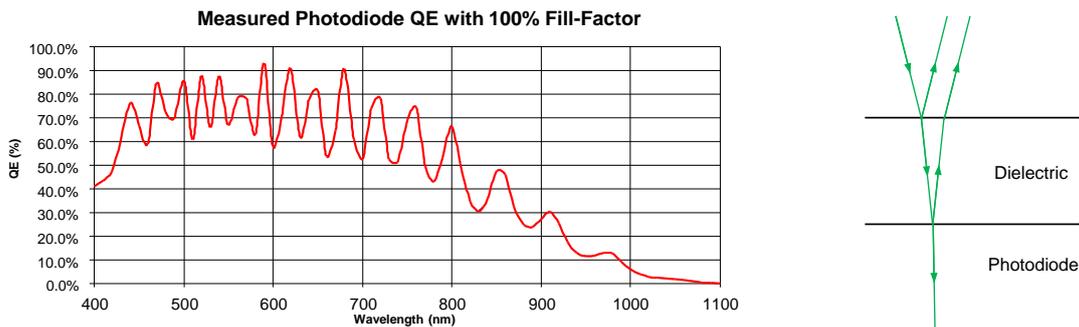


Figure 14: Optical interference effects in the photodiode

Devices have been subject to heavy ion radiation testing with excellent results. The sensor is insensitive to both single-event latch-up (SEL) and single-event upsets (SEU) in the read-out sections for ions having a linear energy transfer (LET) of up to  $67.7 \text{ MeV/mg/cm}^2$ . The design of various memory elements is known to be less hard (to save area and power consumption) and the threshold LET is lower at  $18 \text{ MeV/mg/cm}^2$ . However, from the anticipated radiation flux it is calculated that this sensitivity corresponds to only one SEU every five years.

### 3.7 MetImage (CIS116)

METImage is to be a multi-purpose instrument providing detailed information on clouds and land surface properties, together with sea, ice, and land surface temperature, thereby contributing important data for meteorological- and climate forecasting. The basic requirement is for very large pixels, 250  $\mu\text{m}$  square. To minimize transfer lag these are to be produced as a group of 8 smaller pixels with outputs feeding a common sense node, as shown schematically in figure 15.

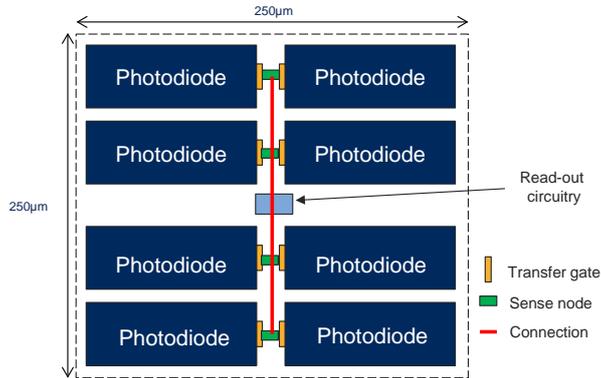


Figure 15: CIS116 Pixel

The device is currently in design using results obtained from test devices, as shown in figure 16.

	CVF ( $\mu\text{V}/\text{e}^-$ )	$N_o$ (max) (ke)	Quantum Efficiency	$V_{SO}$ (max) (V)
Variant 1	3.11	604	53.6%	1.88
Variant 3	1.97	970	52.7%	1.92
Variant 2	0.72	2505	47.8%	1.81
Variant 4	0.95	1987	47.7%	1.90
Variant 5	1.20	1495	54.1%	1.79
Variant 6	0.76	2425	43.6%	1.84
Variant 7	3.12	597	53.0%	1.86
Variant 8	2.03	950	50.3%	1.93

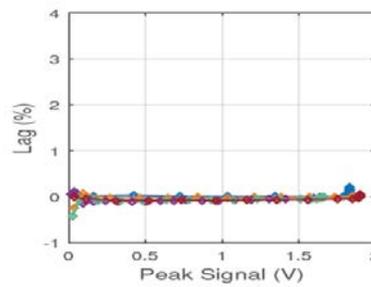


Figure 16: CIS116 Test results

The lag is virtually zero. The rms noise floor of the read-out chain is typically 120 $\mu\text{V}$  using a low noise video output or 300 $\mu\text{V}$  using a drive circuit capable of large loading. Dividing by the CVF gives the NES value in electrons. The somewhat higher values are simply a consequence of the large value of node capacitance being necessary to detect these large signals, e.g.  $C_N \sim 230$  fF to detect 2.5M electrons with  $V_{SO}$  (max)  $\sim 1.8\text{V}$ . The dynamic ranges are however large, approximately 84dB, as was described in section 3.2.

### 3.8 New CMOS developments

Various developments are in progress at e2v.

#### 3.8.1 Back-illumination

The manufacturing techniques developed for the fabrication of back-illuminated CCD sensors are being extended to CMOS sensors. The CIS115 sensor with 2K $\times$ 1.5K pixels each 7  $\mu\text{m}$  square is being used in a programme to fully space-qualify a back-thinned CMOS sensor against the ESA9020 standard.

A difficulty with CMOS sensors is to achieve the thick fully-depleted silicon required for extended red response with the constraints imposed by modern processes. The depth of depletion is given by:

$$X_D = [2\epsilon_0\epsilon_s V_D/qN_A]$$

where  $V_D$  is the depleting voltage and  $N_A$  is the substrate doping concentration. Typically, with a pinned photodiode  $V_D$  is about 1V and the lowest practical value for  $N_A$  is about  $1 \times 10^{13} /\text{cm}^3$  (resistivity  $\sim 1\text{k}\Omega \cdot \text{cm}$ ) giving  $X_D \sim 10 \mu\text{m}$ . In practice the value can be somewhat smaller through the shielding effects of adjacent structures. One possibility for improvement is to apply a negative bias to the back surface to increase the value of  $V_D$ , but a complication is that high leakage currents can then flow between the back surface and front-surface p+ regions. Experiments are currently in progress with the inclusion of internal structures aimed at blocking these paths.

### 3.8.2 TDI sensors

Devices described so far essentially operate in a push-broom mode with a succession of snap-shot images taken with an integration time that is sufficiently short to minimize image smear. In some applications it can be possible to operating in a “time-delay-and-integration” (TDI) mode with a considerable improvement in the along-track resolution. This is easily achieved in CCD by a clocking scheme that moves the potential wells to match the image movement over the sensor. The signal summation is in the charge domain and noiseless, so the maximum dynamic range is set by the full-well capacity and the output circuit noise. In CMOS sensors with a conventional pixel giving a voltage output achieving a TDI function is possible by signal summing in the external electronics. For  $M$  lines summed, effectively the peak signal is  $M \times N_O$  (max) and the noise is  $\sqrt{M} \times \text{NES}$ . The overall dynamic range therefore increases by a factor  $\sqrt{M}$ , but at the expense of higher noise. The fact that considerable signal processing is involved means that there is likely to be a significant increase in the power dissipation as  $M$  increases. It could therefore be an advantage for larger  $M$ , say  $>5$ , to fabricate a CCD-type structure within a CMOS sensor.

Most CCD sensors utilize several levels of overlapping polysilicon to fabricate the electrode structures. However, such multiple layers are not generally available in modern CMOS foundry processes. Various alternative approaches have been developed at e2v with considerable success<sup>2</sup>. One possibility is to use a single polysilicon layer with etched gaps, but it can be difficult to adapt the process to dope the electrodes (to lower the resistance) and avoid dopant being present in the gap regions. An alternative is to use single-layer polysilicon electrodes in combination with diffused virtual-phase type electrodes formed from the pinned photodiode dopants. Results for the two approaches using test devices with  $10 \mu\text{m}$  square elements are as follows.

	Basic CCD	Virtual phase
$N_O$ (max): electrons	110k	18k
Dark signal: nA/cm <sup>2</sup>	12	2
Charge transfer inefficiency	$2 \times 10^{-4}$	$7 \times 10^{-5}$
QE at 400/600/900 nm %	2/45/10	30/42/10

The CTI is not as low as the conventional CCDs at e2v, but is more than sufficient for the small number of transfers generally required for earth observation systems. A useful feature is that the increase with radiation is smaller than with CCD, the CTI roughly doubling after a dose of  $10^{11}$  protons/cm<sup>2</sup>.

## REFERENCES

- [1] D. Burt, J. Endicott, P. Jerram, et al., “Improving radiation tolerance in e2v CCD sensors,” Proc. SPIE, vol. 7439, 2015.
- [2] F Mayer et al., “First Measurements of True Charge Transfer TDI Using a Standard CMOS Technology” International Conference on Space Optics, 2012